

TC551001BPL/BFL/BFTL/BTRL-70L/85L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL	
	-70L	-85L
Access Time	70ns	85ns
$\overline{CE1}$ Access Time	70ns	85ns
CE2 Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

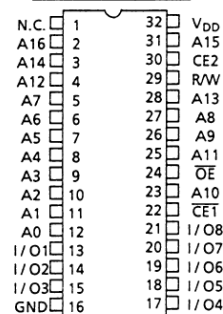
- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package
 - TC551001BPL : DIP32-P-600
 - TC551001BFL : SOP32-P-525
 - TC551001BFTL : TSOP32-P-0820
 - TC551001BTRL : TSOP32-P-0820A

Pin Names

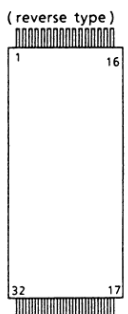
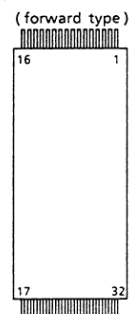
A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

Pin Connection (Top View)

○ 32 PIN DIP & SOP



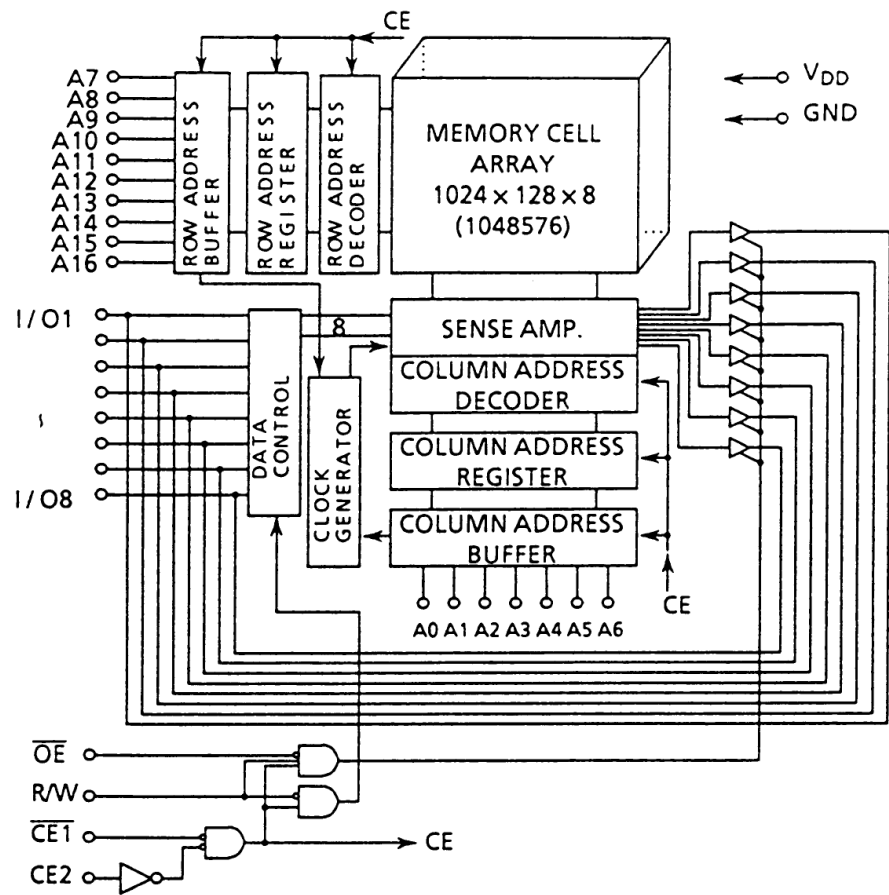
○ 32 PIN TSOP



TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDS}
	*	L	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature (10s)	260	°C
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width of 50ns Max

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V at pulse width of 50ns Max.

DC and Operating Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
				1μs	—	—	20	
I _{DDO2}		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
				1μs	—	—	10	
I _{BDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}			—	—	3	mA
I _{BDS2} ⁽¹⁾		CE1 = V _{DD} - 0.2V or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C		—	—	30	μA
			Ta = 25°C		—	2	4	

Note: (1) In standby mode with $\overline{CE1} \geq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)**Read Cycle**

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	–	85	–	ns
t _{ACC}	Address Access Time	–	70	–	85	
t _{CO1}	CE1 Access Time	–	70	–	85	
t _{CO2}	CE2 Access Time	–	70	–	85	
t _{OE}	Output Enable to Output in Valid	–	35	–	45	
t _{COE}	Chip Enable ($\overline{\text{CE}}1$, CE2) to Output in Low-Z	10	–	10	–	
t _{OOE}	Output Enable to Output in Low-Z	5	–	5	–	
t _{OD}	Chip Enable ($\overline{\text{CE}}1$, CE2) to Output in High-Z	–	25	–	30	
t _{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t _{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

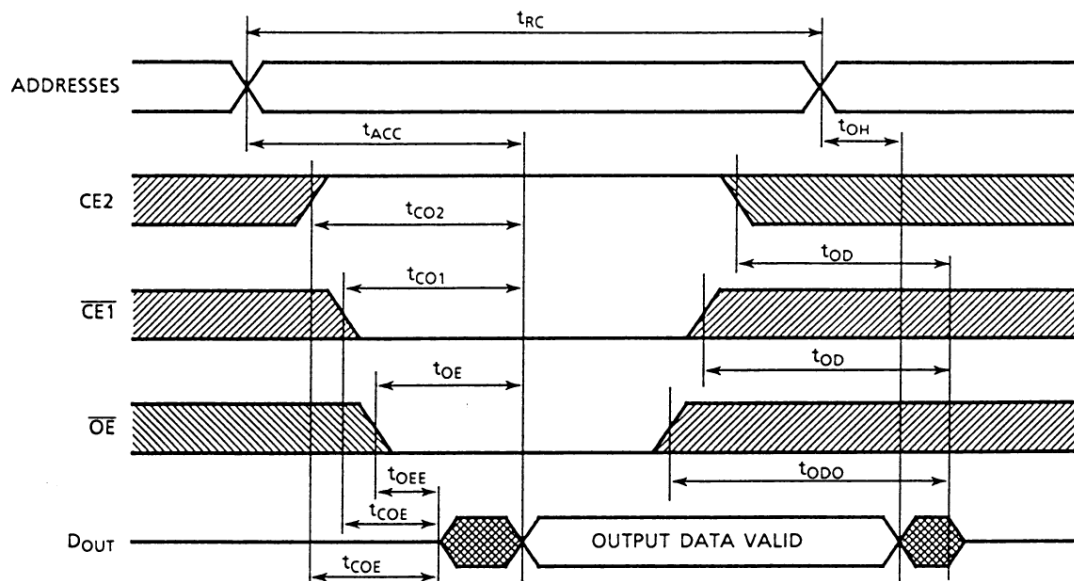
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	–	85	–	ns
t _{WP}	Write Pulse Width	50	–	60	–	
t _{CW}	Chip Selection to End of Write	60	–	75	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W to Output in High-Z	–	25	–	30	
t _{OEW}	R/W to Output in Low-Z	5	–	5	–	
t _{DS}	Data Setup Time	30	–	35	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

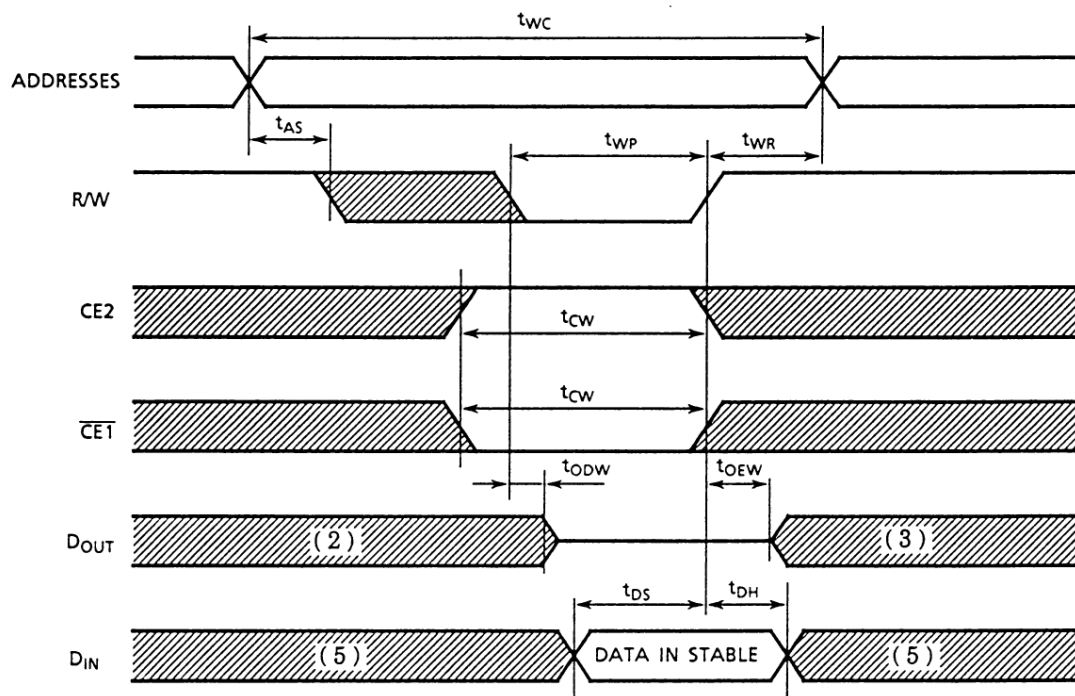
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C _L = 100pF

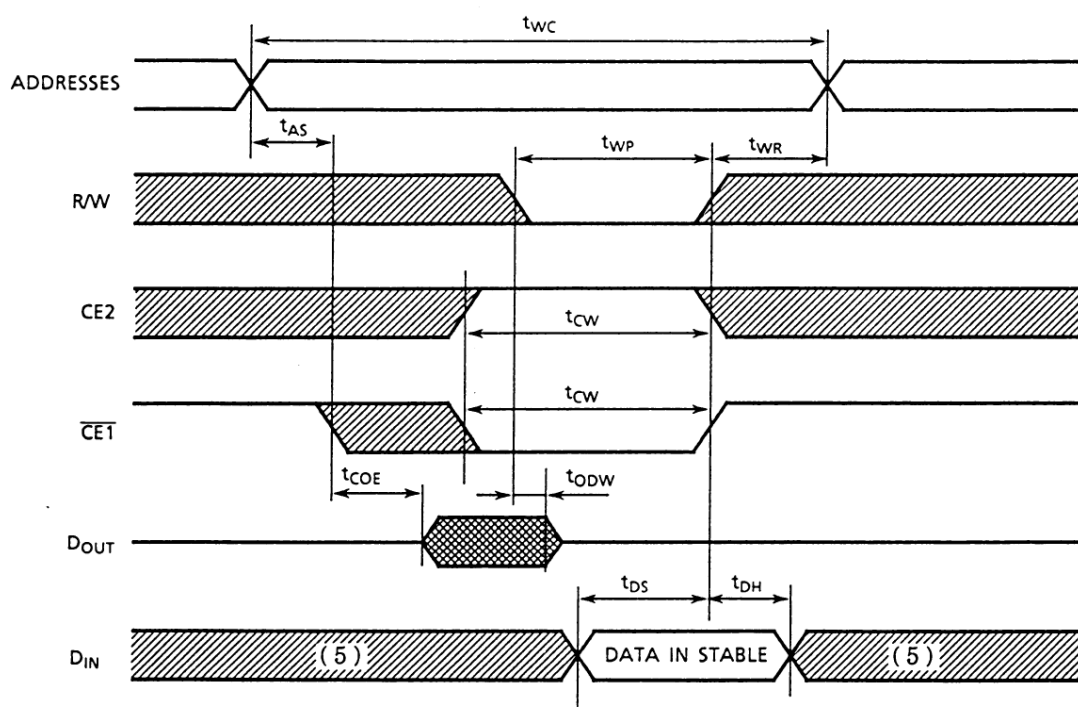
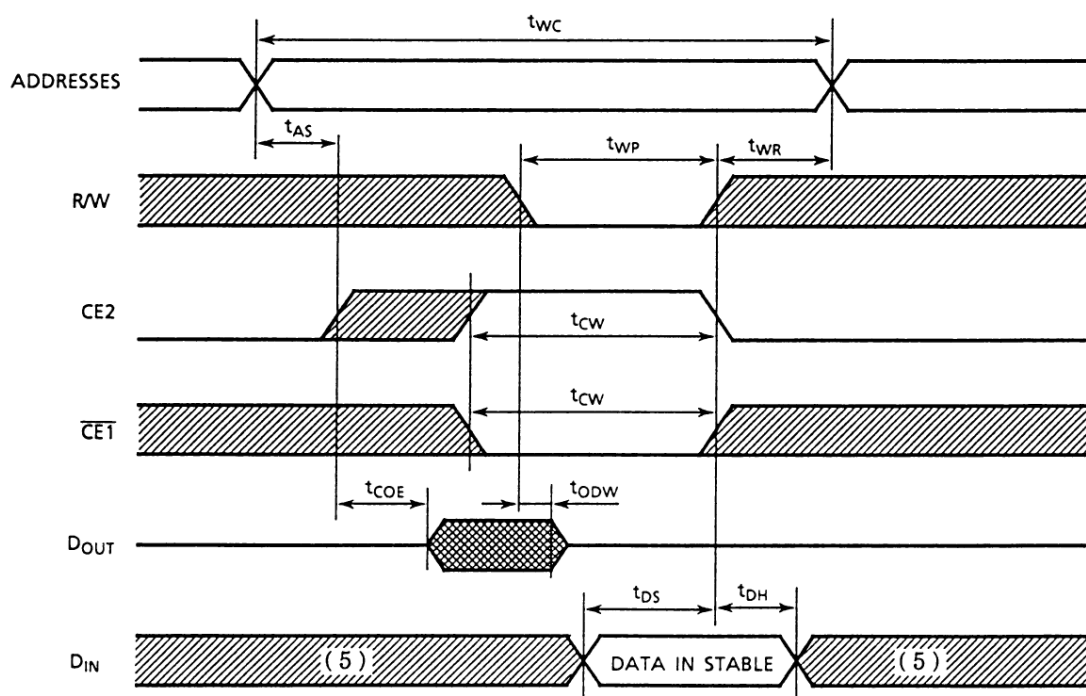
Timing Waveforms

Read Cycle ⁽¹⁾



Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)

Notes:

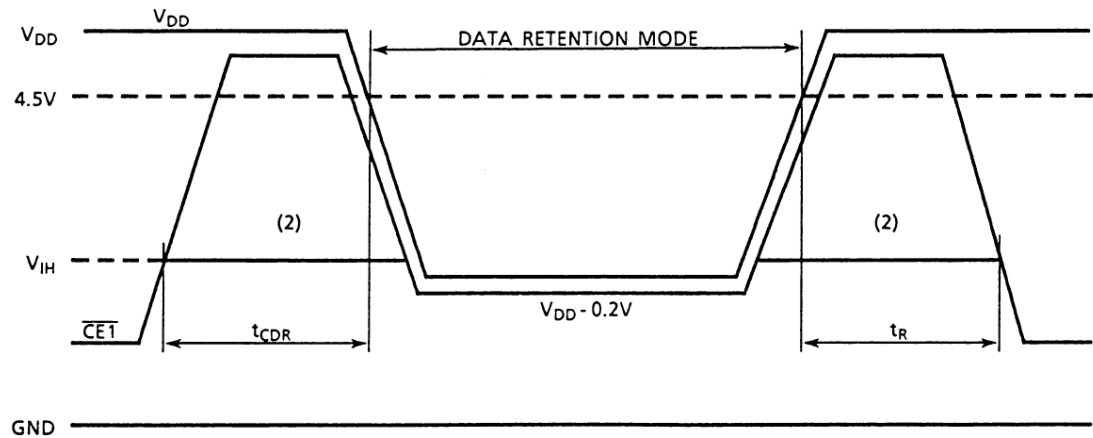
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W high transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

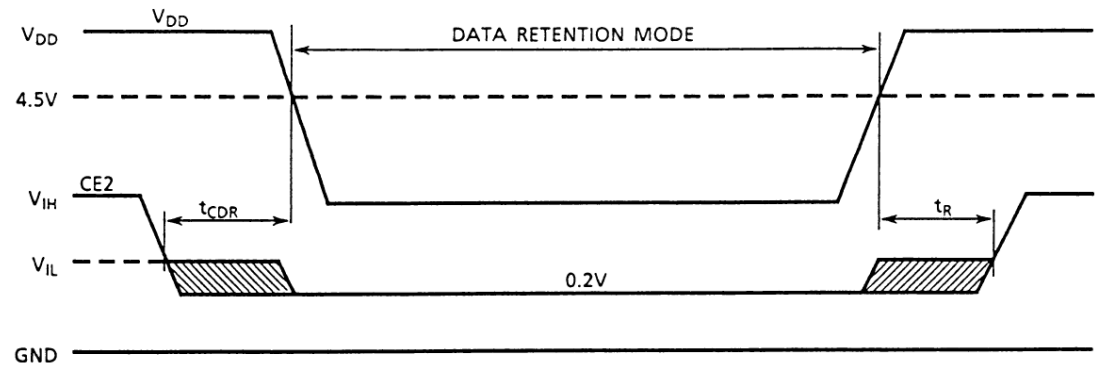
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I _{DDS2}	Standby Current	V _{DD} = 3.0V	—	—	15*	μA
		V _{DD} = 5.5V	—	—	30	
t _{CDR}	Chip Deselect to Data Retention Mode		0	—	—	ns
t _R	Recovery Time		5	—	—	ms

*3μA (max.) Ta = 0 ~ 40°C

CE1 Controlled Data Retention Mode ⁽¹⁾



CE2 Controlled Data Retention Mode ⁽³⁾

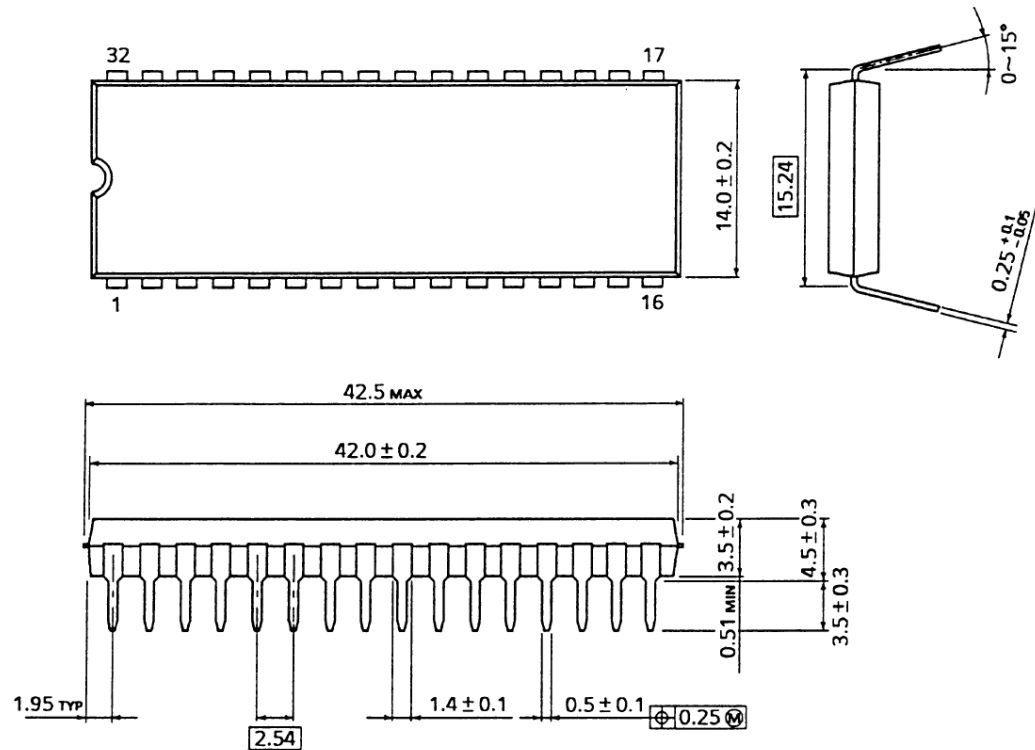


- Notes:
1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$ or $\text{CE2} \geq V_{\text{DD}} - 0.2\text{V}$.
 2. If the V_{IH} of $\overline{\text{CE1}}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.
 3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$.

Outline Drawing

DIP32-P-600

Unit in mm

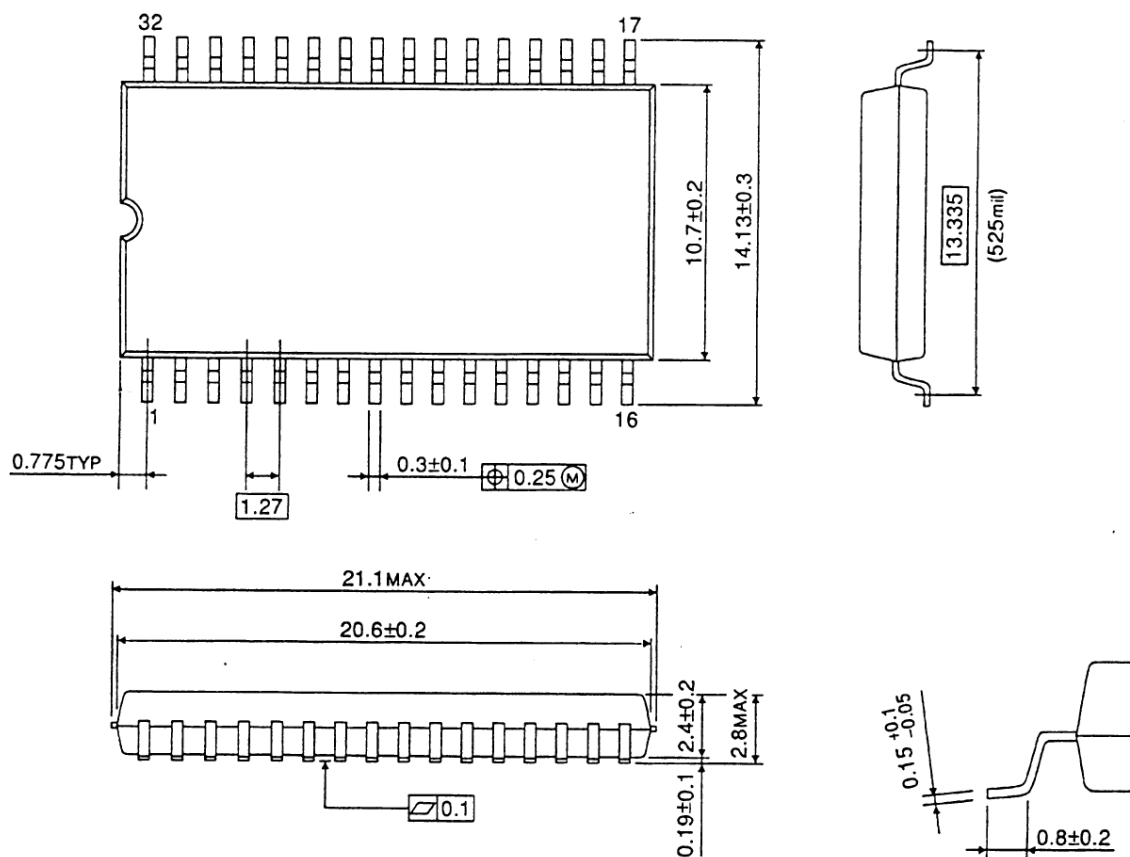


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

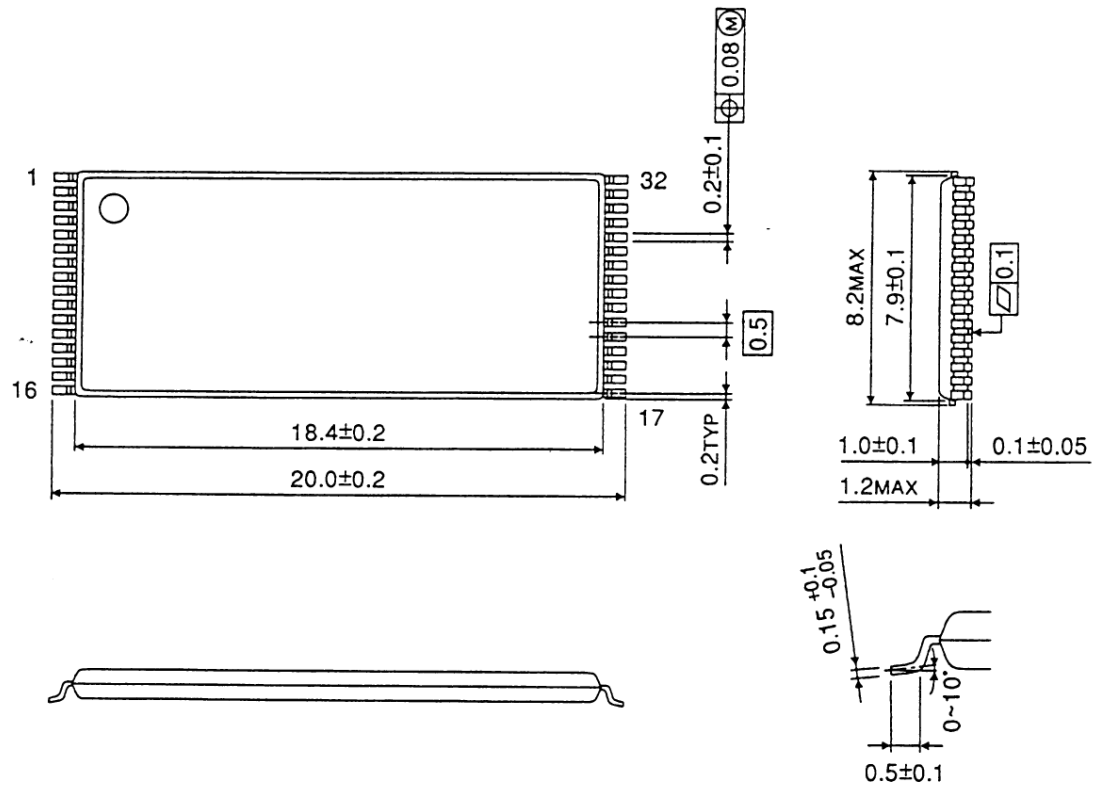


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

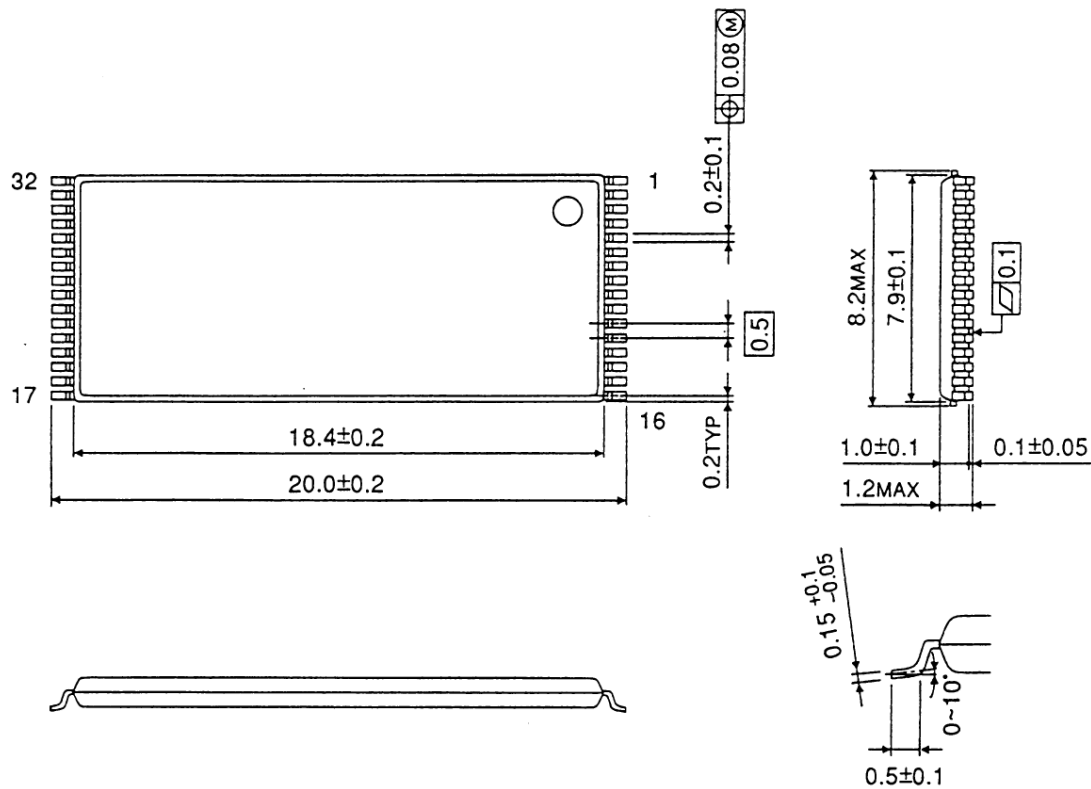


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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