

NL17SZ06

Single Inverter with Open Drain Outputs

The NL17SZ06 is a high performance single inverter with open drain outputs operating from a 1.65 to 5.5 V supply.

The Output stage is open drain with Over Voltage Tolerance. This allows the NL17SZ06 to be used to interface 5.0 V circuits to circuits of any voltage between 0 and +7.0 V.

Features

- Tiny SOT-353 and SOT-553 Packages
- Extremely High Speed: t_{PD} 2.5 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation, CMOS Compatible
- Over Voltage Tolerant Inputs V_{IN} may be Between 0 and 7.0 V for V_{CC} Between 0.5 and 5.5 V
- TTL Compatible – Interface Capability with 5.0 V TTL Logic with $V_{CC} = 2.7$ V to 3.6 V
- LVCMOS Compatible
- 24 mA Output Sink Capability, Pullup may be between 0 and 7.0 V
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Chip Complexity: FET = 20
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

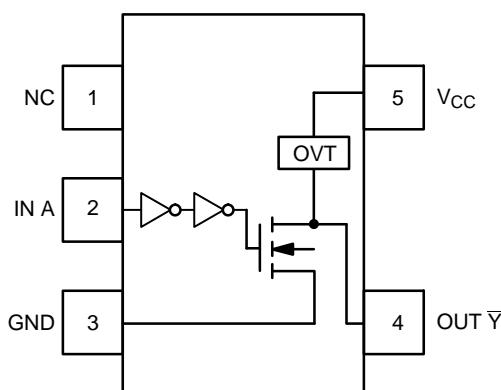


Figure 1. Pinout (Top View)

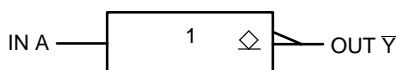


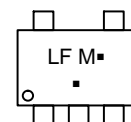
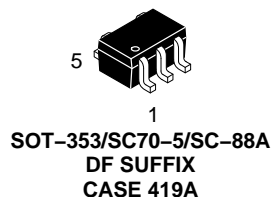
Figure 2. Logic Symbol



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MARKING DIAGRAMS



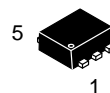
LF = Specific Device Marking

M = Date Code*

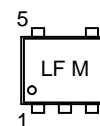
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.



SOT-553
XV5 SUFFIX
CASE 463B



LF = Specific Device Marking

M = Date Code

PIN ASSIGNMENT

Pin	Function
1	NC
2	IN A
3	GND
4	OUT \bar{Y}
5	V_{CC}

FUNCTION TABLE

A Input	\bar{Y} Output
L	Z
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NL17SZ06

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0	V
V _I	DC Input Voltage	−0.5 ≤ V _I ≤ +7.0	V
V _O	DC Output Voltage Output in Z or LOW State (Note 1)	−0.5 ≤ V _O ≤ 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	−50	mA
I _{OK}	DC Output Diode Current V _O < GND	−50	mA
I _O	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current Per Supply Pin	±100	mA
I _{GND}	DC Ground Current Per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
P _D	Power Dissipation in Still Air SOT−353 SOT−553	186 135	mW
θ _{JA}	Thermal Resistance SOT−353 SOT−553	350 496	°C/W
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
I _{Latch-Up}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 5)	±100	mA
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
ESD	ESD Classification Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	2000 200 N/A	V V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A, rated to EIA/JESD22−A114−B.
3. Tested to EIA/JESD22−A115−A, rated to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage (Z or LOW State)	0	5.5	V
T _A	Operating Free−Air Temperature	−55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ±0.2 V V _{CC} = 3.0 V ±0.3 V V _{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V
I _{LKG}	Z-State Output Leakage Current	V _{IN} = V _{IL} V _{OUT} = V _{CC} or GND	2.3 to 5.5			±5.0		±10.0	μA
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.65 to 5.5		0.0	0.1		0.1	V
		I _{OL} = 4 mA	1.65		0.08	0.24		0.24	
		I _{OL} = 8 mA	2.3		0.22	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0			1.0		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5			1.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PZL}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 500 Ω, C _L = 50 pF	1.65	0.8	5.3	11.6	0.8	12.0	ns
			2.5 ± 0.2	0.8	3.0	3.6	0.8	4.1	
			3.3 ± 0.3	0.8	2.4	3.2	0.8	3.7	
			5.0 ± 0.5	0.5	2.4	3.0	0.5	3.5	
t _{PLZ}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 500 Ω, C _L = 50 pF	1.65	0.8	5.3	11.6	0.8	12.0	ns
			2.5 ± 0.2	0.8	2.5	3.6	0.8	4.1	
			3.3 ± 0.3	0.8	2.1	3.2	0.8	3.7	
			5.0 ± 0.5	0.5	1.2	3.0	0.5	3.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	> 2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4.0	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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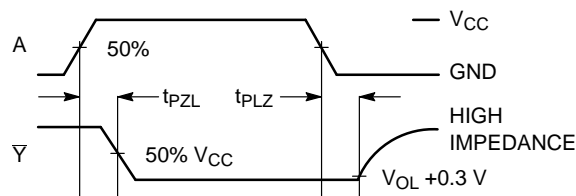


Figure 3. Switching Waveforms

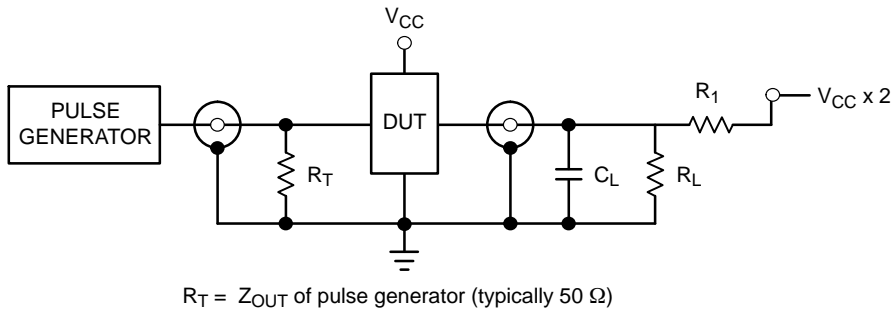


Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size†
NL17SZ06DFT2G	SOT-353/SC70-5/SC-88A (Pb-Free)	3000 / Tape & Reel
NL17SZ06XV5T2G	SOT-553 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

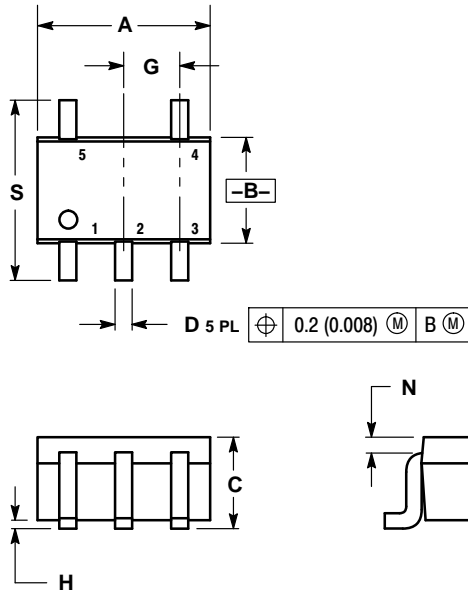
NL17SZ06

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)

CASE 419A-02

ISSUE L

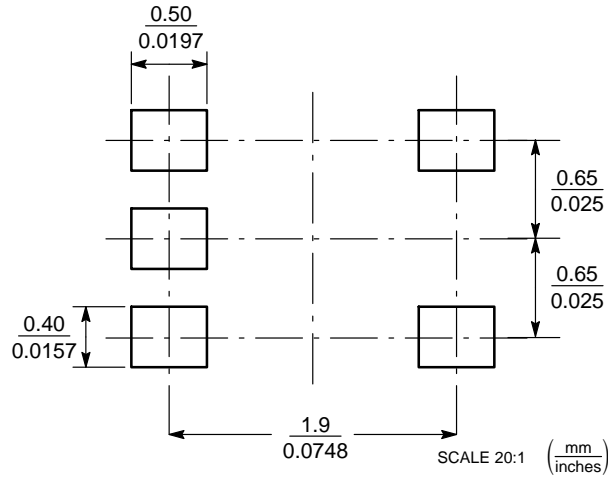


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT*

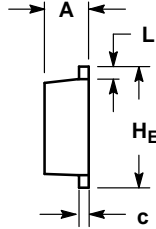
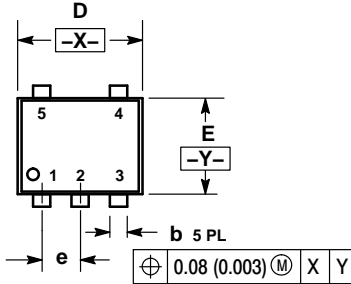


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOT-553 XV5 SUFFIX CASE 463B ISSUE C

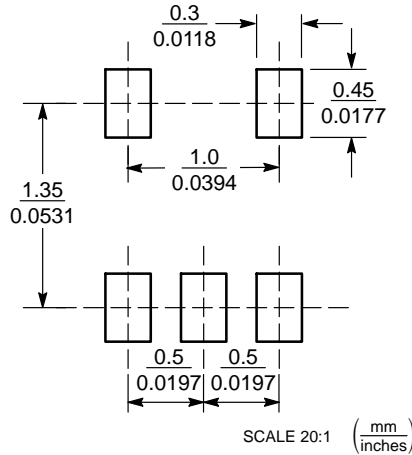


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.55	1.60	1.65	0.061	0.063	0.065

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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