

## CRYSTAL-TO-MLVDS PCI EXPRESS™ CLOCK SYNTHESIZER W/SPREAD SPECTRUM

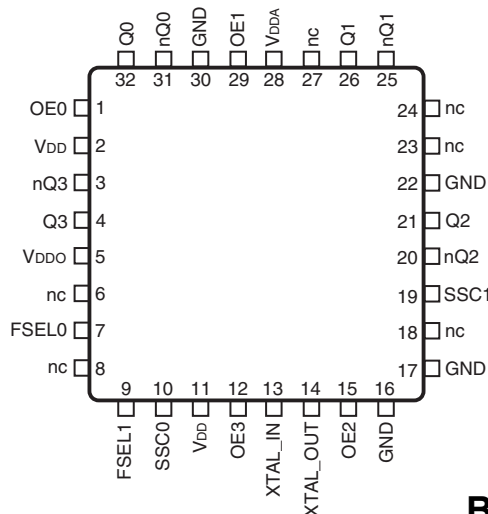
## ICS845204

### General Description



The ICS845204 is a 4 output PCI Express clock synthesizer optimized to generate low jitter PCI Express™ reference clocks with or without spread spectrum modulation and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. Spread type and amount can be configured via the SSC control pins. Using a 25MHz, 18pF parallel resonant crystal, the device will generate M-LVDS clocks at either 25MHz, 100MHz, 125MHz or 250MHz. The ICS845204 uses a low jitter VCO that easily meets PCI Express jitter requirements and is packaged in a 32-pin VFQFN package.

### Pin Assignment



**ICS845204**

**32 Lead VFQFN**

**5mm x 5mm x 0.925mm**

**package body**

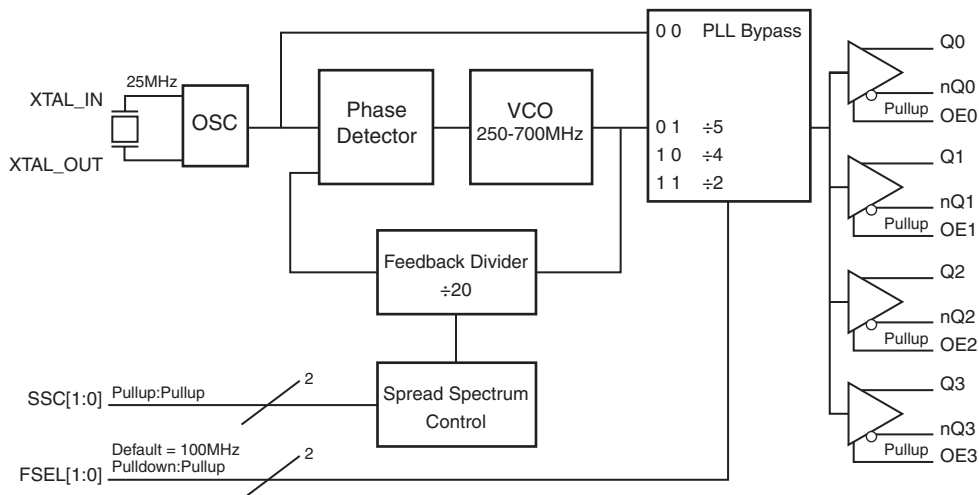
**K Package**

**Top View**

### Features

- Four differential spread spectrum clock outputs
- Each output can be individually disabled by separate output-enable inputs
- Crystal oscillator interface designed for 18pF, 25MHz parallel resonant crystal
- Supports the following output frequencies: 25MHz, 100MHz, 125MHz or 250MHz
- VCO range: 250MHz - 700MHz
- Supports SSC downspread at 0.05% and -0.75%, centerspread at  $\pm 0.25\%$  and no spread options
- Cycle-to-cycle jitter: 50ps (maximum) design target
- Period jitter, RMS: TBD
- Full 3.3V output supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

### Block Diagram



The Advance Information presented herein represents a product that is developmental or prototype. The noted characteristics are design targets. Integrated Device Technologies, Inc. (IDT) reserves the right to change any circuitry or specifications without notice.

**Table 1. Pin Descriptions**

| Number                  | Name                | Type   |          | Description                                                                                                                           |
|-------------------------|---------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------|
| 1                       | OE0                 | Input  | Pullup   | Output enable pin for Q0/nQ0 outputs. Logic High, outputs are enabled. Logic LOW, outputs are in Hi-Z. LVCMOS/LVTTL interface levels. |
| 2, 11                   | V <sub>DD</sub>     | Power  |          | Core supply pins.                                                                                                                     |
| 3, 4                    | nQ3, Q3             | Output |          | Differential output pair. M-LVDS interface levels.                                                                                    |
| 5                       | V <sub>DDO</sub>    | Power  |          | Output supply pin.                                                                                                                    |
| 6, 8, 18, 23,<br>24, 27 | nc                  | Unused |          | No connect.                                                                                                                           |
| 7                       | FSEL0               | Input  | Pullup   | Output frequency select pins. See Table 3A. LVCMOS/LVTTL interface levels.                                                            |
| 9                       | FSEL1               | Input  | Pulldown | Output frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.                                                             |
| 10,<br>19               | SSC0,<br>SSC1       | Input  | Pullup   | Spread spectrum control pins. See Table 3B. LVCMOS/LVTTL interface levels.                                                            |
| 12                      | OE3                 | Input  | Pullup   | Output enable pin for Q3/nQ3 outputs. Logic High, outputs are enabled. Logic LOW, outputs are in Hi-Z. LVCMOS/LVTTL interface levels. |
| 13,<br>14               | XTAL_IN<br>XTAL_OUT | Input  |          | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.                                                           |
| 15                      | OE2                 | Input  | Pullup   | Output enable pin for Q2/nQ2 outputs. Logic High, outputs are enabled. Logic LOW, outputs are in Hi-Z. LVCMOS/LVTTL interface levels. |
| 16, 17, 22, 30          | GND                 | Power  |          | Power supply ground.                                                                                                                  |
| 20, 21                  | nQ2, Q2             | Output |          | Differential output pair. M-LVDS interface levels.                                                                                    |
| 25, 26                  | nQ1, Q1             | Output |          | Differential output pair. M-LVDS interface levels.                                                                                    |
| 28                      | V <sub>DDA</sub>    | Power  |          | Analog supply pin.                                                                                                                    |
| 29                      | OE1                 | Input  | Pullup   | Output enable pin for Q1/nQ1 outputs. Logic High, outputs are enabled. Logic LOW, outputs are in Hi-Z. LVCMOS/LVTTL interface levels. |
| 31, 32                  | nQ0, Q0             | Output |          | Differential output pair. M-LVDS interface levels.                                                                                    |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Function Tables

Table 3A. F\_SEL[1:0] Function Table

| Inputs |       | Outputs            |
|--------|-------|--------------------|
| FSEL1  | FSEL0 | Q[0:3]/nQ[0:3]     |
| 0      | 0     | PLL Bypass (25MHz) |
| 0      | 1     | 100MHz (default)   |
| 1      | 0     | 125MHz             |
| 1      | 1     | 250MHz             |

Table 3B. SSC[1:0] Function Table

| Inputs |      | Spread%             |
|--------|------|---------------------|
| SSC1   | SSC0 |                     |
| 0      | 0    | Center $\pm$ -0.25  |
| 0      | 1    | Down -0.5           |
| 1      | 0    | Down -0.75          |
| 1      | 1    | No Spread (default) |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                                  | Rating                   |
|-------------------------------------------------------|--------------------------|
| Supply Voltage, $V_{DD}$                              | 4.6V                     |
| Inputs, $V_I$                                         | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | 10mA<br>15mA             |
| Package Thermal Impedance, $\theta_{JA}$              | 42.4°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$                        | -65°C to 150°C           |

## DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ 

| Symbol    | Parameter             | Test Conditions | Minimum                       | Typical | Maximum  | Units |
|-----------|-----------------------|-----------------|-------------------------------|---------|----------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135                         | 3.3     | 3.465    | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | $V_{DD} - I_{DDA} * 10\Omega$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135                         | 3.3     | 3.465    | V     |
| $I_{DD}$  | Power Supply Current  |                 |                               | TBD     |          | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |                               | TBD     |          | mA    |
| $I_{DDO}$ | Power Supply Current  |                 |                               | TBD     |          | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol   | Parameter          |                            | Test Conditions                | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|----------------------------|--------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                            |                                | 2       |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                            |                                | -0.3    |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | F_SEL1                     | $V_{DD} = V_{IN} = 3.465V$     |         |         | 150            | $\mu A$ |
|          |                    | SSC0, SSC1, FSEL0, OE0:OE3 | $V_{DD} = V_{IN} = 3.465V$     |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | F_SEL1                     | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                    | SSC0, SSC1, FSEL0, OE0:OE3 | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |         |                | $\mu A$ |

**Table 4C. M-LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol          | Parameter                    | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|------------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage  |                 | 480     |         | 650     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change    |                 |         | 50      |         | mV    |
| $V_{OS}$        | Offset Voltage               |                 | 0.30    |         | 2.10    | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change    |                 |         | 50      |         | mV    |
| $I_{SC}$        | Output Short Circuit Current |                 |         |         | 43      | mA    |

**Table 5. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |
| Drive Level                        |                 |             |         | TBD     | mW       |

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ$**

| Parameter      | Symbol                              | Test Conditions                             | Minimum | Typical | Maximum | Units |
|----------------|-------------------------------------|---------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$      | Output Frequency                    |                                             |         | 25      |         | MHz   |
|                |                                     |                                             |         | 100     |         | MHz   |
|                |                                     |                                             |         | 125     |         | MHz   |
| $f_{jit(per)}$ | Period Jitter, Random               | 25MHz,<br>Integration Range: 12kHz – 20MHz  |         | TBD     |         | ps    |
|                |                                     | 100MHz,<br>Integration Range: 12kHz – 20MHz |         | TBD     |         | ps    |
|                |                                     | 125MHz,<br>Integration Range: 12kHz – 20MHz |         | TBD     |         | ps    |
|                |                                     | 250MHz,<br>Integration Range: 12kHz – 20MHz |         | TBD     |         | ps    |
| $f_{jit(cc)}$  | Cycle-to-Cycle Jitter;<br>NOTE 1, 2 | 25MHz                                       |         |         | 50      | ps    |
|                |                                     | 100MHz                                      |         |         | 50      | ps    |
|                |                                     | 125MHz                                      |         |         | 50      | ps    |
|                |                                     | 250MHz                                      |         |         | 50      | ps    |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3              |                                             |         | TBD     |         | ps    |
| $F_{XTAL}$     | Crystal Input Range: NOTE 1         |                                             |         | 25      |         | MHz   |
| $F_M$          | SSC Modulation Frequency;<br>NOTE 4 |                                             |         | TBD     |         | kHz   |
| $F_{MF}$       | SSC Modulation Factor;<br>NOTE 4    |                                             |         | TBD     |         | %     |
| $SSC_{RED}$    | Spectral Reduction                  |                                             |         | TBD     |         | dB    |
| $t_{STABLE}$   | Power-up Stable Clock<br>Output     |                                             |         |         | 10      | ms    |
| $t_R / t_F$    | Output Rise/Fall Time               | 20% to 80%                                  |         | TBD     |         | ps    |
| odc            | Output Duty Cycle                   |                                             |         | 50      |         | %     |

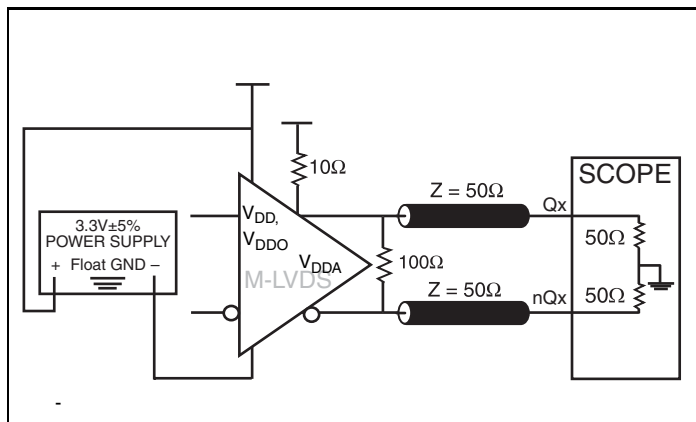
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Only valid within the VCO operating range.

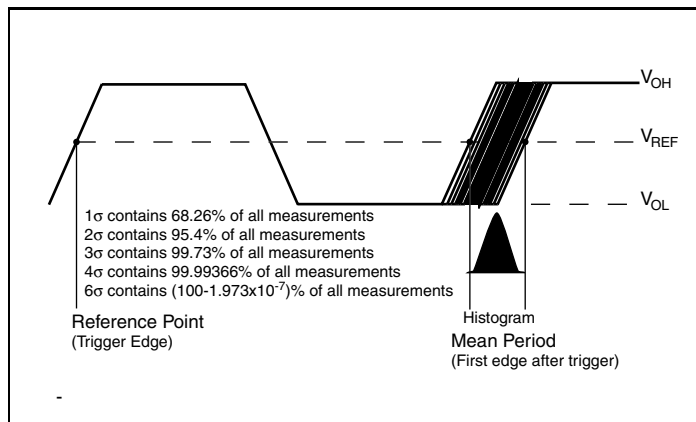
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.  
Measured at the output differential cross points.

NOTE 4: Spread Spectrum clocking enabled.

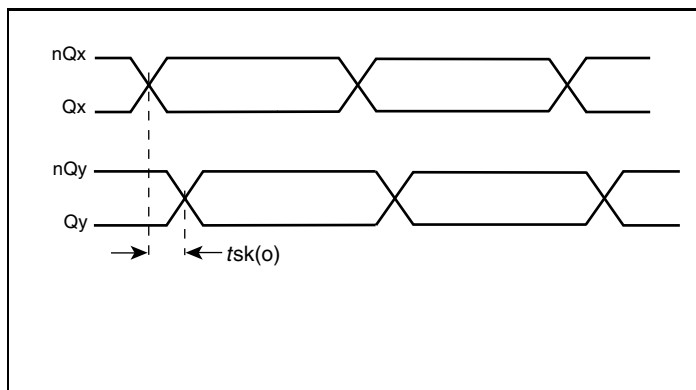
## Parameter Measurement Information



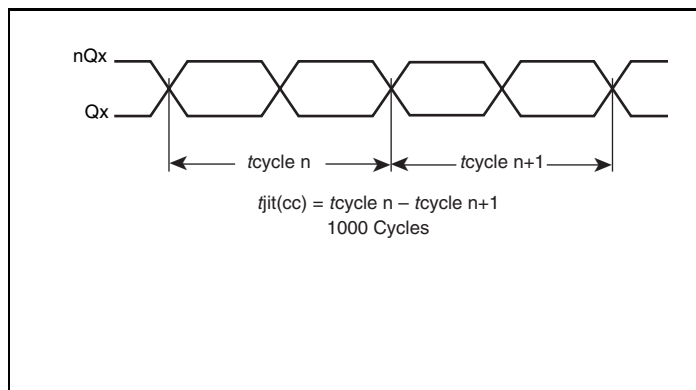
3.3V LVDS Output Load AC Test Circuit



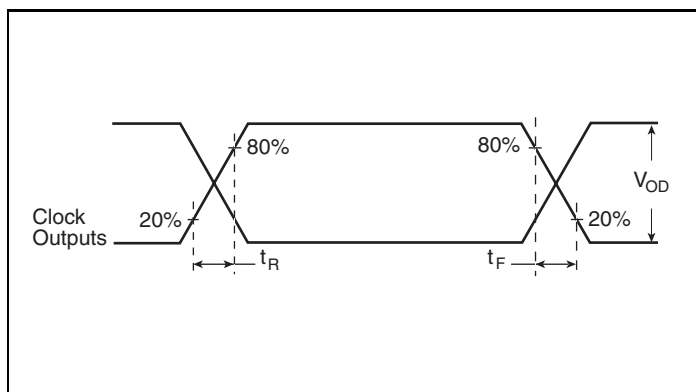
Period Jitter



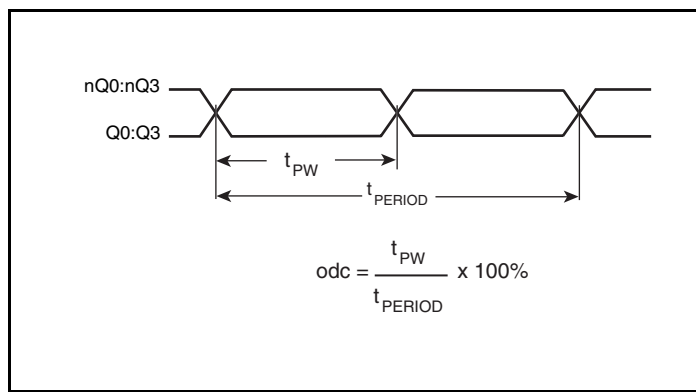
Output Skew



Cycle-to-Cycle Jitter

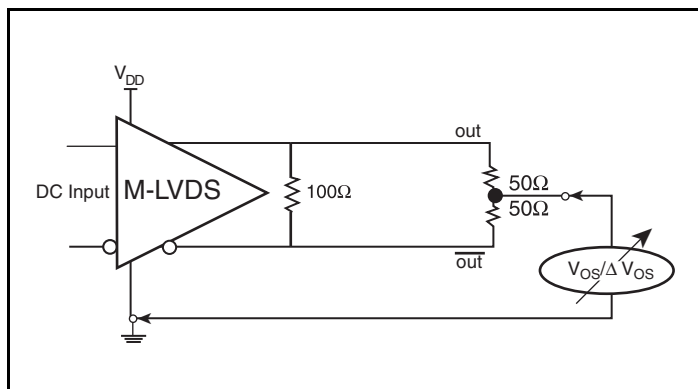


Output Rise/Fall Time

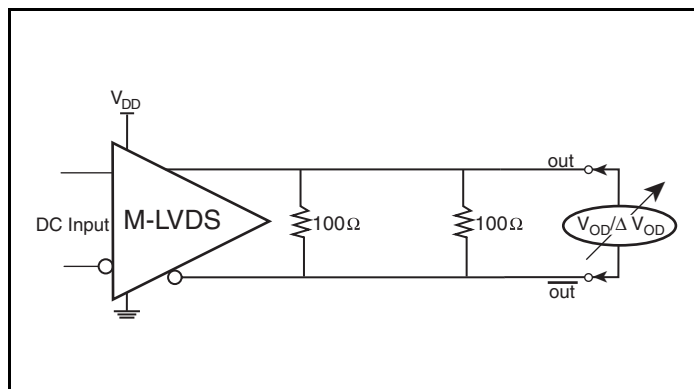


Output Duty Cycle/Pulse Width/Period

## Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS845204 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a 0.01μF bypass capacitor should be connected to each  $V_{DDA}$  pin.

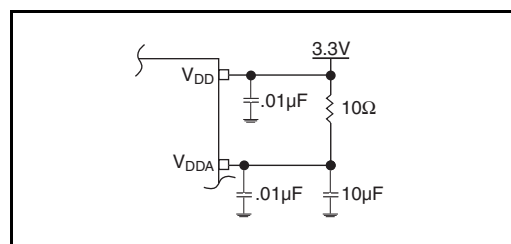


Figure 1. Power Supply Filtering

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

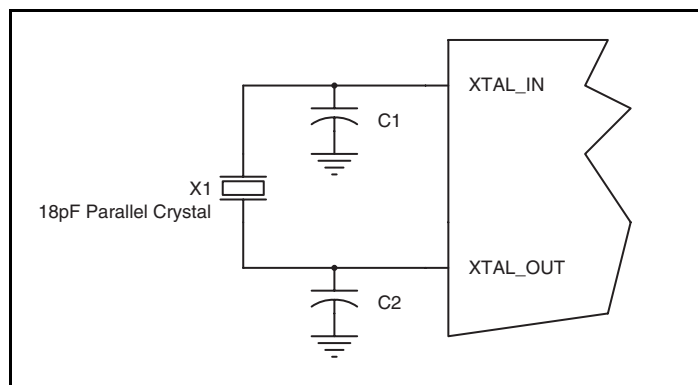
#### M-LVDS Outputs

All unused M-LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## Crystal Input Interface

The ICS845204 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

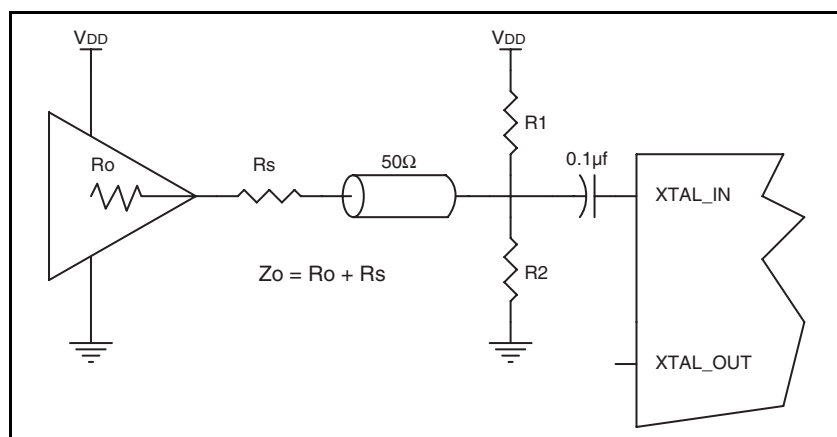


**Figure 2. Crystal Input Interface**

## LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.



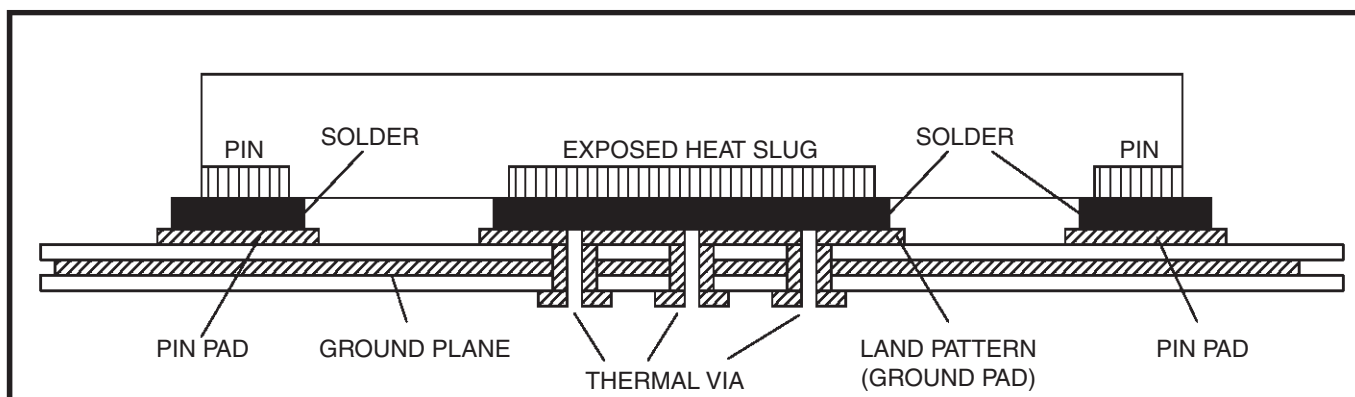
**Figure 3. General Diagram for LVC MOS Driver to XTAL Input Interface**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

### 3.3V M-LVDS Driver Termination

A general M-LVDS interface is shown in *Figure 5*. In a  $100\Omega$  differential transmission line environment, M-LVDS drivers require a matched load termination of  $100\Omega$  across near the receiver input.

For a multiple M-LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

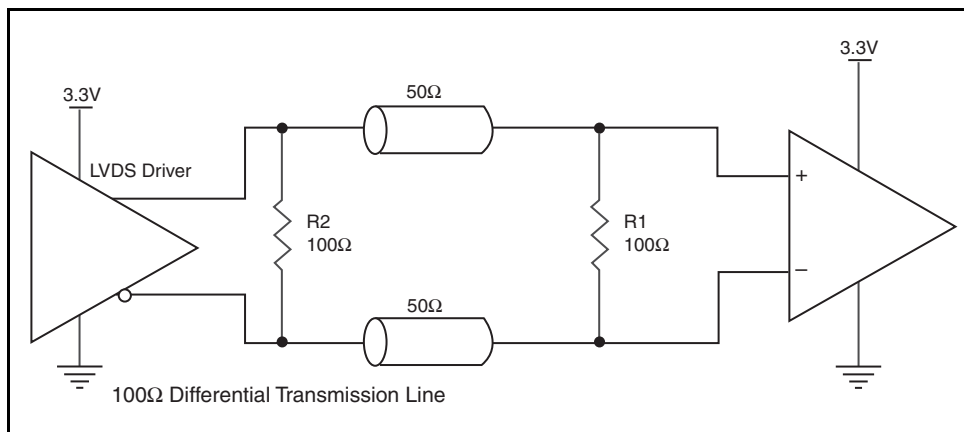


Figure 5. Typical M-LVDS Driver Termination

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 32Lead VFQFN

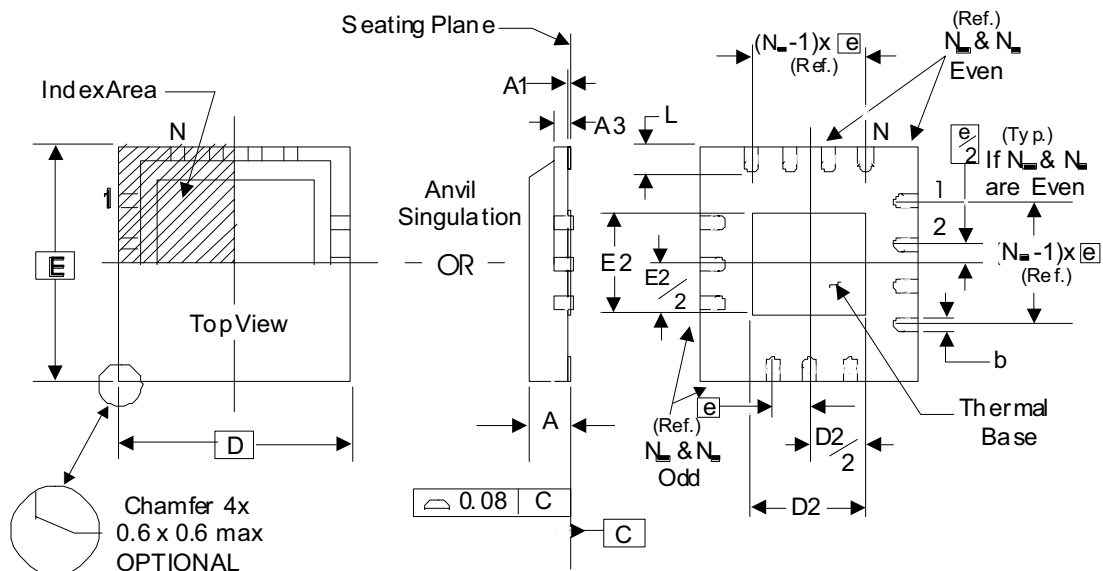
| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---------------------------------------------|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.4°C/W | 37.0°C/W | 33.2°C/W |

## Transistor Count

The transistor count for ICS845204 is: 3749

## Package Outline and Package Dimension

### Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout

of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

**Table 8. Package Dimensions**

| JEDEC Variation: VHHD-2/-4<br>All Dimensions in Millimeters |         |            |         |
|-------------------------------------------------------------|---------|------------|---------|
| Symbol                                                      | Minimum | Nominal    | Maximum |
| $N$                                                         |         | 32         |         |
| $A$                                                         | 0.80    |            | 1.00    |
| $A1$                                                        | 0       |            | 0.05    |
| $A3$                                                        |         | 0.25 Ref.  |         |
| $b$                                                         | 0.18    | 0.25       | 0.30    |
| $N_D$ & $N_E$                                               |         |            | 8       |
| $D$ & $E$                                                   |         | 5.00 Basic |         |
| $D2$ & $E2$                                                 | 3.0     |            | 3.3     |
| $e$                                                         |         | 0.50 Basic |         |
| $L$                                                         | 0.30    | 0.40       | 0.50    |

Reference Document: JEDEC Publication 95, MO-220

## Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking     | Package                   | Shipping Packaging | Temperature |
|-------------------|-------------|---------------------------|--------------------|-------------|
| 845204AK          | TBD         | 32 Lead VFQFN             | Tray               | 0°C to 70°C |
| 845204AKT         | TBD         | 32 Lead VFQFN             | 2500 Tape & Reel   | 0°C to 70°C |
| 845204AKLF        | ICS845204AL | "Lead-Free" 32 Lead VFQFN | Tray               | 0°C to 70°C |
| 845204AKLFT       | ICS845204AL | "Lead-Free" 32 Lead VFQFN | 2500 Tape & Reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

ICS845204

CRYSTAL-TO-MLVDS CLOCK SYNTHESIZER W/SPREAD SPECTRUM

ADVANCE INFORMATION

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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

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