

# N-Channel 150-V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
150	0.052 at $V_{GS} = 10$ V	25
	0.060 at $V_{GS} = 6$ V	23

## FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC

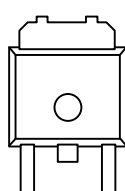


**RoHS**  
COMPLIANT

## APPLICATIONS

- Primary Side Switch

TO-252

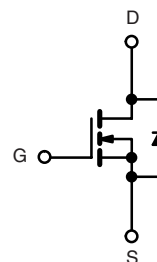


Top View

Drain Connected to Tab

### Ordering Information:

SUD25N15-52-E3 (Lead (Pb)- free)



N-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C) <sup>b</sup>	$I_D$	25	A
	$I_D$	14.5	
Pulsed Drain Current	$I_{DM}$	50	
Continuous Source Current (Diode Conduction)	$I_S$	25	
Avalanche Current	$I_{AR}$	25	mJ
Repetitive Avalanche Energy (Duty Cycle $\leq 1$ %)	$E_{AR}$	31	
Maximum Power Dissipation	$P_D$	136 <sup>b</sup>	W
	$P_D$	3 <sup>a</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	15	18	°C/W
	$R_{thJA}$	40	50	
Junction-to-Case (Drain)	$R_{thJC}$	0.85	1.1	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

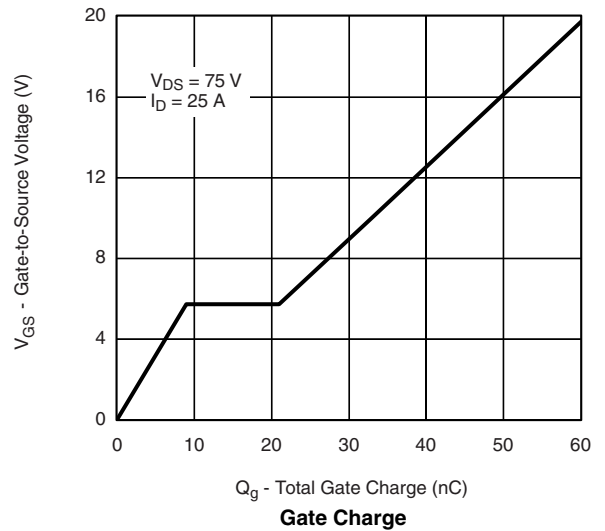
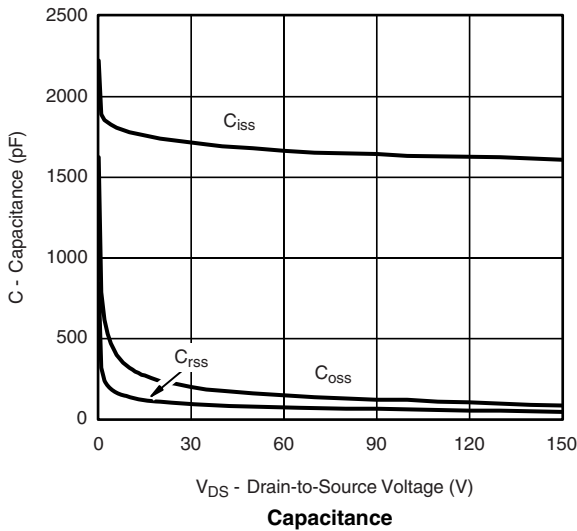
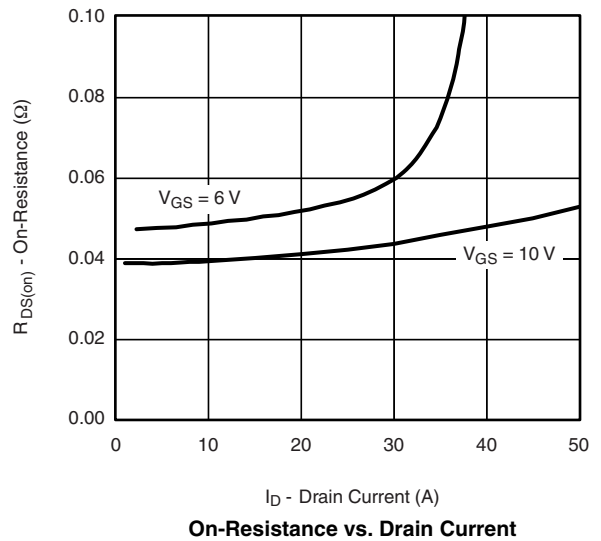
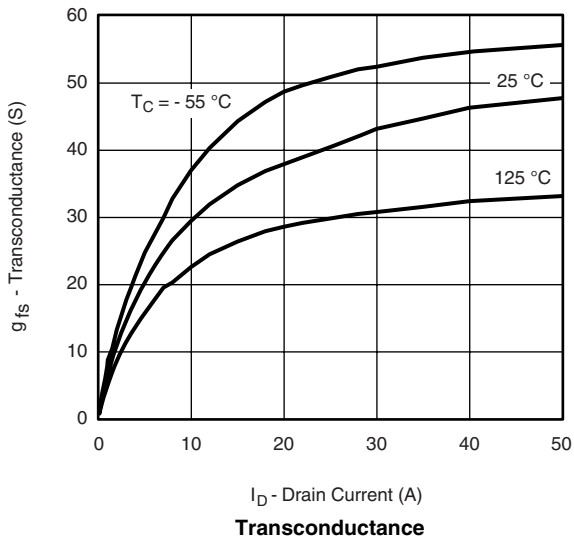
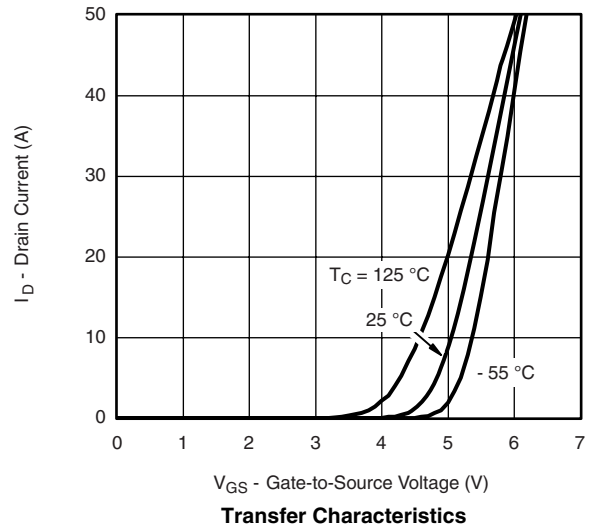
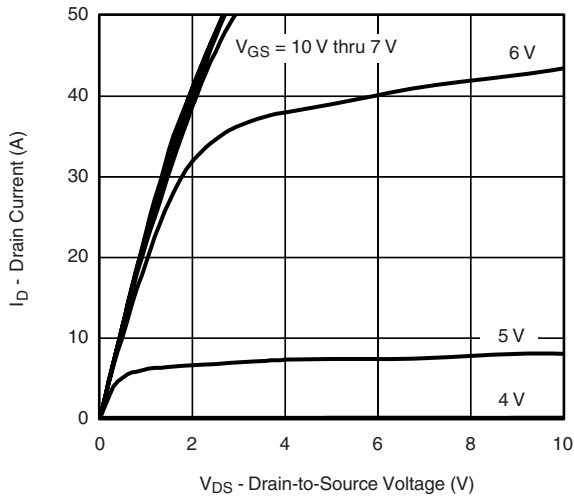
b. See SOA curve for voltage derating.

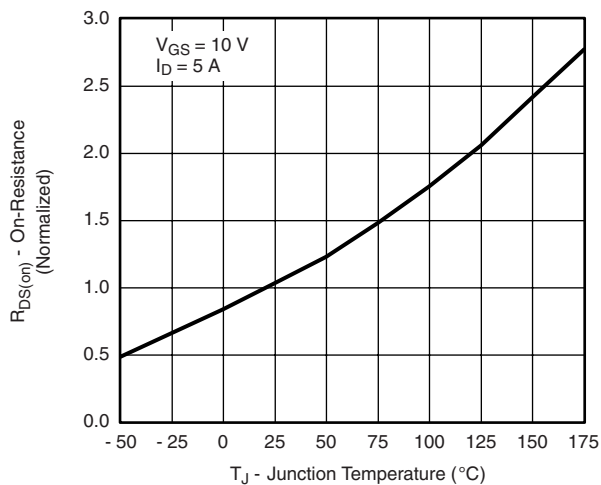
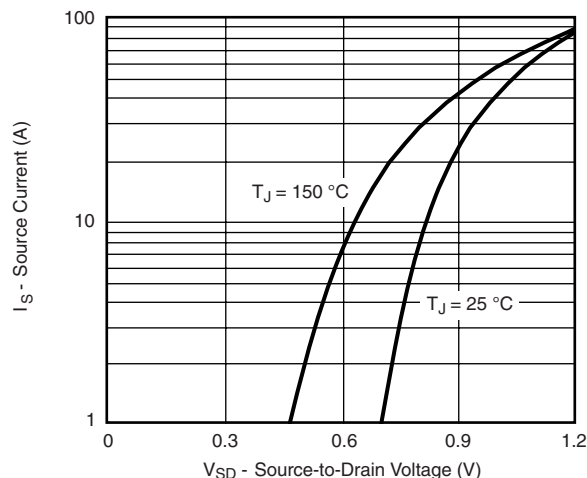
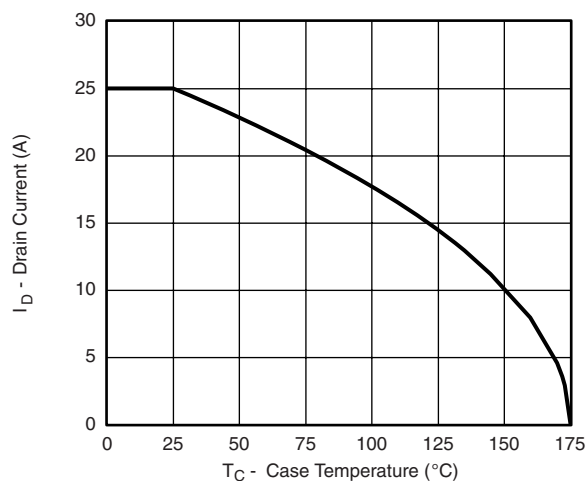
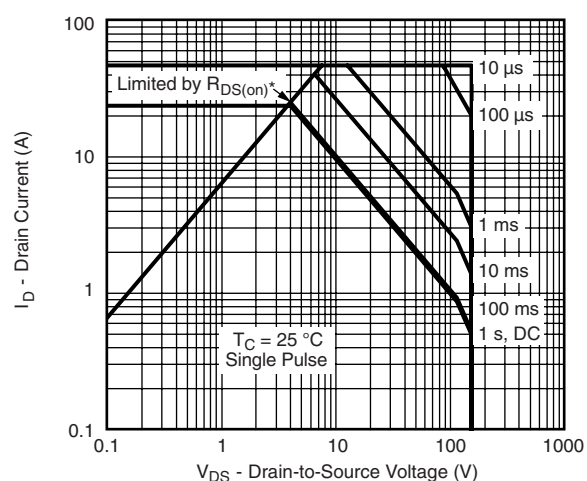
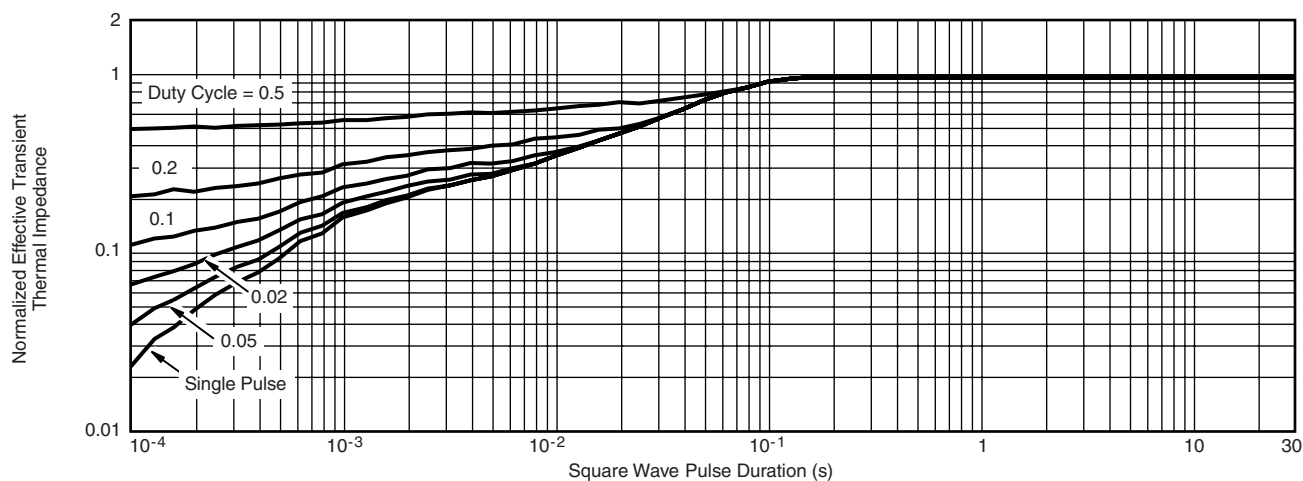
SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	150			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A		0.042	0.052	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 125 °C			0.109	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 175 °C			0.145	
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 5 A		0.047	0.060	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		40		S
Dynamic <sup>a</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		1725		pF
Output Capacitance	C <sub>oss</sub>			216		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		33	40	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			9		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			12		
Gate Resistance	R <sub>g</sub>		1		3	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 3 Ω I <sub>D</sub> ≅ 25 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		15	25	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			70	100	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			25	40	
Fall Time <sup>c</sup>	t <sub>f</sub>			60	90	
Source-Drain Diode Ratings and Characteristics T <sub>C</sub> = 25 °C						
Pulsed Current	I <sub>SM</sub>				50	A
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 25 A, dI/dt = 100 A/μs		95	140	ns

## Notes:

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

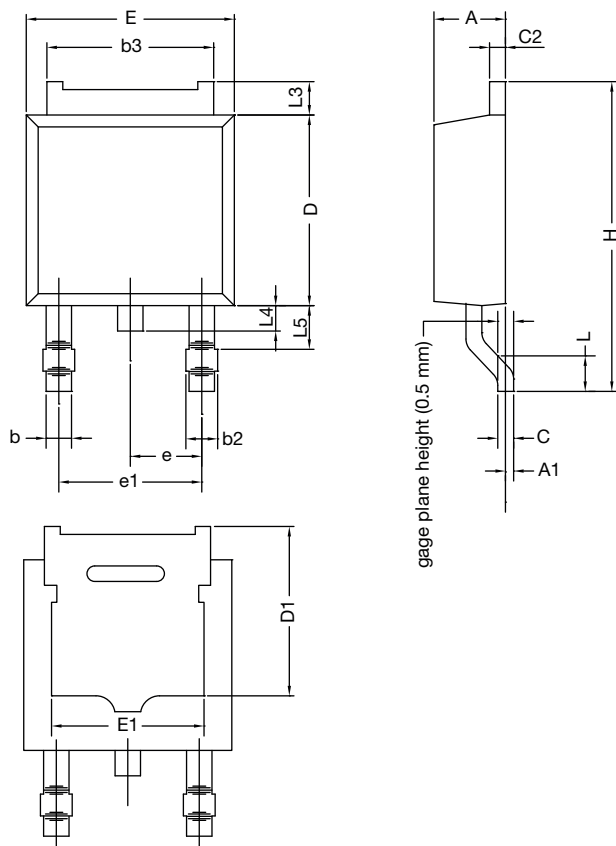
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****THERMAL RATINGS****Maximum Avalanche Drain Current vs. Case Temperature****Safe Operating Area**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified**Normalized Thermal Transient Impedance, Junction-to-Case**

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## TO-252AA Case Outline

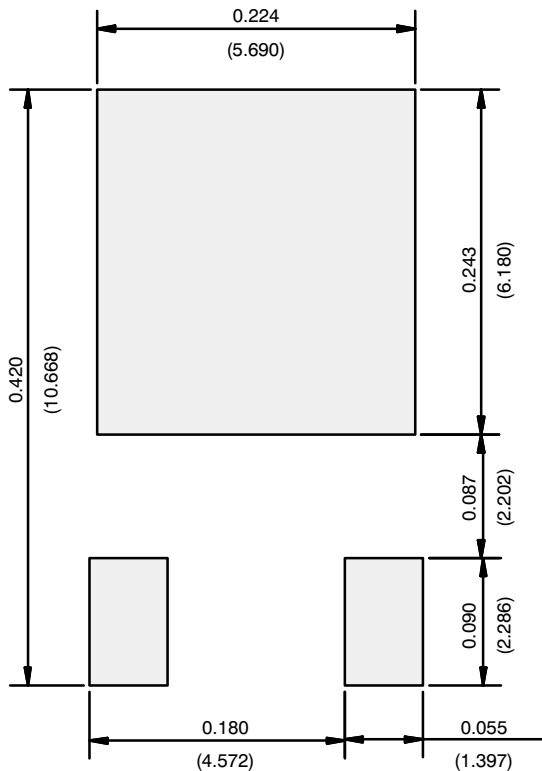


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

### Notes

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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