3 V/5 V, 2 MSPS, 8-Bit, 1-, 4-, 8-Channel Sampling ADCs

AD7822/AD7825/AD7829

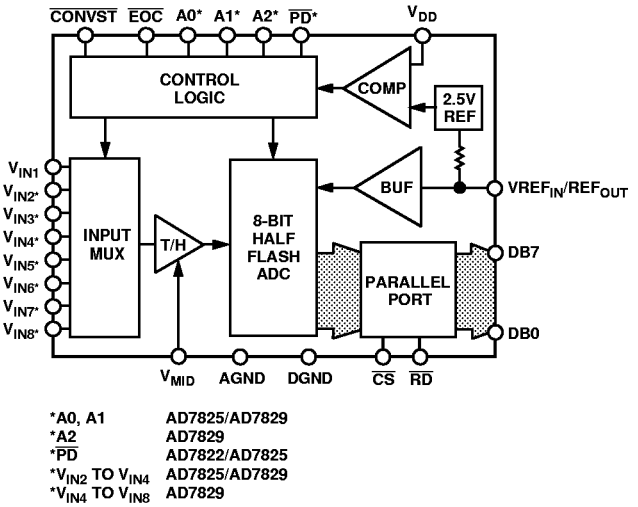
FEATURES

8-Bit Half-Flash ADC with 420 ns Conversion Time
1, 4 and 8 Single-Ended Analog Input Channels Available with Input Offset Adjust
On-Chip Track-and-Hold
SNR Performance Given for Input Frequencies Up to 10 MHz
On-Chip Reference (2.5 V)
Automatic Power-Down at the End of Conversion
Wide Operating Supply Range
3 V ± 10% and 5 V ± 10%
Input Ranges
0 V to 2 V p-p, V_{DD} = 3 V ± 10%
0 V to 2.5 V p-p, V_{DD} = 5 V ± 10%
Flexible Parallel Interface with EOC Pulse to Allow Stand-Alone Operation

APPLICATIONS

Data Acquisition Systems, DSP Front Ends
Disk Drives
Mobile Communication Systems, Subsampling Applications

FUNCTIONAL BLOCK DIAGRAM



*A0, A1 AD7825/AD7829
*A2 AD7829
*PD AD7822/AD7825
*V_{IN2} TO V_{IN4} AD7825/AD7829
*V_{IN4} TO V_{IN8} AD7829

GENERAL DESCRIPTION

The AD7822, AD7825, and AD7829 are high speed, 1-, 4-, and 8-channel, microprocessor-compatible, 8-bit analog-to-digital converters with a maximum throughput of 2 MSPS. The AD7822, AD7825, and AD7829 contain an on-chip reference of 2.5 V (2% tolerance), a track/hold amplifier, a 420 ns 8-bit half-flash ADC and a high speed parallel interface. The converters can operate from a single 3 V ± 10% and 5 V ± 10% supply.

The AD7822, AD7825, and AD7829 combine the convert start and power-down functions at one pin, i.e., the $\overline{\text{CONVST}}$ pin. This allows a unique automatic power-down at the end of a conversion to be implemented. The logic level on the $\overline{\text{CONVST}}$ pin is sampled after the end of a conversion when an $\overline{\text{EOC}}$ (End of Conversion) signal goes high, and if it is logic low at that point, the ADC is powered down. The AD7822 and AD7825 also have a separate power-down pin. (See Operating Modes section of the data sheet.)

The parallel interface is designed to allow easy interfacing to microprocessors and DSPs. Using only address decoding logic, the parts are easily mapped into the microprocessor address space. The $\overline{\text{EOC}}$ pulse allows the ADCs to be used in a stand-alone manner. (See Parallel Interface section of the data sheet.)

The AD7822 and AD7825 are available in a 20-/24-lead 0.3" wide, plastic dual-in-line package (DIP), a 20-/24-lead small outline IC (SOIC) and a 20-/24-lead thin shrink small outline package (TSSOP). The AD7829 is available in a 28-lead 0.6" wide, plastic dual-in-line package (DIP), a 28-lead small outline IC (SOIC) and in a 28-lead thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The AD7822, AD7825, and AD7829 have a conversion time of 420 ns. Faster conversion times maximize the DSP processing time in a real time system.
2. Analog Input Span Adjustment
   The V_{MID} pin allows the user to offset the input span. This feature can reduce the requirements of single supply op amps and take into account any system offsets.
3. FPBW (Full Power Bandwidth) of Track and Hold
   The track-and-hold amplifier has an excellent high frequency performance. The AD7822, AD7825, and AD7829 are capable of converting full-scale input signals up to a frequency of 10 MHz. This makes the parts ideally suited to subsampling applications.
4. Channel Selection
   Channel selection is made without the necessity of writing to the part.

REV. A

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AD7822/AD7825/AD7829—SPECIFICATIONS (V_{DD} = 3 V ± 10%, V_{DD} = 5 V ± 10%, GND = 0 V, $V_{REF\ IN/OUT}$ = 2.5 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	Version B	Unit	Test Condition/Comment
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz. f_{SAMPLE} = 2 MHz
Signal to (Noise + Distortion) Ratio[1]	48	dB min	
Total Harmonic Distortion[1]	–55	dB max	
Peak Harmonic or Spurious Noise[1]	–55	dB max	
Intermodulation Distortion[1]			fa = 27.3 kHz, fb = 28.3 kHz
2nd Order Terms	–65	dB typ	
3rd Order Terms	–65	dB typ	
Channel-to-Channel Isolation[1]	–70	dB typ	f_{IN} = 20 kHz
DC ACCURACY			
Resolution	8	Bits	
Minimum Resolution for Which			
No Missing Codes Are Guaranteed	8	Bits	
Integral Nonlinearity (INL)[1]	±0.75	LSB max	
Differential Nonlinearity (DNL)[1]	±0.75	LSB max	
Gain Error[1]	±2	LSB max	
Gain Error Match[1]	±0.1	LSB typ	
Offset Error[1]	±1	LSB max	
Offset Error Match[1]	±0.1	LSB typ	
ANALOG INPUTS[2]			See Analog Input Section
V_{DD} = 5 V ± 10%			Input Voltage Span = 2.5 V
V_{IN1} to V_{IN8} Input Voltage	V_{DD}	V max	
	0	V min	
V_{MID} Input Voltage	V_{DD} – 1.25	V max	Default V_{MID} = 1.25 V
	1.25	V min	
V_{DD} = 3 V ± 10%			Input Voltage Span = 2 V
V_{IN1} to V_{IN8} Input Voltage	V_{DD}	V max	
	0	V min	
V_{MID} Input Voltage	V_{DD} – 1	V max	Default V_{MID} = 1 V
	1	V min	
V_{IN} Input Leakage Current	±1	µA max	
V_{IN} Input Capacitance	15	pF max	
V_{MID} Input Impedance	6	kΩ typ	
REFERENCE INPUT			
$V_{REF\ IN/OUT}$ Input Voltage Range	2.55	V max	2.5 V + 2%
	2.45	V min	2.5 V – 2%
Input Current	1	µA typ	
	100	µA max	
ON-CHIP REFERENCE			Nominal 2.5 V
Reference Error	±50	mV max	
Temperature Coefficient	50	ppm/°C typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 10%
Input High Voltage, V_{INH}	2	V min	V_{DD} = 3 V ± 10%
Input Low Voltage, V_{INL}	0.4	V max	V_{DD} = 3 V ± 10%
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}			I_{SOURCE} = 200 µA
	4	V min	V_{DD} = 5 V ± 10%
	2.4	V min	V_{DD} = 3 V ± 10%
Output Low Voltage, V_{OL}			I_{SINK} = 200 µA
	0.4	V max	V_{DD} = 5 V ± 10%
	0.2	V max	V_{DD} = 3 V ± 10%
High Impedance Leakage Current	±1	µA max	
High Impedance Capacitance	10	pF max	

Parameter	Version B	Unit	Test Condition/Comment
CONVERSION RATE			
Track/Hold Acquisition Time	200	ns max	See Functional Description Section
Conversion Time	420	ns max	
POWER SUPPLY REJECTION			
V_{DD} ± 10%	±1	LSB max	
POWER REQUIREMENTS			
V_{DD}	4.5	V min	5 V ± 10%. For Specified Performance
	5.5	V max	
V_{DD}	2.7	V min	3 V ± 10%. For Specified Performance
	3.3	V max	
I_{DD}			
Normal Operation	12	mA max	8 mA Typically
Power-Down	5	µA max	Logic Inputs = 0 V or V_{DD}
	0.2	µA typ	
Power Dissipation			V_{DD} = 3 V
Normal Operation	36	mW max	Typically 24 mW
Power-Down			
200 kSPS	9.58	mW max	
1 MSPS	47.88	mW max	

NOTES
[1]See Terminology section of this data sheet.
[2]Refer to the Analog Input section for an explanation of the Analog Input(s).
Specifications subject to change without notice.

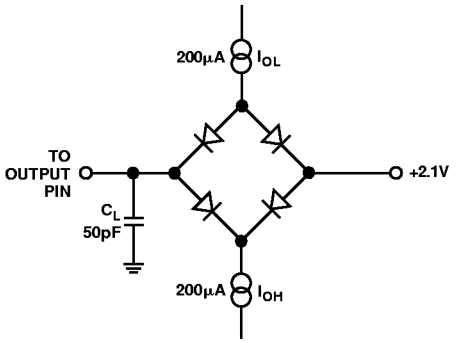


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ORDERING GUIDE

Model	Linearity Error	Package Description	Package Option
AD7822BN	±0.75 LSB	Plastic DIP	N-20
AD7822BR	±0.75 LSB	Small Outline IC	R-20
AD7822BRU	±0.75 LSB	Thin Shrink Small Outline (TSSOP)	RU-20
AD7825BN	±0.75 LSB	Plastic DIP	N-24
AD7825BR	±0.75 LSB	Small Outline IC	R-24
AD7825BRU	±0.75 LSB	Thin Shrink Small Outline (TSSOP)	RU-24
AD7829BN	±0.75 LSB	Plastic DIP	N-28
AD7829BR	±0.75 LSB	Small Outline IC	R-28
AD7829BRU	±0.75 LSB	Thin Shrink Small Outline (TSSOP)	RU-28

TIMING CHARACTERISTICS[1, 2] ($V_{REF\ IN/OUT}$ = 2.5 V. All specifications –40°C to +85°C unless otherwise noted)

Parameter	5 V ± 10%	3 V ± 10%	Unit	Conditions/Comments
t_1	420	420	ns max	Conversion Time.
t_2	20	20	ns min	Minimum $\overline{CONVST}$ Pulsewidth.
t_3	30	30	ns min	Minimum time between the rising edge of $\overline{RD}$ and next falling edge of convert start.
t_4	110	110	ns max	$\overline{EOC}$ Pulsewidth.
	70	70	ns min	
t_5	10	10	ns max	$\overline{RD}$ rising edge to $\overline{EOC}$ pulse high.
t_6	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time.
t_7	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time.
t_8	30	30	ns min	Minimum $\overline{RD}$ Pulsewidth.
t_9[3]	10	20	ns max	Data access time after $\overline{RD}$ low.
t_{10}[4]	5	5	ns min	Bus relinquish time after $\overline{RD}$ high.
	20	20	ns max	
t_{11}	10	10	ns min	Address setup time before falling edge of $\overline{RD}$.
t_{12}	15	15	ns min	Address hold time after falling edge of $\overline{RD}$.
t_{13}	200	200	ns min	Minimum time between new channel selection and convert start.
$t_{POWER\ UP}$	25	25	µs typ	Power-up time from rising edge of $\overline{CONVST}$ using on-chip reference.
$t_{POWER\ UP}$	1	1	µs max	Power-up time from rising edge of $\overline{CONVST}$ using external 2.5 V reference.

NOTES

[1]Sample tested to ensure compliance.

[2]See Figures 20, 21 and 22.

[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V with V_{DD} = 5 V ± 10%, and time required for an output to cross 0.4 V or 2.0 V with V_{DD} = 3 V ± 10%.

[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measurednumber is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{10}, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
  V_{IN1} to V_{IN8} ..... –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to AGND ... –0.3 V to V_{DD} + 0.3 V
V_{MID} Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature, (Soldering, 10 sec) ..... 260°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... 215°C
    Infrared (15 sec) ..... 220°C
TSSOP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 128°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... 215°C
    Infrared (15 sec) ..... 220°C
ESD ..... 1 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

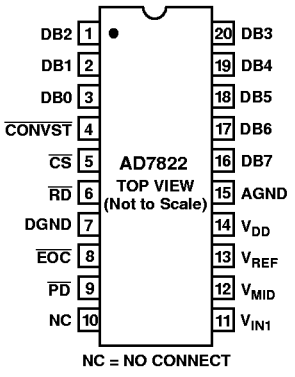
CAUTION

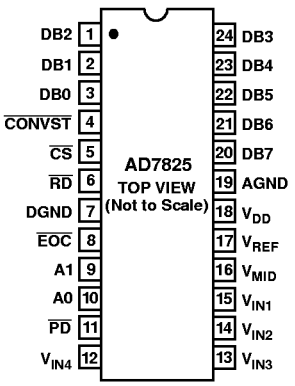
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7822/AD7825/AD7829 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

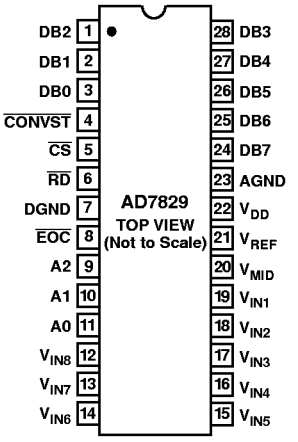
PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
V_{IN1} to V_{IN8}	Analog Input Channels. The AD7822 has a single input channel; the AD7825 and AD7829 have four and eight analog input channels respectively. The inputs have an input span of 2.5 V and 2 V depending on the supply voltage (V_{DD}). This span may be centered anywhere in the range AGND to V_{DD} using the V_{MID} Pin. The default input range (V_{MID} unconnected) is AGND to 2 V (V_{DD} = 3 V ± 10%) or AGND to 2.5 V (V_{DD} = 5 V ± 10%). See Analog Input section of the data sheet for more information.
V_{DD}	Positive supply voltage, 3 V ± 10% and 5 V ± 10%.
AGND	Analog Ground. Ground reference for track/hold, comparators, reference circuit and multiplexer.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{CONVST}$	Logic Input Signal. The convert start signal initiates an 8-bit analog-to-digital conversion on the falling edge of this signal. The falling edge of this signal places the track/hold in hold mode. The track/hold goes into track mode again 120 ns after the start of a conversion. The state of the $\overline{CONVST}$ signal is checked at the end of a conversion. If it is logic low, the AD7822/AD7825/AD7829 will power down. (See Operating Mode section of the data sheet.)
$\overline{EOC}$	Logic Output. The End of Conversion signal indicates when a conversion has finished. The signal can be used to interrupt a microcontroller when a conversion has finished or latch data into a gate array. (See Parallel Interface section of this data sheet.)
$\overline{CS}$	Logic input signal. The chip select signal is used to enable the parallel port of the AD7822, AD7825, and AD7829. This is necessary if the ADC is sharing a common data bus with another device.
$\overline{PD}$	Logic Input. The Power-Down pin is present on the AD7822 and AD7825 only. Bringing the $\overline{PD}$ pin low places the AD7822 and AD7825 in Power-Down mode. The ADCs will power-up when $\overline{PD}$ is brought logic high again.
$\overline{RD}$	Logic Input Signal. The read signal is used to take the output buffers out of their high impedance state and drive data onto the data bus. The signal is internally gated with the $\overline{CS}$ signal. Both $\overline{RD}$ and $\overline{CS}$ must be logic low to enable the data bus.
A0–A2	Channel Address Inputs. The address of the next multiplexer channel must be present on these inputs when the $\overline{RD}$ signal goes low.
DB0–DB7	Data Output Lines. They are normally held in a high impedance state. Data is driven onto the data bus when both $\overline{RD}$ and $\overline{CS}$ go active low.
$V_{REF\ IN/OUT}$	Analog Input and Output. An external reference can be connected to the AD7822, AD7825, and AD7829 at this pin. The on-chip reference is also available at this pin.

PIN CONFIGURATIONS
DIP/SOIC/TSSOP







TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus, for an 8-bit converter, this is 50 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7822/AD7825/AD7829 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7822/AD7825/AD7829 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 20 kHz sine wave signal to one input channel and determining how much that signal is attenuated in each of the other channels. The figure given is the worst case across all four or eight channels of the AD7825 and AD7829 respectively.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the 128th code transition (01111111) to (10000000) from the ideal, i.e., V_{MID}.

Offset Error Match
The difference in offset error between any two channels.

Zero-Scale Error
The deviation of the first code transition (00000000) to (00000001) from the ideal, i.e., V_{MID} – 1.25 V + 1 LSB (V_{DD} = 5 V ± 10%), or V_{MID} – 1.0 V + 1 LSB (V_{DD} = 3 V ± 10%).

Full-Scale Error
The deviation of the last code transition (11111110) to (11111111) from the ideal, i.e., V_{MID} + 1.25 V – 1 LSB (V_{DD} = 5 V ± 10%), or V_{MID} + 1.0 V – 1 LSB (V_{DD} = 3 V ± 10%).

Gain Error
The deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal, i.e., V_{REF} – 1 LSB, after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

Track/Hold Acquisition Time
The time required for the output of the track/hold amplifier to reach its final value, within ± 1/2 LSB, after the point at which the track/hold returns to track mode. This happens approximately 120 ns after the falling edge of $\overline{\text{CONVST}}$.

It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7822/AD7825/AD7829. It means that the user must wait for the duration of the track/hold acquisition time after a channel change/step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

PSR (Power Supply Rejection)
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

CIRCUIT DESCRIPTION

The AD7822, AD7825, and AD7829 consist of a track-and-hold amplifier followed by a half-flash analog-to-digital converter. These devices use a half-flash conversion technique where one 4-bit flash ADC is used to achieve an 8-bit result. The 4-bit flash ADC contains a sampling capacitor followed by fifteen comparators that compare the unknown input to a reference ladder to achieve a 4-bit result. This first flash, i.e., coarse conversion, provides the 4 MSBs. For a full 8-bit reading to be realized, a second flash, i.e., a fine conversion, must be performed to provide the 4 LSBs. The 8-bit word is then placed on the data output bus.

Figures 2 and 3 below show simplified schematics of the ADC. When the ADC starts a conversion, the track and hold goes into hold mode and holds the analog input for 120 ns. This is the acquisition phase as shown in Figure 2, when Switch 2 is in Position A. At the point when the track and hold returns to its track mode, this signal is sampled by the sampling capacitor as Switch 2 moves into Position B. The first flash occurs at this instant and is then followed by the second flash. Typically, the first flash is complete after 100 ns, i.e., at 220 ns, while the end of the second flash and hence the 8-bit conversion result is available at 330 ns. As shown in Figure 4, the track-and-hold returns to track mode after 120 ns, and starts the next acquisition before the end of the current conversion. Figure 6 shows the ADC transfer function.

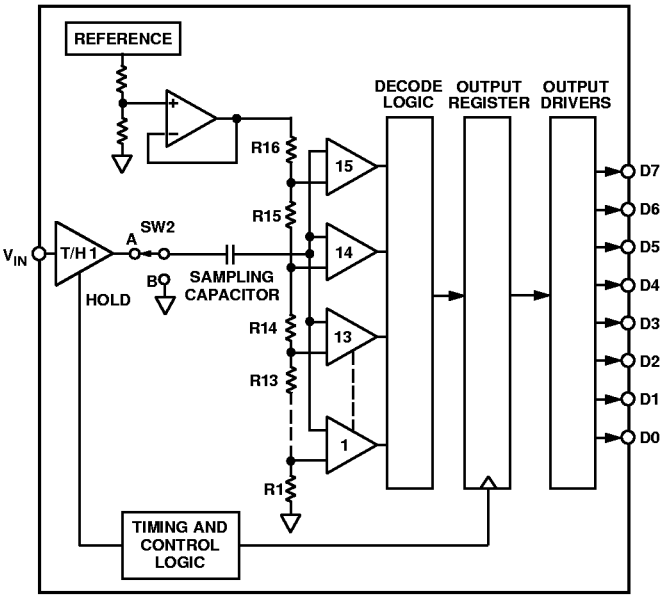


Figure 2. ADC Acquisition Phase

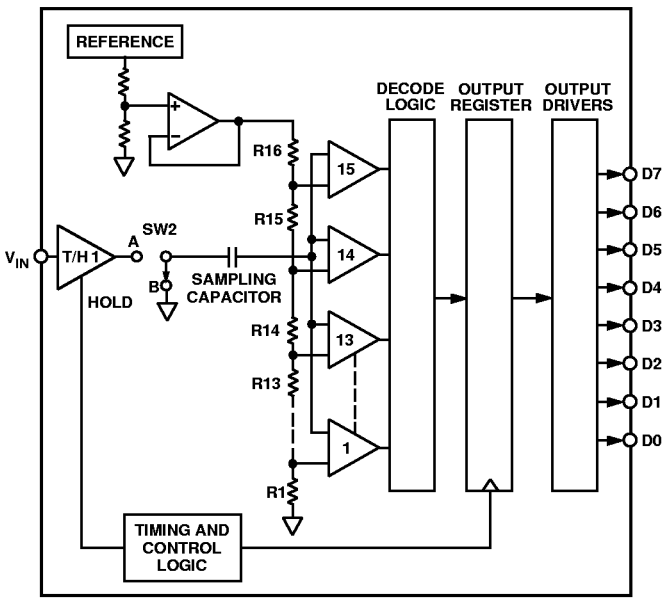


Figure 3. ADC Conversion Phase

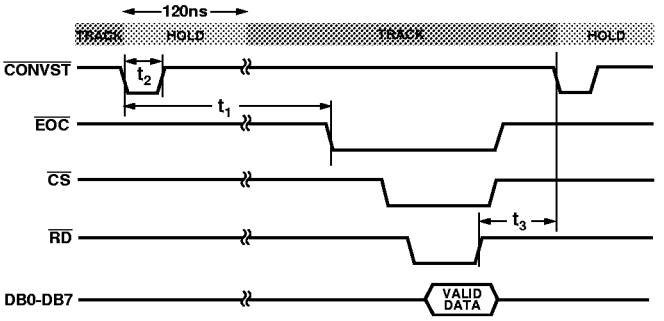


Figure 4. Track-and-Hold Timing

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7822, AD7825, and AD7829. The AGND and DGND are connected together at the device for good noise suppression. The parallel interface is implemented using an 8-bit data bus. The end of conversion signal ($\overline{EOC}$) idles high, the falling edge of $\overline{CONVST}$ initiates a conversion and at the end of conversion the falling edge of $\overline{EOC}$ is used to initiate an Interrupt Service Routine (ISR) on a microprocessor. (See Parallel interface section for more details.) V_{REF} and V_{MID} are connected to voltage source such as the AD780, while V_{DD} is connected to a voltage source that can vary from 4.5 V to 5.5 V. (See Table I in Analog Input section.) When V_{DD} is first connected, the AD7822, AD7825, and AD7829 power up in a low current mode, i.e., power-down, with the default logic level on the $\overline{EOC}$ pin on the AD7822 and AD7825 equal to a low. Ensure the $\overline{CONVST}$ line is not floating when V_{DD} is applied, as this could put the AD7822/AD7825/AD7829 into an unknown state. A rising edge on the $\overline{CONVST}$ pin will cause the AD7829 to fully power up while a rising edge on the $\overline{PD}$ pin will cause the AD7822 and AD7825 to fully power up. For applications where power consumption is of concern, the automatic power-down at the end of a conversion should be used to improve power performance. (See Power-Down Options section of the data sheet.)

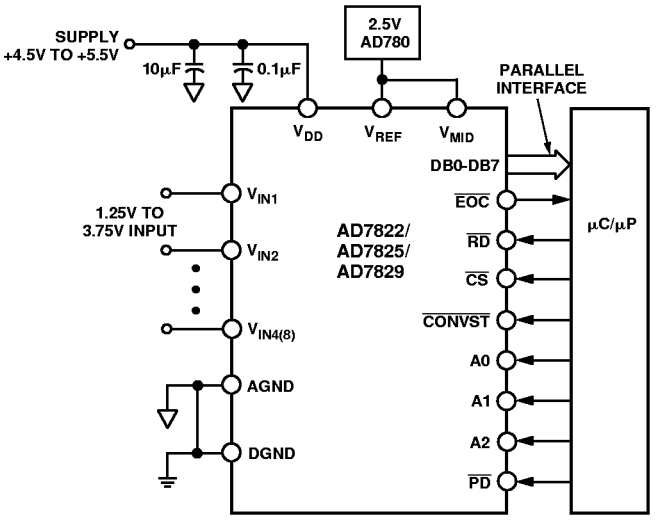


Figure 5. Typical Connection Diagram

ADC TRANSFER FUNCTION

The output coding of the AD7822, AD7825, and AD7829 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = $V_{REF}/256$ (V_{DD} = 5 V) or the LSB size = (0.8 V_{REF})/256 (V_{DD} = 3 V). The ideal transfer characteristic for the AD7822, AD7825, and AD7829 is shown in Figure 6, below.

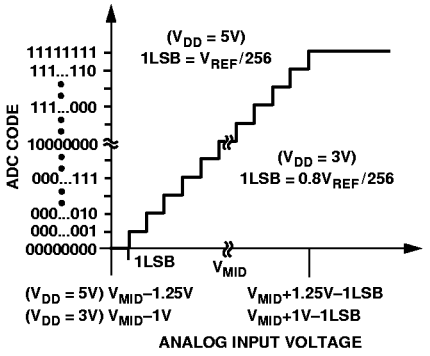


Figure 6. Transfer Characteristic

ANALOG INPUT

The AD7822 has a single input channel and the AD7825 and AD7829 have four and eight input channels respectively. Each input channel has an input span of 2.5 V or 2.0 V, depending on the supply voltage (V_{DD}). This input span is automatically set up by an on-chip "V_{DD} Detector" circuit. 5 V operation of the ADCs is detected when V_{DD} exceeds 4.1 V and 3 V operation is detected when V_{DD} falls below 3.8 V. This circuit also possesses a degree of glitch rejection; for example, a glitch from 5.5 V to 2.7 V up to 60 ns wide will not trip the V_{DD} detector.

The V_{MID} pin is used to center this input span anywhere in the range AGND to V_{DD}. If no input voltage is applied to V_{MID}, i.e., if V_{MID} is left unconnected, the default input range is AGND to 2.0 V (V_{DD} = 3 V ± 10%) i.e., centered about 1.0 V, or AGND to 2.5 V (V_{DD} = 5 V ± 10%) i.e., centered about 1.25 V.

If, however, an external V_{MID} is applied, the analog input range will be from V_{MID} – 1.0 V to V_{MID} + 1.0 V (V_{DD} = 3 V ± 10%), or from V_{MID} – 1.25 V to V_{MID} + 1.25 V (V_{DD} = 5 V ± 10%).

The range of values of V_{MID} that can be applied depends on the value of V_{DD}. For V_{DD} = 3 V ± 10%, the range of values that can be applied to V_{MID} is from 1.0 V to V_{DD} – 1.0 V and is 1.25 V to V_{DD} – 1.25 V when V_{DD}= 5 V ± 10%. Table I shows the relevant ranges of V_{MID} and the input span for various values of V_{DD}. Figure 7 illustrates the input signal range available with various values of V_{MID}.

Table I.

V_{DD}	V_{MID} Internal	V_{MID} Ext Max	V_{IN} Span	V_{MID} Ext Min	V_{IN} Span
5.5	1.25	4.25	3.0 to 5.5	1.25	0 to 2.5
5.0	1.25	3.75	2.5 to 5.0	1.25	0 to 2.5
4.5	1.25	3.25	2.0 to 4.5	1.25	0 to 2.5
3.3	1.00	2.3	1.3 to 3.3	1.00	0 to 2.0
3.0	1.00	2.0	1.0 to 3.0	1.00	0 to 2.0
2.7	1.00	1.7	0.7 to 2.7	1.00	0 to 2.0

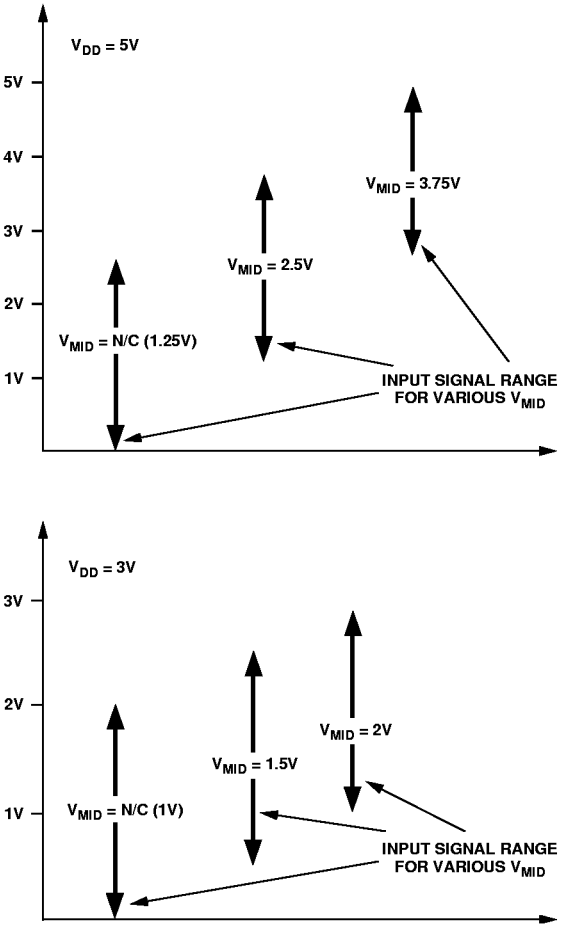


Figure 7. Analog Input Span Variation with V_{MID}

V_{MID} may be used to remove offsets in a system by applying the offset to the V_{MID} pin as shown in Figure 8, or it may be used to accommodate bipolar signals by applying V_{MID} to a level-shifting circuit before V_{IN}, as shown in Figure 9. When V_{MID} is being driven by an external source, the source may be directly tied to the level-shifting circuitry, see Figure 9; however, if the internal V_{MID}, i.e., the default value, is being used as an output, it must be buffered before applying it to the level-shifting circuitry as the V_{MID} pin has an impedance of approximately 6 kΩ, see Figure 10.

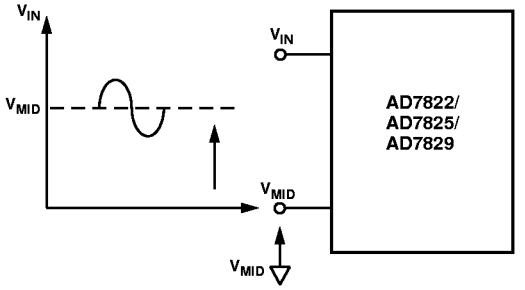


Figure 8. Removing Offsets Using V_{MID}

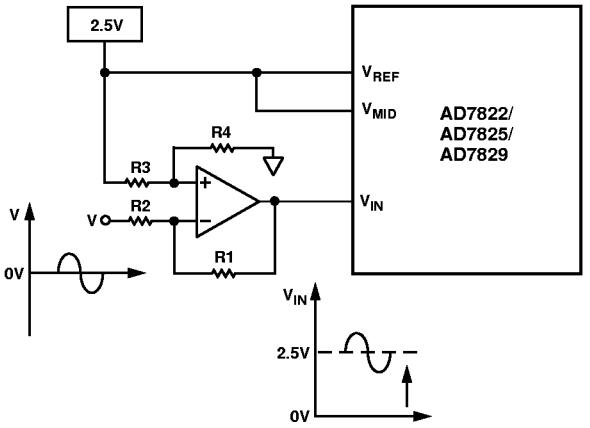


Figure 9. Accommodating Bipolar Signals Using External V_{MID}

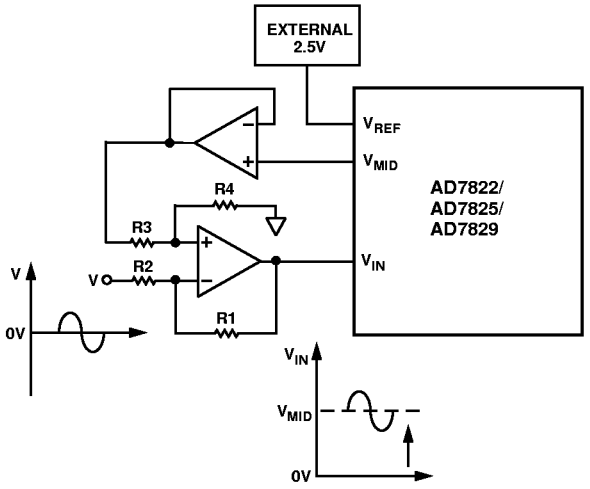


Figure 10. Accommodating Bipolar Signals Using Internal V_{MID}

NOTE: Although there is a V_{REF} pin from which a voltage reference of 2.5 V may be sourced, or to which an external reference may be applied, this does not provide an option of varying the value of the voltage reference. As stated in the specifications for the AD7822, AD7825, and AD7829, the input voltage range at this pin is 2.5 V ± 2%.

Analog Input Structure

Figure 11 shows an equivalent circuit of the analog input structure of the AD7822, AD7825, and the AD7829. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 20 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. However, it is worth noting that a small amount of current (1 mA) being conducted into the substrate due to an over voltage on an unselected channel, can cause inaccurate conversions on a selected channel. The capacitor C2 in Figure 11 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor, R1, is a lumped component made up of the on resistance of several components, including that of the multiplexer and the track and hold. This resistor is typically about 310 Ω. The capacitor C1 is the track-and-hold capacitor and has a capacitance of 0.5 pF. Switch 1 is the track-and-hold switch, while Switch 2 is that of the sampling capacitor as shown in Figures 2 and 3.

When in track phase, Switch 1 is closed and Switch 2 is in Position A; when in hold mode, Switch 1 opens while Switch 2 remains in Position A. The track-and-hold remains in hold mode for 120 ns—see Circuit Description, after which it returns to track mode and the ADC enters its conversion phase. At this point Switch 1 opens and Switch 2 moves to Position B. At the end of the conversion Switch 2 moves back to Position A.

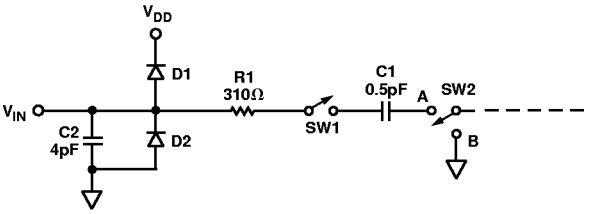


Figure 11. Equivalent Analog Input Circuit

Analog Input Selection

On power-up, the default V_{IN} selection is V_{IN1}. When returning to normal operation from power-down, the V_{IN} selected will be the same one that was selected prior to power-down being initiated. Table II below shows the multiplexer address corresponding to each analog input from V_{IN1} to $V_{IN4(8)}$ for the AD7825 or AD7829.

Table II.

A2	A1	A0	Analog Input Selected
0	0	0	V_{IN1}
0	0	1	V_{IN2}
0	1	0	V_{IN3}
0	1	1	V_{IN4}
1	0	0	V_{IN5}
1	0	1	V_{IN6}
1	1	0	V_{IN7}
1	1	1	V_{IN8}

Channel selection on the AD7825 and AD7829 is made without the necessity of a write operation. The address of the *next* channel to be converted is latched at the start of the *current* read operation, as shown in Figure 12. This allows for improved throughput rates in "channel hopping" applications.

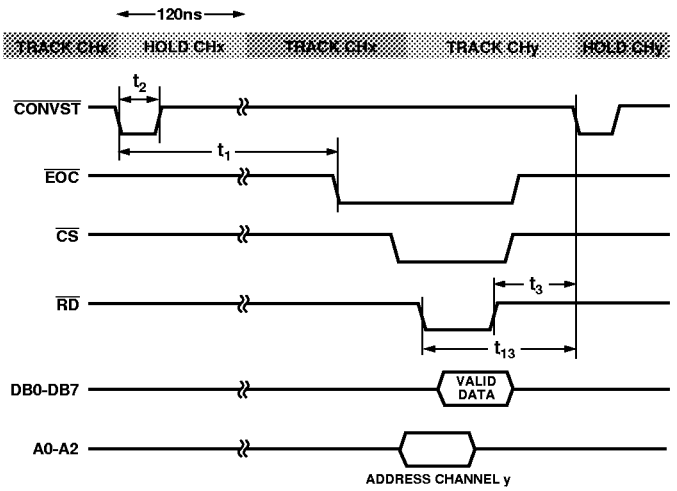


Figure 12. Channel Hopping Timing

There is a minimum time delay between the falling edge of $\overline{RD}$ and the next falling edge of the $\overline{CONVST}$ signal, t_{13}. This is the minimum acquisition time required of the track-and-hold in order to maintain 8-bit performance. Figure 13 shows the typical performance of the AD7825 when channel hopping for various acquisition times. These results were obtained using an external reference and internal V_{MID} while channel hopping between V_{IN1} and V_{IN4} with 0 V on Channel 4 and 0.5 V on Channel 1.

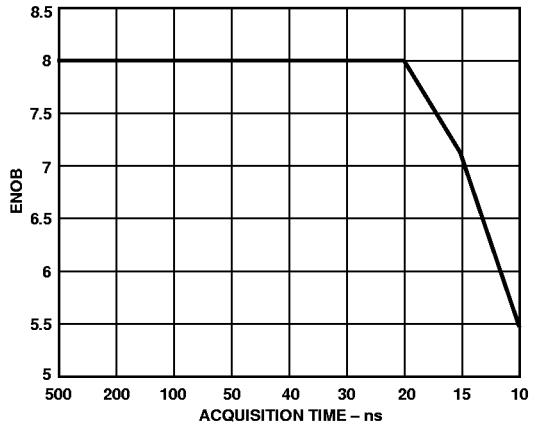


Figure 13. Effective Number of Bits vs. Acquisition Time for the AD7825

The on-chip track-and-hold can accommodate input frequencies to 10 MHz, making the AD7822, AD7825, and AD7829 ideal for subsampling applications. When the AD7825 is converting a 10 MHz input signal at a sampling rate of 2 MSPS, the effective number of bits typically remains above seven, corresponding to a signal-to-noise ratio of 42 dBs as shown in Figure 14.

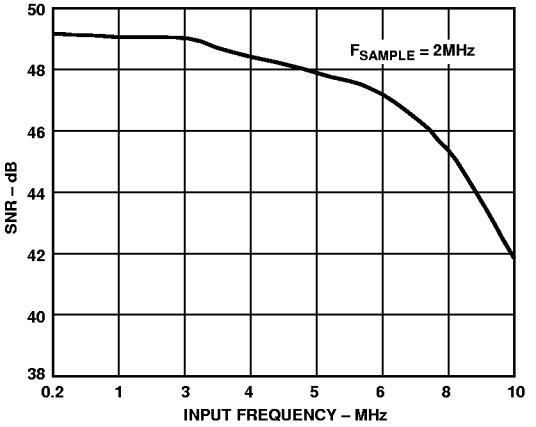


Figure 14. SNR vs. Input Frequency on the AD7825

POWER-UP TIMES

The AD7822/AD7825/AD7829 have a 1 µs power-up time when using an external reference and a 25 µs power-up time when using the on-chip reference. When V_{DD} is first connected, the AD7822, AD7825, and AD7829 are in a low current mode of operation. Ensure that the $\overline{CONVST}$ line is not floating when V_{DD} is applied, as this could put the AD7822/AD7825/AD7829 into an unknown state. In order to carry out a conversion the AD7822, AD7825, and AD7829 must first be powered up. The AD7829 is powered up by a rising edge on the $\overline{CONVST}$ pin and a conversion is initiated on the falling edge of $\overline{CONVST}$. Figure 15 shows how to power up the AD7829 when V_{DD} is first connected or after the AD7829 has been powered down using the $\overline{CONVST}$ pin when using either the on-chip, or an external, reference. When using an external reference, the falling edge of $\overline{CONVST}$ may occur before the required power-up time has elapsed; however, the conversion will not be initiated on the falling edge of $\overline{CONVST}$ but rather at the moment when the part has completely powered up, i.e., after 1 µs. If the falling edge of $\overline{CONVST}$ occurs after the required power-up time has elapsed, then it is upon this falling edge that a conversion is initiated. When using the on-chip reference, it is necessary to wait the required power-up time of approximately 25 µs before initiating a conversion; i.e., a falling edge on $\overline{CONVST}$ may not occur before the required power-up time has elapsed, when V_{DD} is first connected or after the AD7829 has been powered down using the $\overline{CONVST}$ pin as shown in Figure 15.

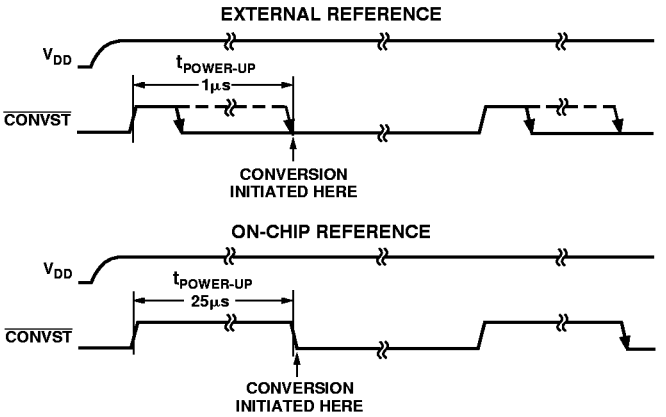


Figure 15. AD7829 Power-Up Time

Figure 16 shows how to power up the AD7822 or AD7825 when V_{DD} is first connected or after the ADCs have been powered down using the $\overline{PD}$ pin, or the $\overline{CONVST}$ pin, with either the on-chip or an external reference. When the supplies are first connected or after the part has been powered down by the $\overline{PD}$ pin, only a rising edge on the $\overline{PD}$ pin will cause the part to power up. When the part has been powered down using the $\overline{CONVST}$ pin, a rising edge on either the $\overline{PD}$ pin or the $\overline{CONVST}$ pin will power the part up again.

As with the AD7829, when using an external reference with the AD7822 or AD7825, the falling edge of $\overline{CONVST}$ may occur before the required power-up time has elapsed, however, if this is the case, the conversion will not be initiated on the falling edge of $\overline{CONVST}$, but rather at the moment when the part has powered up completely, i.e., after 1 µs. If the falling edge of $\overline{CONVST}$ occurs after the required power-up time has elapsed, it is upon this falling edge that a conversion is initiated. When using the on-chip reference it is necessary to wait the required power-up time of approximately 25 µs before initiating a conversion; i.e., a falling edge on $\overline{CONVST}$ may not occur before the required power-up time has elapsed, when supplies are first connected to the AD7822 or AD7825, or when the ADCs have been powered down using the PD pin or the $\overline{CONVST}$ pin as shown in Figure 16.

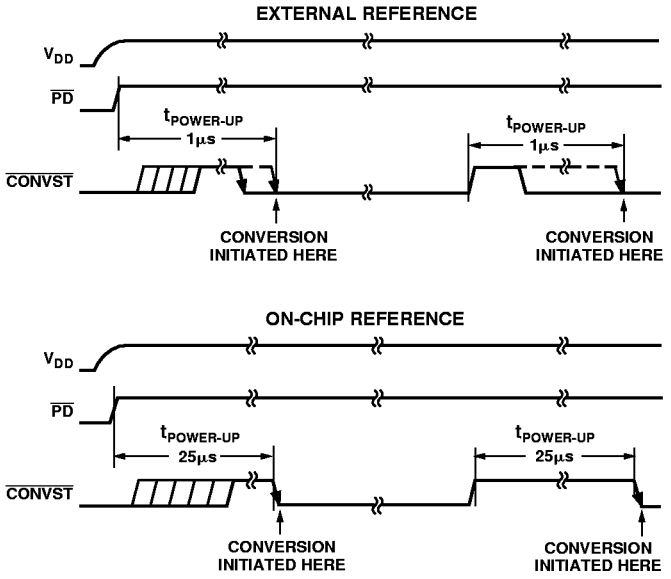


Figure 16. AD7822/AD7825 Power-Up Time

POWER VS. THROUGHPUT

Superior power performance can be achieved by using the automatic power-down (Mode 2) at the end of a conversion—see Operating Modes section of the data sheet.

Figure 17 shows how the automatic power-down is implemented using the $\overline{CONVST}$ signal to achieve the optimum power performance for the AD7822, AD7825, and AD7829. The duration of the $\overline{CONVST}$ pulse is set to be equal to or less than the power-up time of the devices—see Operating Modes section. As the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

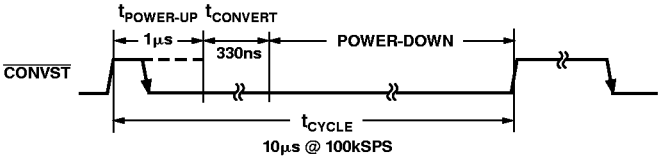


Figure 17. Automatic Power-Down

For example, if the AD7822 is operated in a continuous sampling mode, with a throughput rate of 100 kSPS and using an external reference, the power consumption is calculated as follows. The power dissipation during normal operation is 36 mW, V_{DD} = 3 V. If the power-up time is 1 µs and the conversion time is 330 ns (@ +25°C), the AD7822 can be said to dissipate 36 mW for 1.33 µs (worst case) during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (1.33/10) × (36 mW) = 4.79 mW.

Figure 18 shows the power vs. throughput rate for automatic full power-down.

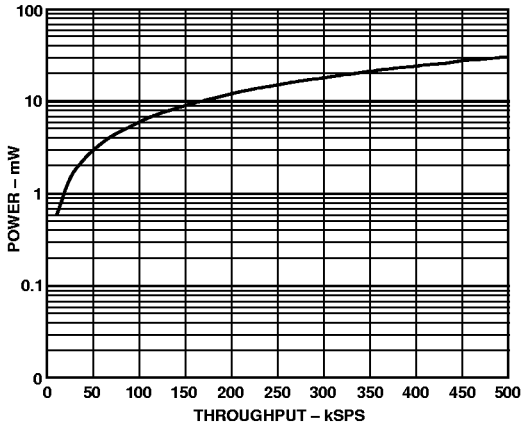


Figure 18. AD7822/AD7825/AD7829 Power vs. Throughput

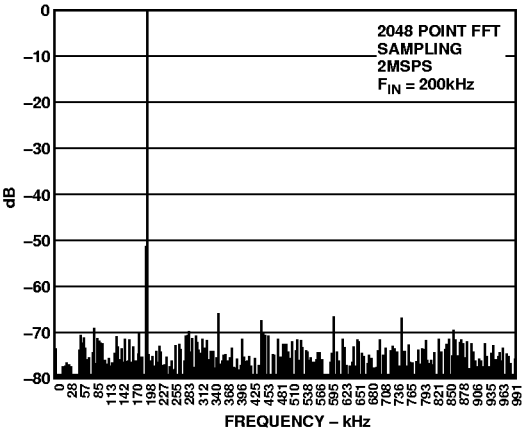


Figure 19. AD7822/AD7825/AD7829 SNR

OPERATING MODES

The AD7822, AD7825, and AD7829 have two possible modes of operation, depending on the state of the $\overline{\text{CONVST}}$ pulse approximately 100 ns after the end of a conversion, i.e., upon the rising edge of the $\overline{\text{EOC}}$ pulse.

Mode 1 Operation (High Speed Sampling)

When the AD7822, AD7825, and AD7829 are operated in Mode 1 they are not powered-down between conversions. This mode of operation allows high throughput rates to be achieved. Figure 20 shows how this optimum throughput rate is achieved by bringing $\overline{\text{CONVST}}$ high before the end of a conversion, i.e., before the $\overline{\text{EOC}}$ pulses low. When operating in this mode a new conversion should not be initiated until 30 ns after the end of a read operation. This is to allow the track/hold to acquire the analog signal to 0.5 LSB accuracy.

Mode 2 Operation (Automatic Power-Down)

When the AD7822, AD7825, and AD7829 are operated in Mode 2 (see Figure 21), they automatically power down at the end of a conversion. The $\overline{\text{CONVST}}$ signal is brought low to initiate a conversion and is left logic low until after the $\overline{\text{EOC}}$ goes high, i.e., approximately 100 ns after the end of the conversion. The state of the $\overline{\text{CONVST}}$ signal is sampled at this point (i.e., 530 ns maximum after $\overline{\text{CONVST}}$ falling edge) and the AD7822, AD7825, and AD7829 will power down as long as $\overline{\text{CONVST}}$ is low. The ADC is powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. Superior power performance can be achieved in this mode of operation by only powering up the AD7822, AD7825, and AD7829 to carry out a conversion. The parallel interface of the AD7822, AD7825, and AD7829 is still fully operational while the ADCs are powered down. A read may occur while the part is powered down, and so it does not necessarily need to be placed within the $\overline{\text{EOC}}$ pulse as shown in Figure 21.

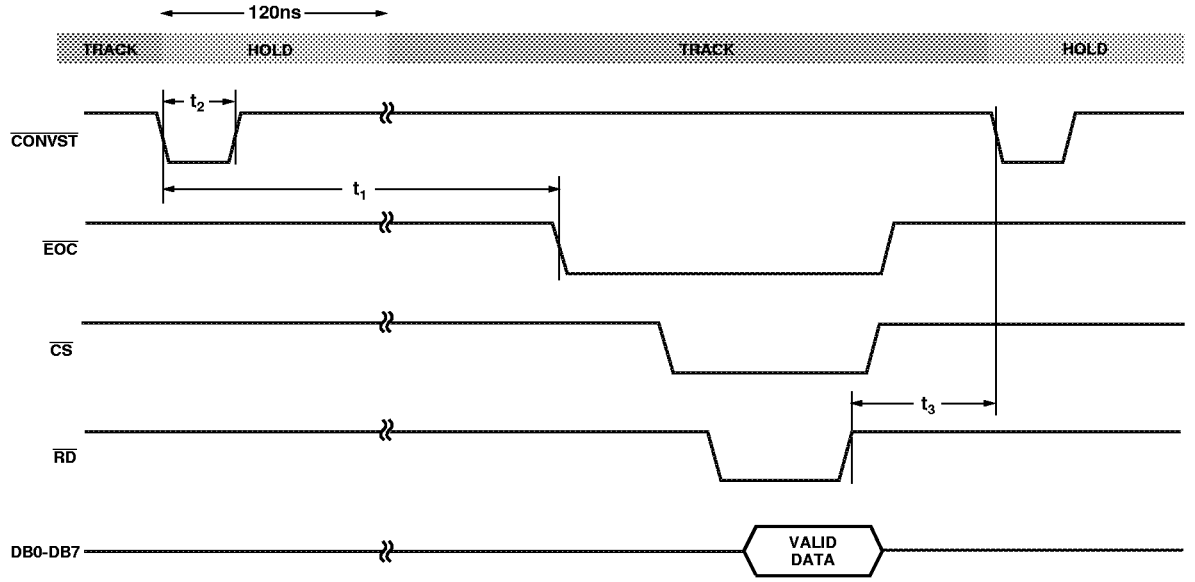


Figure 20. Mode 1 Operation

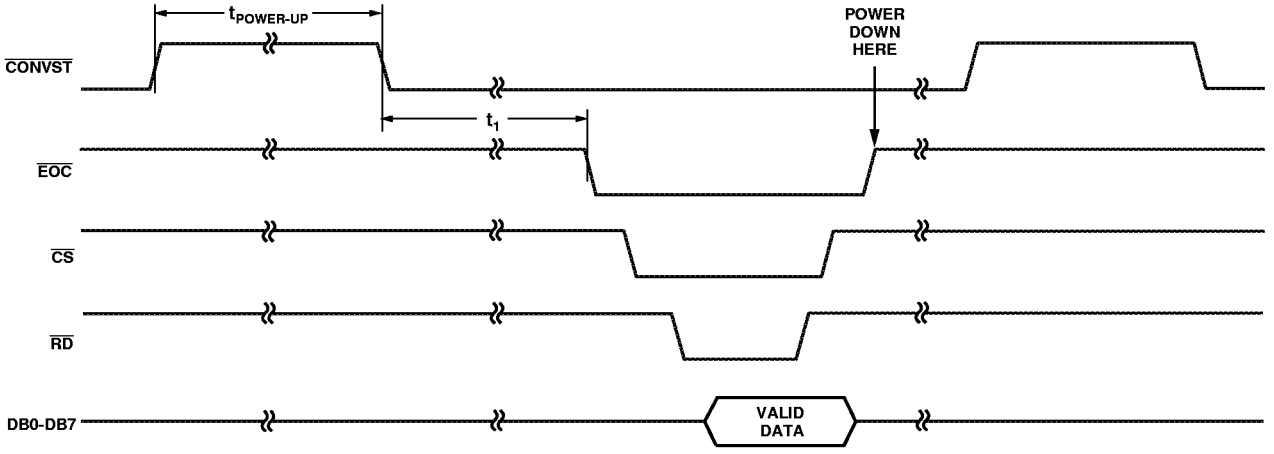


Figure 21. Mode 2 Operation

PARALLEL INTERFACE

The parallel interface of the AD7822, AD7825, and AD7829 is eight bits wide. Figure 22 shows a timing diagram illustrating the operational sequence of the AD7822/AD7825/AD7829 parallel interface. The multiplexer address is latched into the AD7822/AD7825/AD7829 on the falling edge of the $\overline{RD}$ input. The on-chip track/hold goes into hold mode on the falling edge of $\overline{CONVST}$ and a conversion is also initiated at this point. When the conversion is complete, the end of conversion line ($\overline{EOC}$) pulses low to indicate that new data is available in the output register of the AD7822, AD7825, and AD7829. The $\overline{EOC}$ pulse will stay logic low for a maximum time of 110 ns. However, the $\overline{EOC}$ pulse can be reset high by a rising edge of $\overline{RD}$. This $\overline{EOC}$ line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{CS}$ and $\overline{RD}$ going low accesses the 8-bit conversion result. It is possible to tie $\overline{CS}$ permanently low and use only $\overline{RD}$ to access the data. In systems where the part is interfaced to a gate array or ASIC, this $\overline{EOC}$ pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7822, AD7825, and AD7829 and into the gate array or ASIC. This means that the gate array or ASIC does not need any conversion status recognition logic and it also eliminates the logic required in the gate array or ASIC to generate the read signal for the AD7822, AD7825, and AD7829.

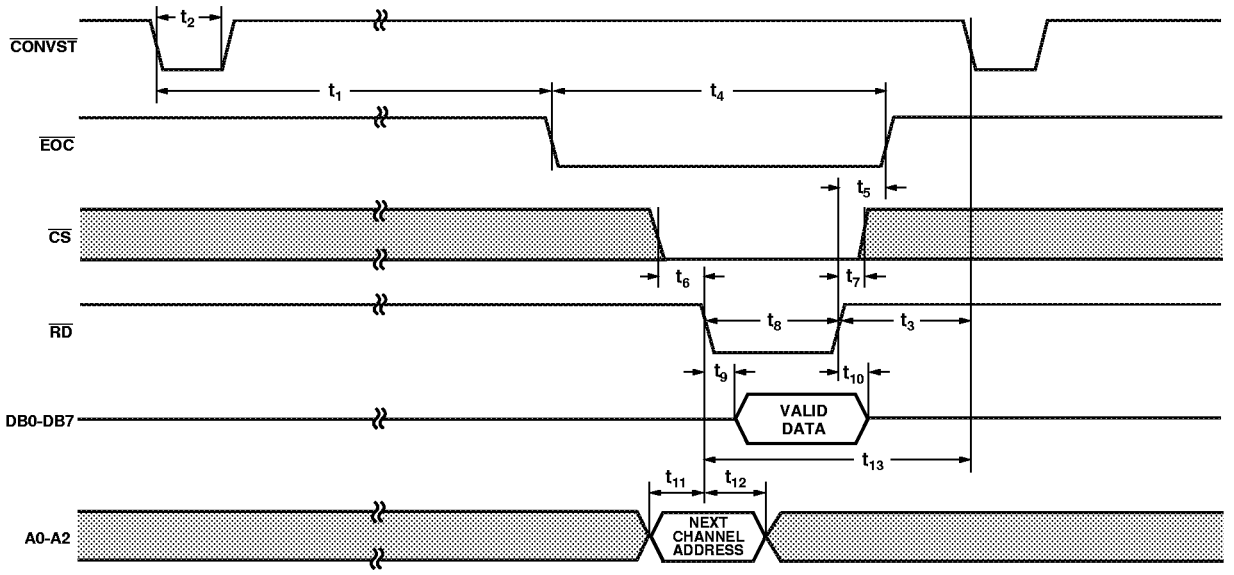


Figure 22. AD7822/AD7825/AD7829 Parallel Port Timing

MICROPROCESSOR INTERFACING

The parallel port on the AD7822/AD7825/AD7829 allows the ADCs to be interfaced to a range of many different microcontrollers. This section explains how to interface the AD7822, AD7825, and AD7829 with some of the more common microcontroller parallel interface protocols.

AD7822/AD7825/AD7829 to 8051

Figure 23 below shows a parallel interface between the AD7822, AD7825, and AD7829 and the 8051 microcontroller. The $\overline{EOC}$ signal on the AD7822, AD7825, and AD7829 provides an interrupt request to the 8051 when a conversion ends and data is ready. Port 0 of the 8051 may serve as an input or output port, or as in this case when used together, may be used as a bidirectional low order address and data bus. The address latch enable output of the 8051 is used to latch the low byte of the address during accesses to the device, while the high order address byte is supplied from Port 2. Port 2 latches remain stable when the AD7822, AD7825, and AD7829 are addressed, as they do not have to be turned around (set to 1) for data input as is the case for Port 0.

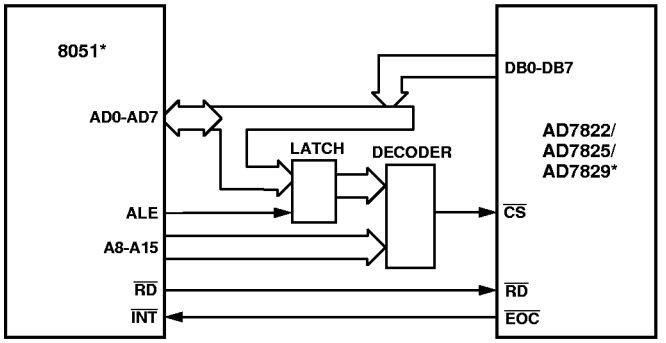


Figure 23. Interfacing to the 8051

AD7822/AD7825/AD7829 to PIC16C6x/7x

Figure 24 shows a parallel interface between the AD7822, AD7825, and AD7829 and the PIC16C64/65/74. The $\overline{EOC}$ signal on the AD7822, AD7825, and AD7829 provides an interrupt request to the microcontroller when a conversion begins. Of the PIC16C6x/7x range of microcontrollers only the PIC16C64/65/74 can provide the option of a parallel slave port. Port D of the microcontroller will operate as an 8-bit wide parallel slave port when control bit PSPMODE in the TRISE register is set. Setting PSPMODE enables the port pin RE0 to be the $\overline{RD}$ output and RE2 to be the $\overline{CS}$ (chip select) output. For this functionality, the corresponding data direction bits of the TRISE register must be configured as outputs (reset to 0). See PIC16/17 Microcontroller User Manual.

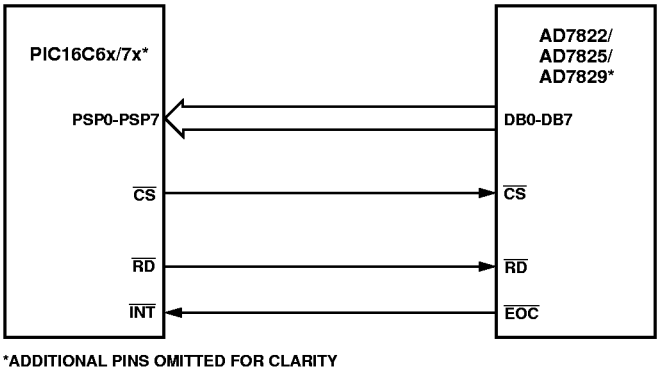


Figure 24. Interfacing to the PIC16C6x/7x

AD7822/AD7825/AD7829 to ADSP-21xx

Figure 25 below shows a parallel interface between the AD7822, AD7825, and AD7829 and the ADSP-21xx series of DSPs. As before, the $\overline{EOC}$ signal on the AD7822, AD7825, and AD7829 provides an interrupt request to the DSP when a conversion ends.

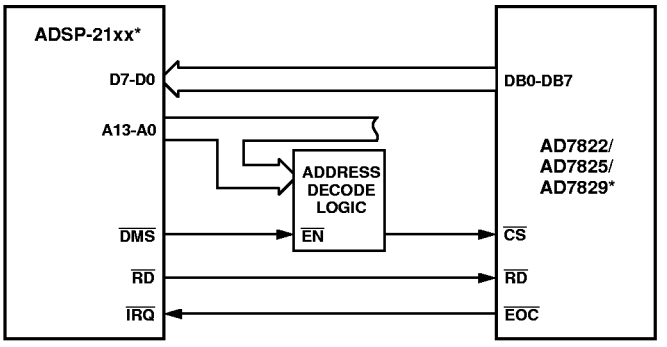


Figure 25. Interfacing to the ADSP-21xx

Interfacing Multiplexer Address Inputs

Figure 26 shows a simplified interfacing scheme between the AD7825/AD7829 and any microprocessor or microcontroller, which facilitates easy channel selection on the ADCs. The multiplexer address is latched on the falling edge of the $\overline{RD}$ signal, as outlined in the Parallel Interface section, which allows the use of the 3 LSBs of the address bus to select the channel address. As shown in Figure 26, only address bits A3 to A15 are address decoded allowing A0 to A2 to be changed according to desired channel selection without affecting chip selection.

The AD7822, being the single channel device, does not have any multiplexer addressing associated with it and can in fact be controlled with just one signal, i.e., the $\overline{CONVST}$ signal. As shown in Figure 27 the $\overline{RD}$ and $\overline{CS}$ pins are both tied to the $\overline{EOC}$ pin and the resulting signal may be used as an interrupt request signal (IRQ) on a DSP, as a $\overline{WR}$ signal to memory or as a CLK to a latch or ASIC. The timing for this interface, as shown in Figure 27, demonstrates how with the $\overline{CONVST}$ signal alone, a conversion may be initiated, data is latched out and the operating mode of the AD7822 can be selected.

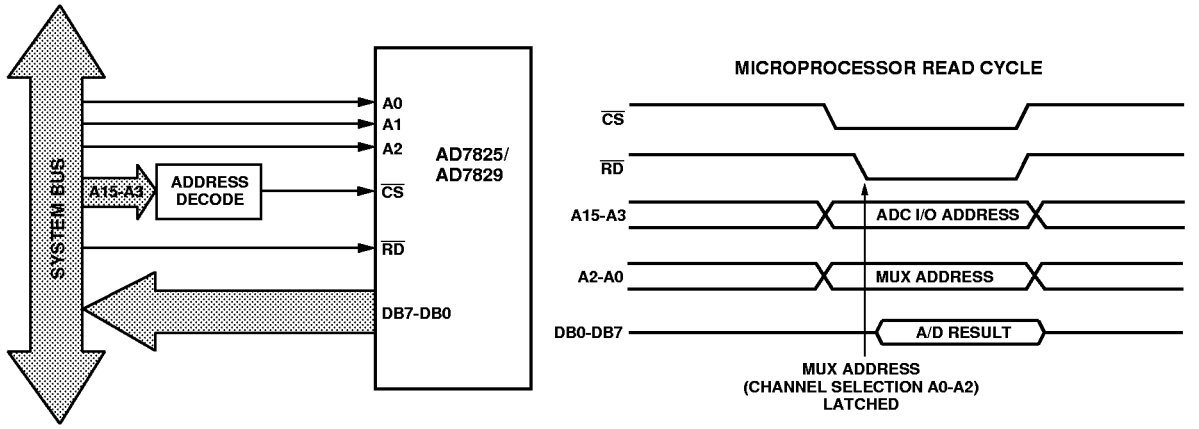


Figure 26. AD7825/AD7829 Simplified Micro Interfacing Scheme

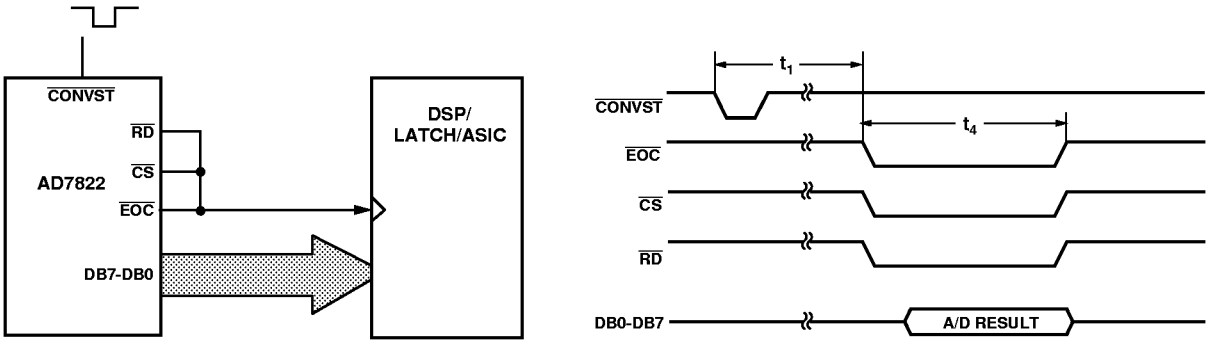
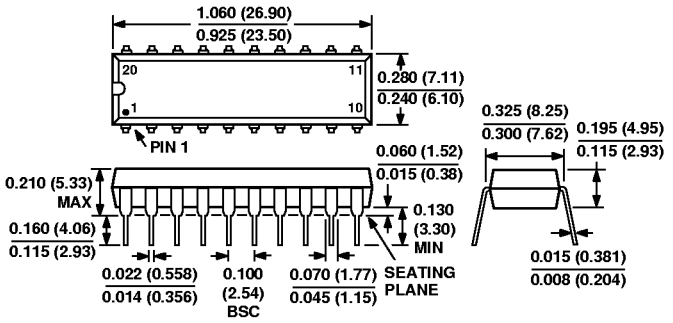


Figure 27. AD7822 Stand-Alone Operation

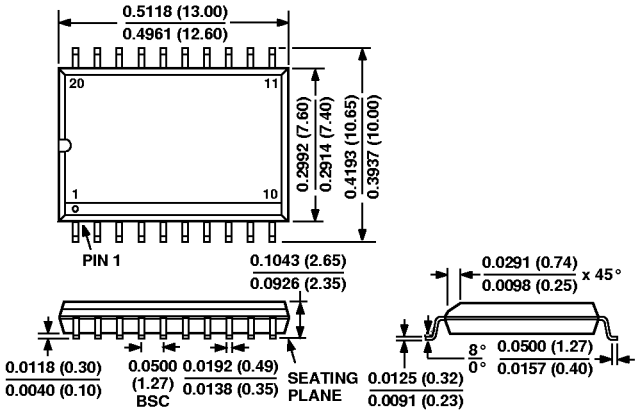
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

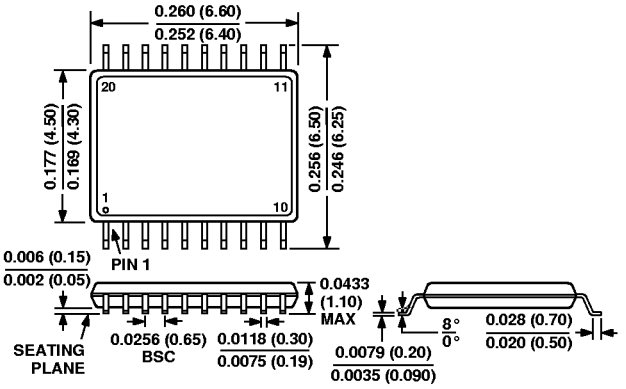
20-Lead Plastic DIP
(N-20)



20-Lead Small Outline Package
(R-20)



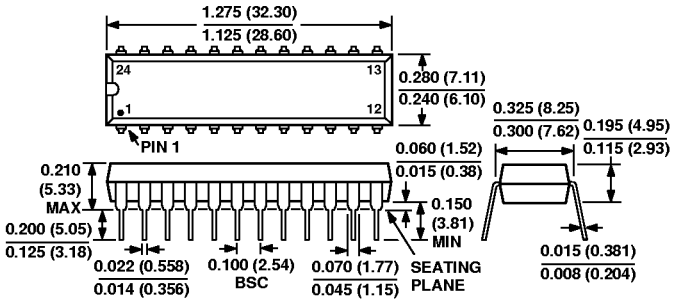
20-Lead Thin Shrink Small Outline Package
(RU-20)



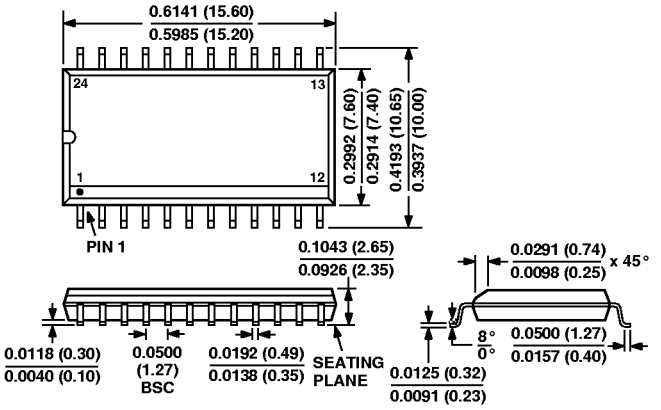
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

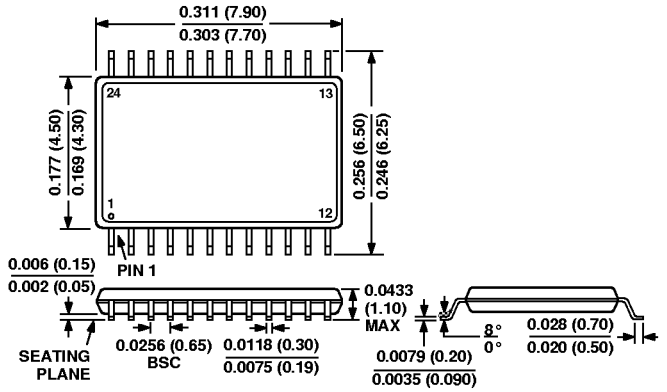
24-Lead Plastic DIP
(N-24)



24-Lead Small Outline Package
(R-24)



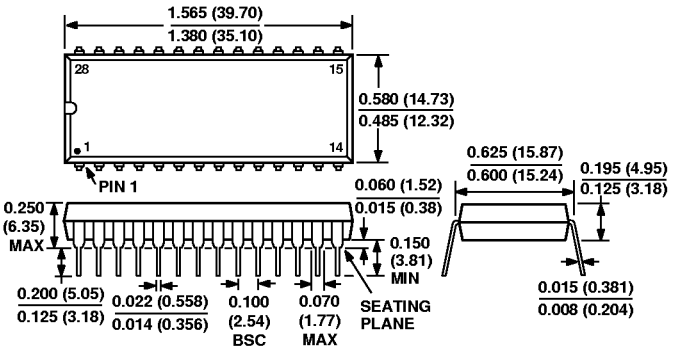
24-Lead Thin Shrink Small Outline Package
(RU-24)



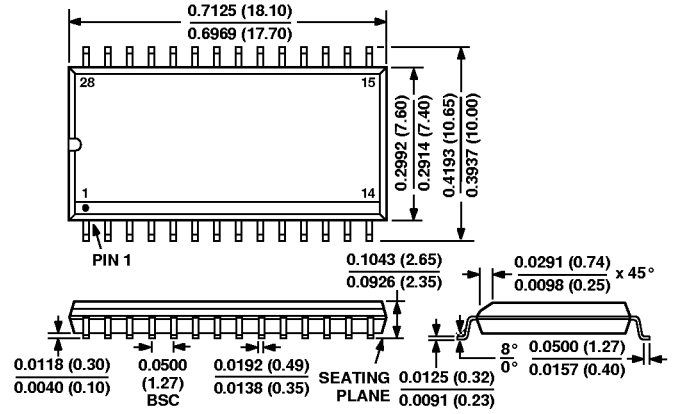
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

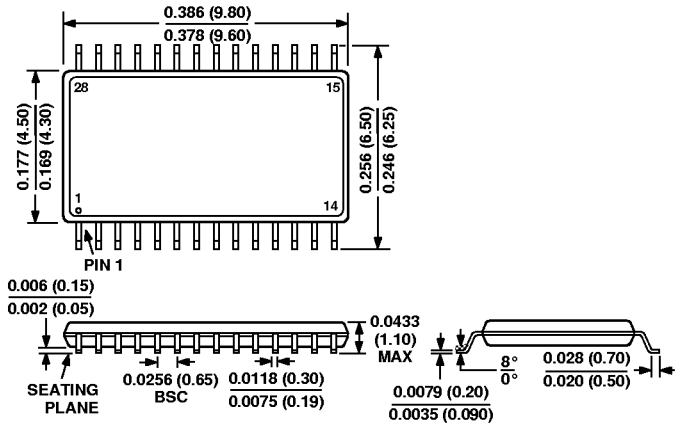
28-Lead Plastic DIP
(N-28)



28-Lead Small Outline Package
(R-28)



28-Lead Thin Shrink Small Outline Package
(RU-28)



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