DS3, 2003-11-24

SEROCCO-D

2-Channel Serial Optimized Communication Controller with DMA

PEB 20542 V1.3, PEF 20542 V1.3 Date Code > E317

Preface

This Preliminary Delta Sheet shows the changes and improvements of SEROCCO-D V1.3 over the previous Version V1.2.

1 Overview

1.1 Functional Changes

The following functions have been changed:

- Version status in register changed in VER3 from 20_H to 30_H.
- The boundary scan version number changed from 2_H to 3_H. A new BSDL file is required.

Revision History: Previous Version:	DS1	2002-09-01
	DS2	2003-08-27

2 Correction of Errata

The following erratas known and documented in the Errata Sheet of SEROCCO-D Version V1.2 have been corrected:

- $\overline{\text{DTACK}}$/$\overline{\text{READY}}$-Controlled Cycles
- DMA in Motorola Interface Mode
- DPLL in Bus Configuration
- HDLC Auto Mode: RNR not clearable
- HDLC Mode: 1-Byte Frames with ITF=1
- Extended Transparent Mode: XDU recovery
- Extended Transparent Mode: Octet alignment in CM5a/b
- CD Status Change Interrupt
- Disable Reception of CRC
- Interframe Time Fill in Combination with Flow Control using $\overline{\text{CTS}}$
- Using Continuous FLAGs as Interframe Time Fill

3 Electrical Characteristics

3.1 Changed AC Characteristics

Table 1 Infineon/Intel Bus Interface Timing (Slave Access)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
10	active $\overline{\text{RD}}$ to valid data delay		24	ns

Table 2 Motorola Bus Interface Timing (Slave Access)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
40	active address to active $\overline{\text{DS}}$ setup time	8		ns
48	active $\overline{\text{DS}}$ (read) to valid data delay		25	ns

Table 3 Infineon/Intel Bus Interface Timing (Master Access)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
60a	clock to valid address delay	9	22	ns

Table 3 Infineon/Intel Bus Interface Timing (Master Access) (cont'd)

No.	Parameter	Limit Values		Unit
		Min.	Max.	
60b	clock to invalid address delay	5	14	ns
63	valid data to inactive RD setup time	8		ns