INTERSIL

2N5452-2N5454 Monolithic Dual N-Channel JFET

FEATURES

- Offset Voltage 5 mV
- Drift 5 $\mu V/^{\circ}C$
- Low Capacitance
- Low Output Conductance — 1 μmho Max

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

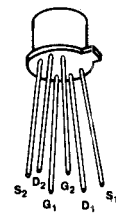
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	2.86 mW/°C
Both Sides	4.3 mW/°C

Maximum Voltages & Currents

V_{GS}	Gate to Source Voltage	-50 V
V_{GD}	Gate to Drain Voltage	-50 V

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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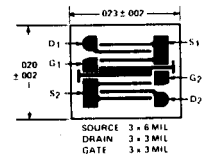

ORDERING INFORMATION

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5452 MIN	2N5452 MAX	2N5453 MIN	2N5453 MAX	2N5454 MIN	2N5454 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
			-200		-200		-200	nA		T_A = 150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	V	V_{DS} = 20 V, I_D = 50 μA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2	V	V_{DS} = 0, I_G = 1 mA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		μmho		f = 100 MHz
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0	μmho		f = 1 kHz
			1.0		1.0		1.0	μmho	V_{DS} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2	pF		
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5	pF	V_{DG} = 10 V, I_S = 0	
$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		V_{DS} = 20 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0	mV		T = 25°C to -55°C
			0.5		1.0		2.5	mV		T = 25°C to +125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		f = 1 kHz