

**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
SURFACE MOUNT (UB)**

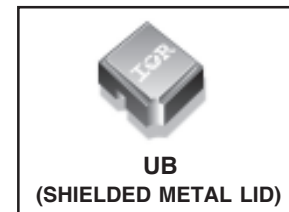
**IRHLUB770Z4
JANSR2N7616UB
60V, N-CHANNEL
REF: MIL-PRF-19500/744**



Product Summary

Part Number	Radiation Level	R _{DS(on)}	I _D	QPL Part Number
IRHLUB770Z4	100K Rads (Si)	0.68Ω	0.8A	JANSR2N7616UB
IRHLUB730Z4	300K Rads (Si)	0.68Ω	0.8A	JANSF2N7616UB

**Refer to Page 11 for 3 Additional Part Numbers -
IRHLUBN770Z4, IRHLUBC770Z4, IRHLUBCN770Z4**



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary P-Channel Available -
IRHLUB7970Z4, IRHLUBN7970Z4
IRHLUBC7970Z4 & IRHLUBCN7970Z4

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = 4.5V, T _C = 25°C	Continuous Drain Current	0.8	A
I _D @ V _{GS} = 4.5V, T _C = 100°C	Continuous Drain Current	0.5	
I _{DM}	Pulsed Drain Current ①	3.2	
P _D @ T _C = 25°C	Max. Power Dissipation	0.6	W
	Linear Derating Factor	0.005	W/°C
V _{GS}	Gate-to-Source Voltage	±10	V
E _{AS}	Single Pulse Avalanche Energy ②	26.6	mJ
I _{AR}	Avalanche Current ①	0.8	A
E _{AR}	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Lead Temperature	300 (for 5s)	
	Weight	43 (Typical)	mg

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.07	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.68	Ω	V _{GS} = 4.5V, I _D = 0.5A ^④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-4.04	—	mV/°C	
g _{fs}	Forward Transconductance	0.23	—	—	S	V _{DS} = 10V, I _{DS} = 0.5A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 48V, V _{GS} = 0V
		—	—	10		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	3.6	nC	V _{GS} = 4.5V, I _D = 0.8A
Q _{gs}	Gate-to-Source Charge	—	—	1.5		V _{DS} = 30V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
t _{d(on)}	Turn-On Delay Time	—	—	8.0	ns	V _{DD} = 30V, I _D = 0.8A, V _{GS} = 5.0V, R _G = 24Ω
t _r	Rise Time	—	—	24		
t _{d(off)}	Turn-Off Delay Time	—	—	30		
t _f	Fall Time	—	—	13		
L _S + L _D	Total Inductance	—	8.4	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	166	—	pF	V _{GS} = 0V, V _{DS} = 25V
C _{oss}	Output Capacitance	—	42	—		f = 100KHz
C _{rss}	Reverse Transfer Capacitance	—	3.5	—		
R _g	Gate Resistance	—	—	14	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	0.8	A	
I _{SM}	Pulse Source Current (Body Diode) ^⑤	—	—	3.2		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _j = 25°C, I _S = 0.8A, V _{GS} = 0V ^⑥
t _{rr}	Reverse Recovery Time	—	—	78	ns	T _j = 25°C, I _F = 0.8A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	75	nC	V _{DD} ≤ 25V ^⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJA}	Junction-to-Ambient	—	—	200	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHLUB770Z4, JANSR2N7616UB

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⑤ ⑥

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV_{DS}	Drain-to-Source Breakdown Voltage	60	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0		$V_{GS} = V_{DS}, I_D = 250\mu A$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 10V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -10V$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	$V_{DS} = 48V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ^④ On-State Resistance (TO-39)	—	0.55	Ω	$V_{GS} = 4.5V, I_D = 0.5A$
$R_{DS(on)}$	Static Drain-to-Source On-state ^④ Resistance (UB)	—	0.68	Ω	$V_{GS} = 4.5V, I_D = 0.5A$
V_{SD}	Diode Forward Voltage ^④	—	1.2	V	$V_{GS} = 0V, I_D = 0.8A$

1. Part Numbers IRHLUB770Z4, IRHLUB730Z4 and additional part numbers listed on page 11.

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS=0V	@VGS=-2V	@VGS=-4V	@VGS=-5V	@VGS=-6V	@VGS=-7V
$38 \pm 5\%$	$300 \pm 7.5\%$	$38 \pm 7.5\%$	60	60	60	60	60	35
$62 \pm 5\%$	$355 \pm 7.5\%$	$33 \pm 7.5\%$	60	60	60	60	30	-
$85 \pm 5\%$	$380 \pm 7.5\%$	$29 \pm 7.5\%$	60	60	60	40	-	-

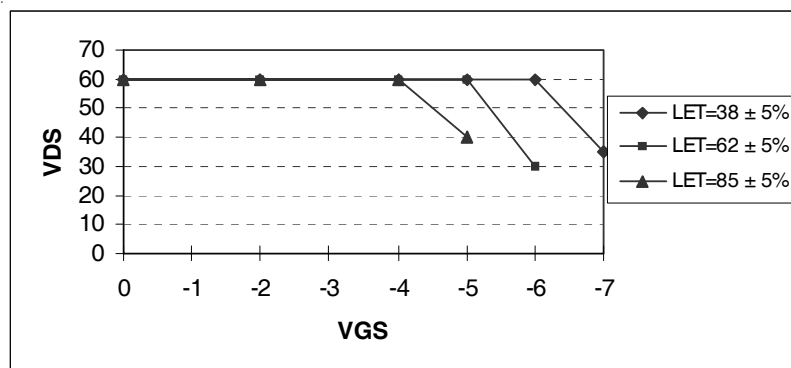


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

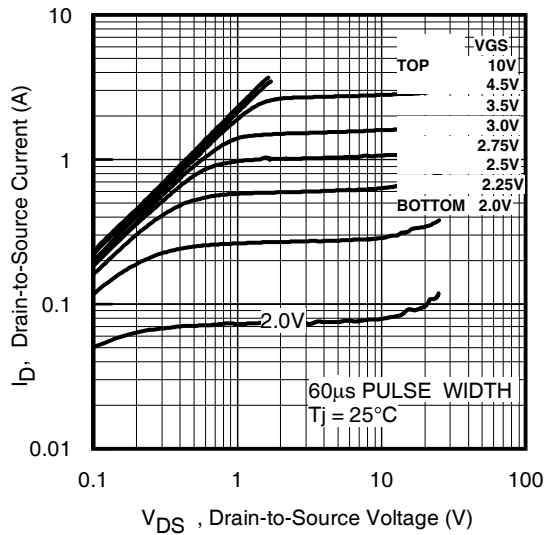


Fig 1. Typical Output Characteristics

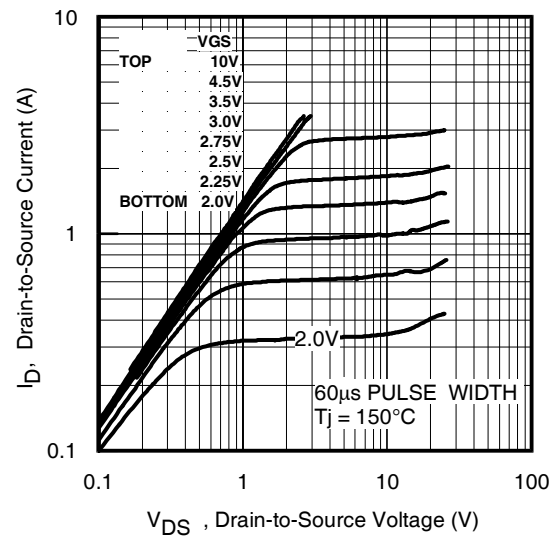


Fig 2. Typical Output Characteristics

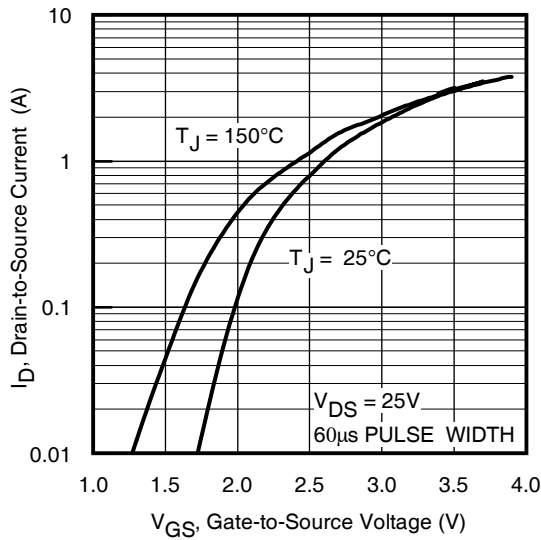


Fig 3. Typical Transfer Characteristics

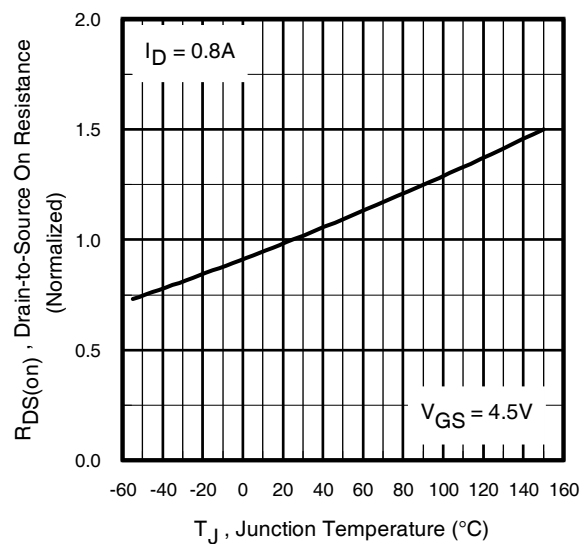


Fig 4. Normalized On-Resistance Vs. Temperature

Pre-Irradiation

IRHLUB770Z4, JANSR2N7616UB

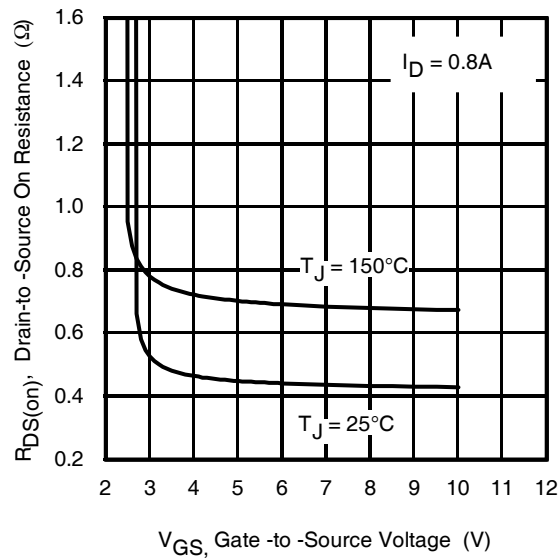


Fig 5. Typical On-Resistance Vs Gate Voltage

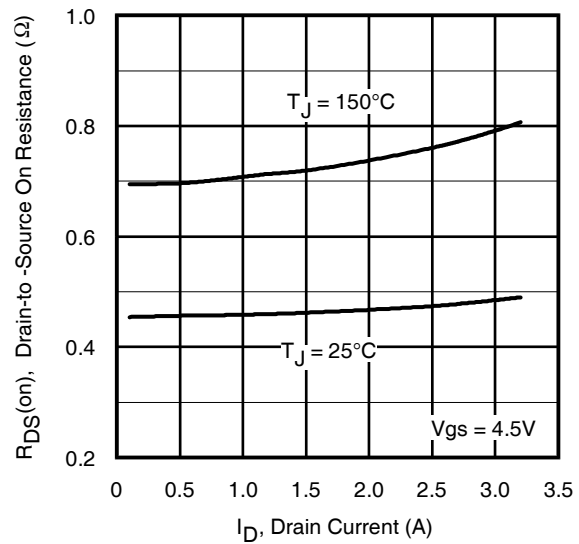


Fig 6. Typical On-Resistance Vs Drain Current

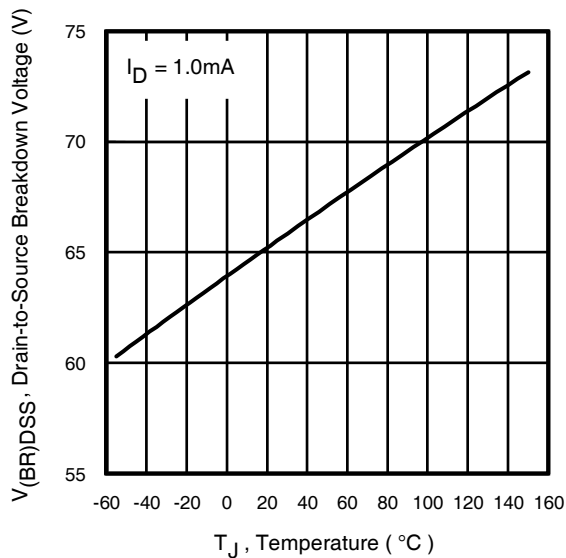


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

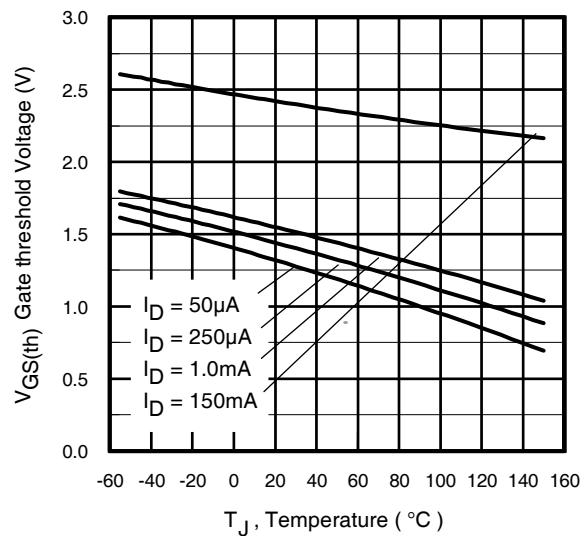


Fig 8. Typical Threshold Voltage Vs Temperature

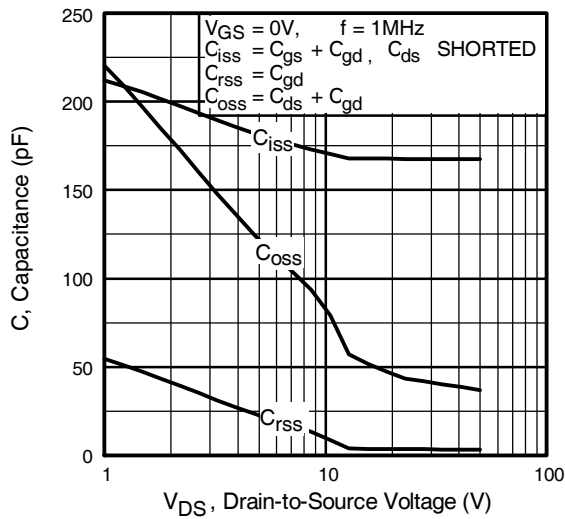


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

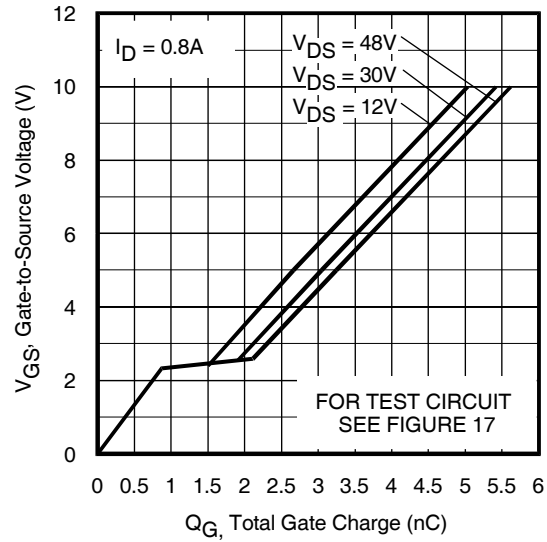


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

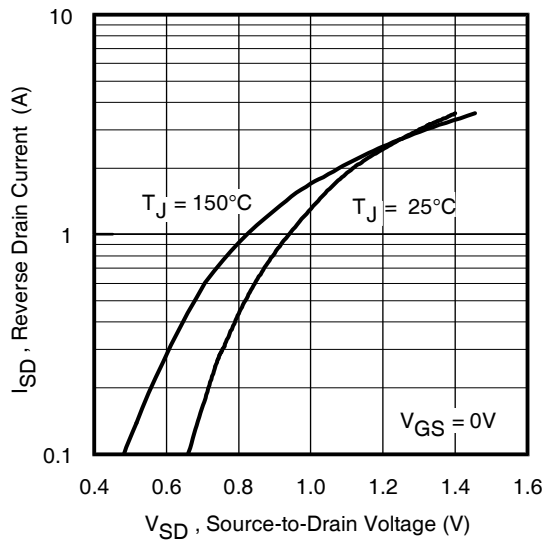


Fig 11. Typical Source-Drain Diode Forward Voltage

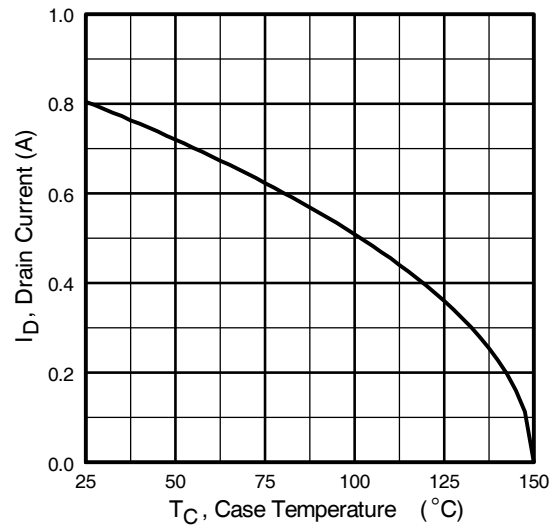


Fig 12. Maximum Drain Current Vs. Case Temperature

Pre-Irradiation

IRHLUB770Z4, JANSR2N7616UB

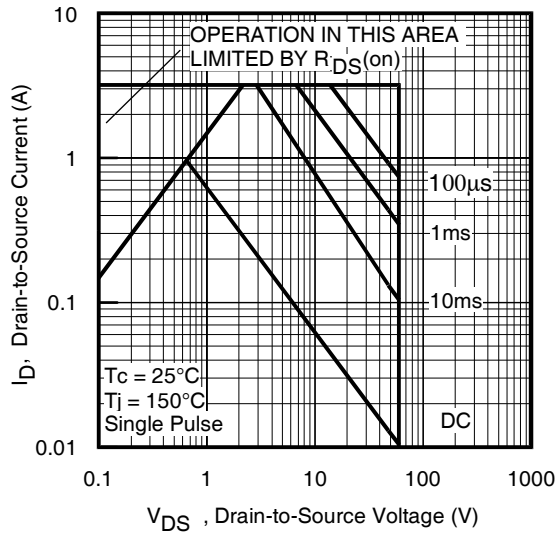


Fig 13. Maximum Safe Operating Area

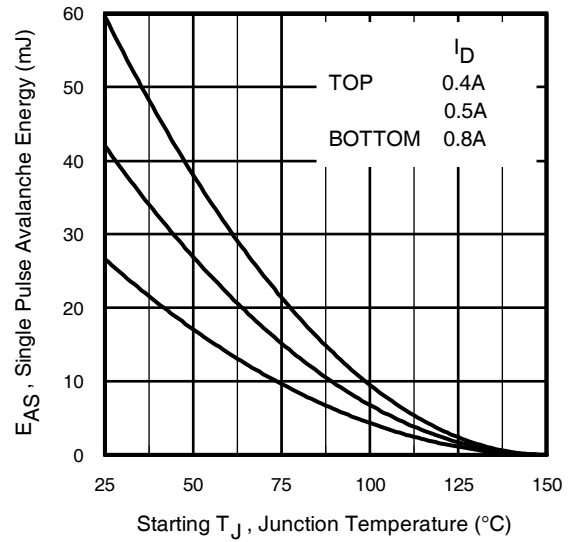


Fig 14. Maximum Avalanche Energy Vs. Drain Current

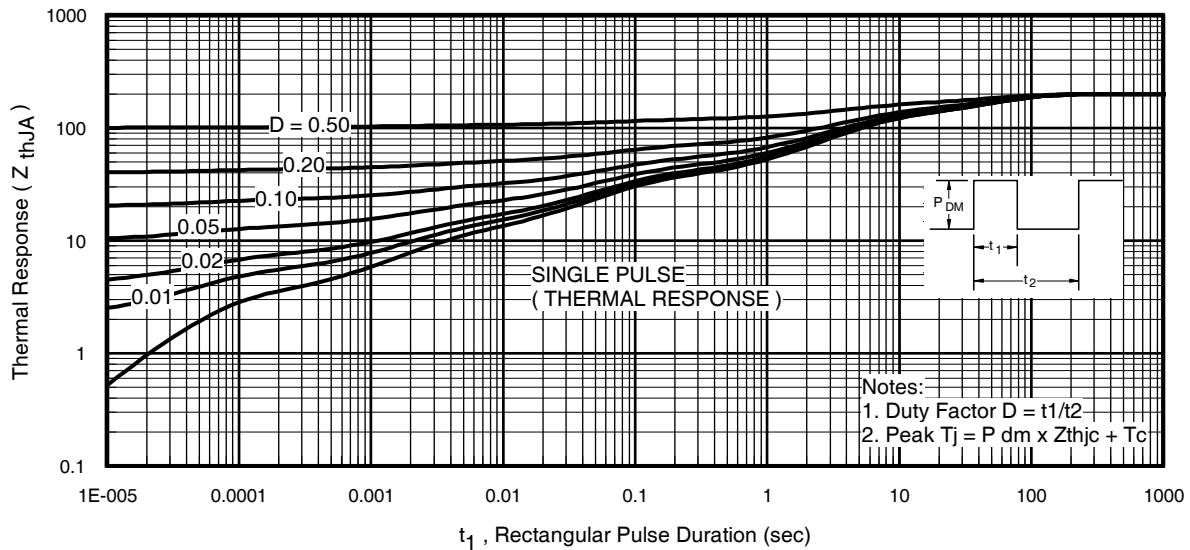


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

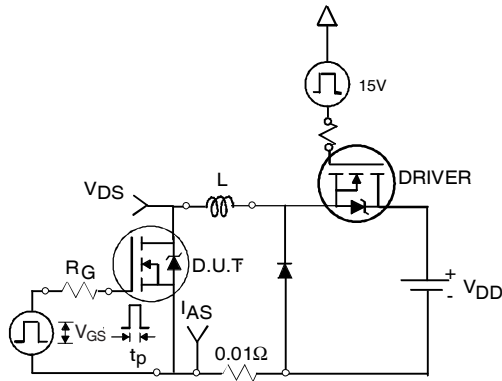


Fig 16a. Unclamped Inductive Test Circuit

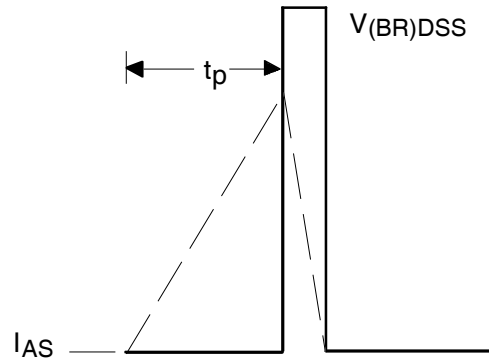


Fig 16b. Unclamped Inductive Waveforms

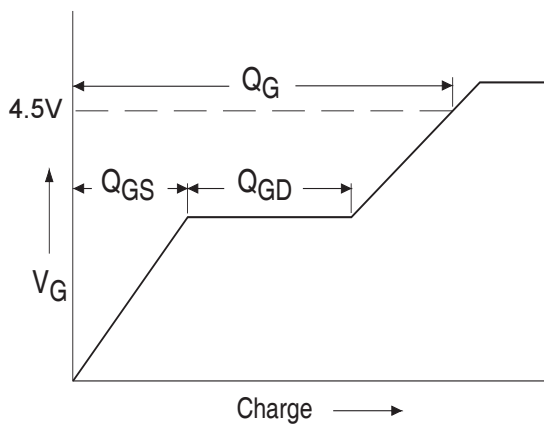


Fig 17a. Basic Gate Charge Waveform

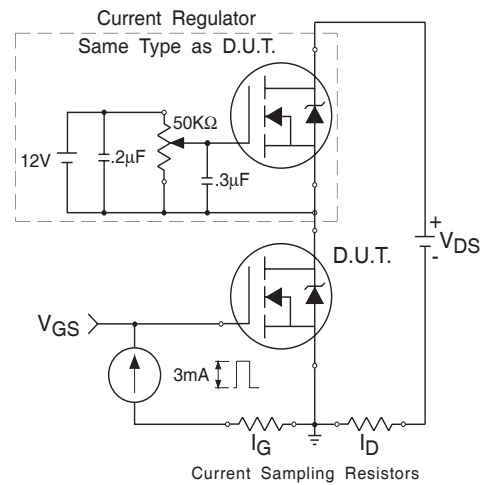


Fig 17b. Gate Charge Test Circuit

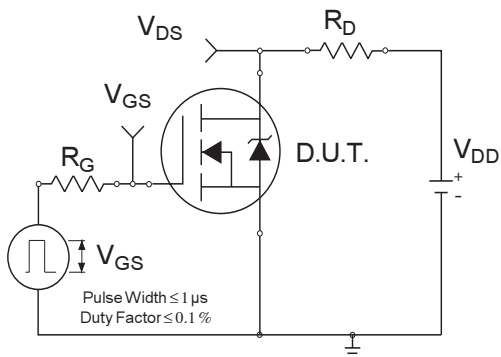


Fig 18a. Switching Time Test Circuit

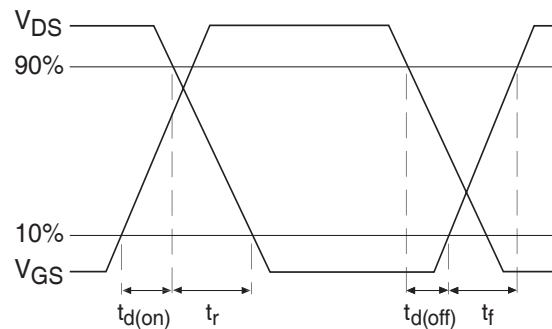
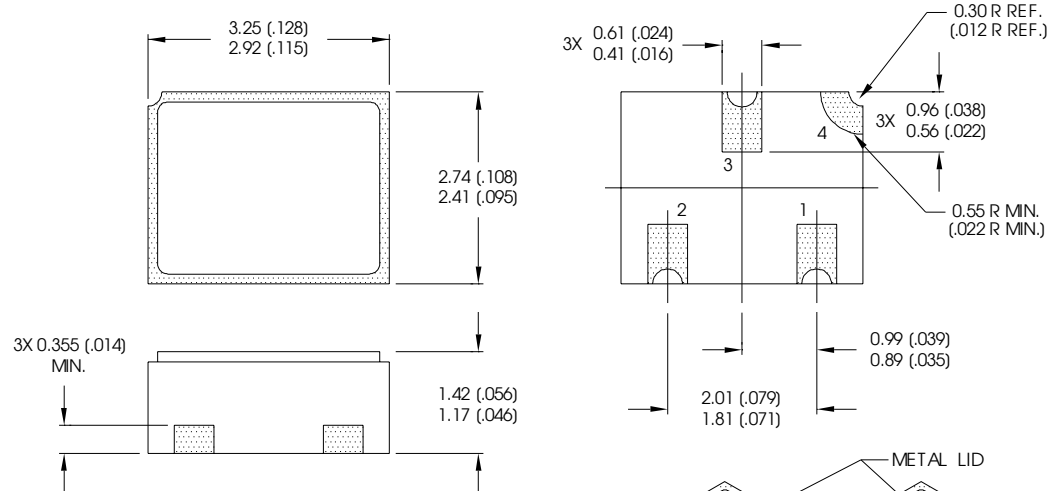
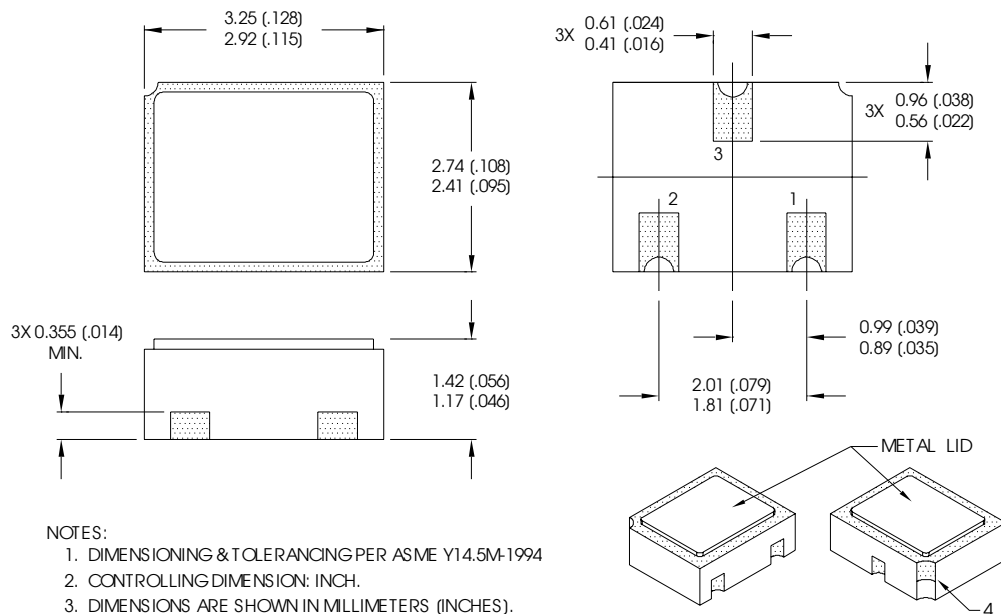


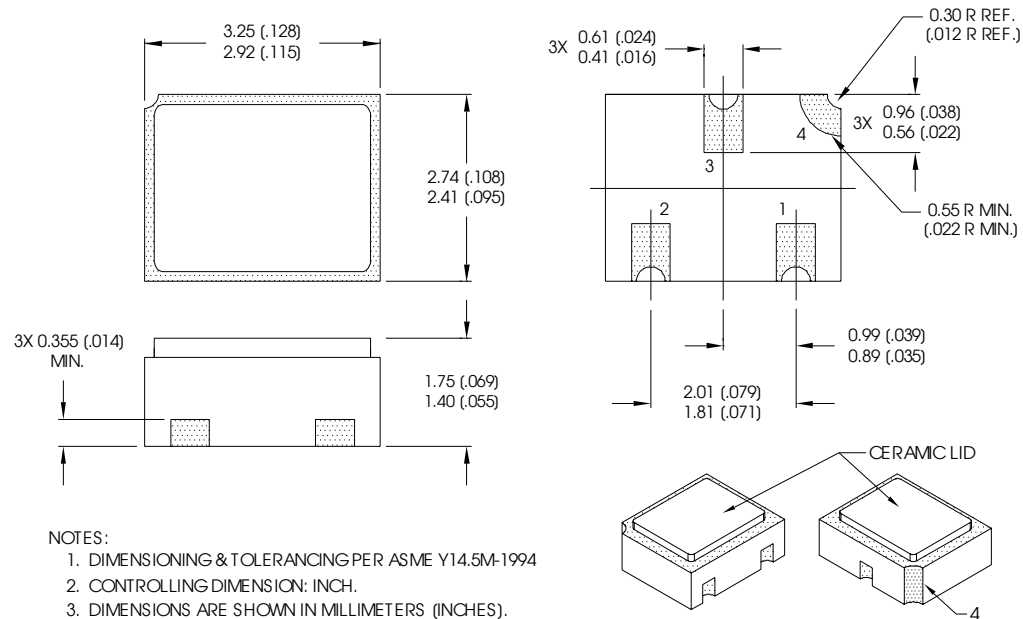
Fig 18b. Switching Time Waveforms

Case Outline and Dimensions — UB (Shielded Metal Lid Connected to 4th Pad)**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.
5. PAD ASSIGNMENTS: 1 = GATE, 2 = SOURCE, 3 = DRAIN, 4 = SHIELDING CONNECTED TO THE LID.

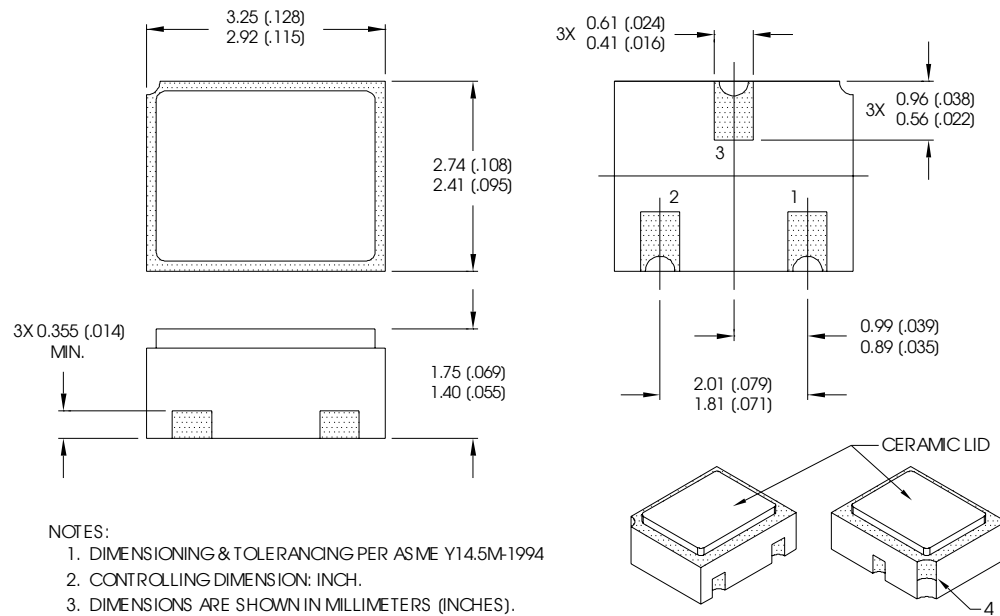
Case Outline and Dimensions — UBN (Isolated Metal Lid, No 4th Pad)**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.
5. PAD ASSIGNMENTS: 1 = GATE, 2 = SOURCE, 3 = DRAIN, 4 = ISOLATED METAL LID.

Case Outline and Dimensions—UBC (Shielded Ceramic Lid Connected to 4th Pad)

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.
5. PAD ASSIGNMENTS: 1 = GATE, 2 = SOURCE, 3 = DRAIN, 4 = SHIELDING CONNECTED TO THE LID.

Case Outline and Dimensions — UBCN (Isolated Ceramic Lid, No 4th Pad)

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.
5. PAD ASSIGNMENTS: 1 = GATE, 2 = SOURCE, 3 = DRAIN, 4 = ISOLATED CERAMIC LID.

Pre-Irradiation

IRHLUB770Z4, JANSR2N7616UB

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, $L = 83\text{ mH}$
Peak $I_L = 0.8A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 0.8A$, $di/dt \leq 130A/\mu s$,
 $V_{DD} \leq 60V$, $T_J \leq 150^{\circ}C$
- ④ Pulse width $\leq 300\text{ }\mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Additional Product Summaries (continued from page 1 and 3)

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBN (ISOLATED METAL LID)
IRHLUBN770Z4	100K Rads (Si)	0.68Ω	0.8A	JANSR2N7616UBN	
IRHLUBN730Z4	300K Rads (Si)	0.68Ω	0.8A	JANSF2N7616UBN	

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBC (SHIELDED CERAMIC LID)
IRHLUBC770Z4	100K Rads (Si)	0.68Ω	0.8A	JANSR2N7616UBC	
IRHLUBC730Z4	300K Rads (Si)	0.68Ω	0.8A	JANSF2N7616UBC	

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBCN (ISOLATED CERAMIC LID)
IRHLUBCN770Z4	100K Rads (Si)	0.68Ω	0.8A	JANSR2N7616UBCN	
IRHLUBCN730Z4	300K Rads (Si)	0.68Ω	0.8A	JANSF2N7616UBCN	

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Data and specifications subject to change without notice. 11/