

## The RF MOSFET Line

### 30W, to 400MHz, 28V

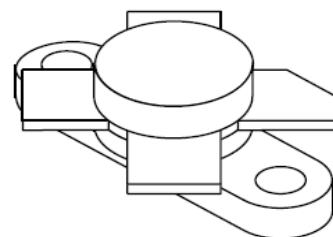
Rev. V2

Designed for wideband large signal output and drive stages up to 400 MHz range.

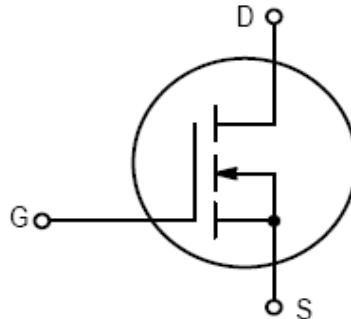
N-Channel enhancement mode

- Guaranteed 28 V, 150 MHz performance
  - Output power = 30 W
  - Minimum gain = 13 dB
  - Efficiency — 60% (Typical)
- Small- and large-signal characterization
- Typical performance at 400 MHz, 28 Vdc, 30 W output = 7.7 dB gain
- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Low noise figure — 1.5 dB (typ.) at 1.0 A, 150 MHz
- Excellent thermal stability, ideally suited for Class A operation
- Facilitates manual gain control, ALC and modulation techniques

#### Product Image



**CASE 211-07, STYLE 2**



## Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Vdc
Drain Current — Continuous	$I_D$	5.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	100 0.571	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Operating Junction Temperature	$T_J$	200	°C

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

**Handling and Packaging** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

1

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**The RF MOSFET Line  
30W, to 400MHz, 28V**

Rev. V2

ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 10$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28$ V, $V_{GS} = 0$ )	$I_{DSS}$	—	—	4.0	mAdc
Gate-Source Leakage Current ( $V_{GS} = 20$ V, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Threshold Voltage ( $V_{DS} = 10$ V, $I_D = 25$ mA)	$V_{GS(\text{th})}$	1.0	3.0	6.0	Vdc
Forward Transconductance ( $V_{DS} = 10$ V, $I_D = 500$ mA)	$g_{fs}$	500	750	—	mmhos

**DYNAMIC CHARACTERISTICS**

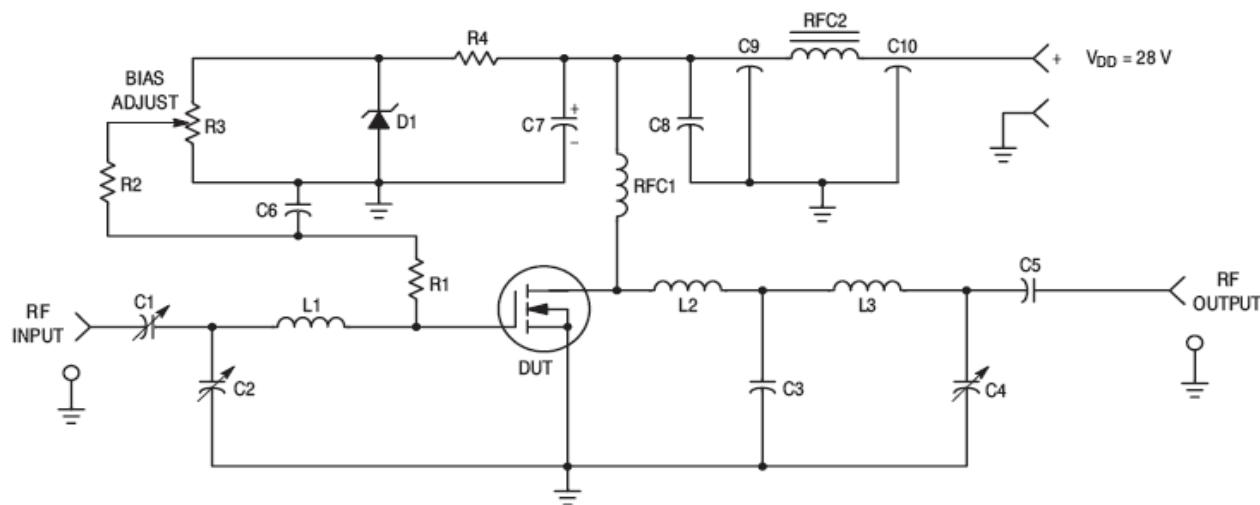
Input Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{iss}$	—	48	—	pF
Output Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{oss}$	—	54	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{rss}$	—	11	—	pF

**FUNCTIONAL CHARACTERISTICS**

Noise Figure ( $V_{DS} = 28$ Vdc, $I_D = 1.0$ A, $f = 150$ MHz)	NF	—	1.5	—	dB
Common Source Power Gain ( $V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz (Figure 1) $I_{DQ} = 25$ mA) $f = 400$ MHz (Figure 14)	$G_{ps}$	13 —	16 7.7	—	dB
Drain Efficiency (Figure 1) ( $V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz, $I_{DQ} = 25$ mA)	$\eta$	50	60	—	%
Electrical Ruggedness (Figure 1) ( $V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz, $I_{DQ} = 25$ mA, VSWR 30:1 at All Phase Angles)	$\psi$	No Degradation in Output Power			

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Rev. V2



C1 — Arco 403, 3.0–35 pF, or equivalent  
 C2 — Arco 406, 15–115 pF, or equivalent  
 C3 — 56 pF Mini-Unelco, or equivalent  
 C4 — Arco 404, 8.0–60 pF, or equivalent  
 C5 — 680 pF, 100 Mils Chip  
 C6 — 0.01  $\mu$ F, 100 V, Disc Ceramic  
 C7 — 100  $\mu$ F, 40 V  
 C8 — 0.1  $\mu$ F, 50 V, Disc Ceramic  
 C9, C10 — 680 pF Feedthru  
 D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29" ID, #18 AWG Enamel, Closewound  
 L2 — 1-1/4 Turns, 0.2" ID, #18 AWG Enamel, Closewound  
 L3 — 2 Turns, 0.2" ID, #18 AWG Enamel, Closewound  
 RFC1 — 20 Turns, 0.30" ID, #20 AWG Enamel, Closewound  
 RFC2 — Ferroxcube VK-200 — 19/4B  
 R1 — 10 k $\Omega$ , 1/2 W Thin Film  
 R2 — 10 k $\Omega$ , 1/4 W  
 R3 — 10 Turns, 10 k $\Omega$   
 R4 — 1.8 k $\Omega$ , 1/2 W  
 Board — G10, 62 Mils

Figure 1. 150 MHz Test Circuit

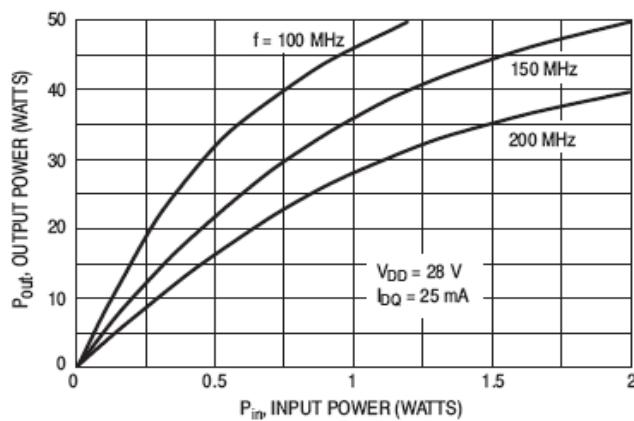


Figure 2. Output Power versus Input Power

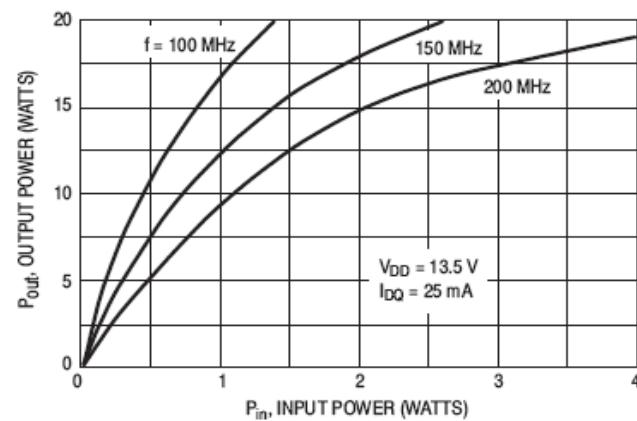


Figure 3. Output Power versus Input Power

**The RF MOSFET Line  
30W, to 400MHz, 28V**

Rev. V2

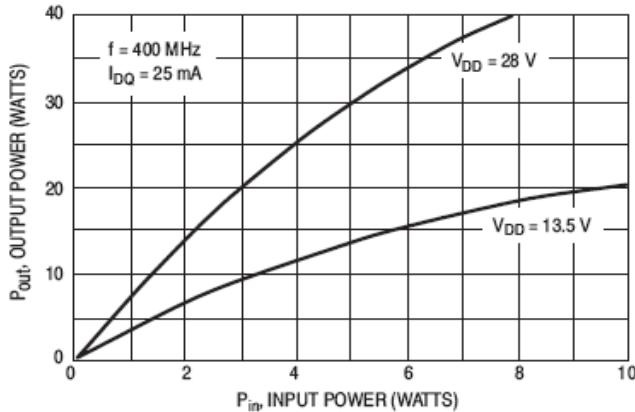


Figure 4. Output Power versus Input Power

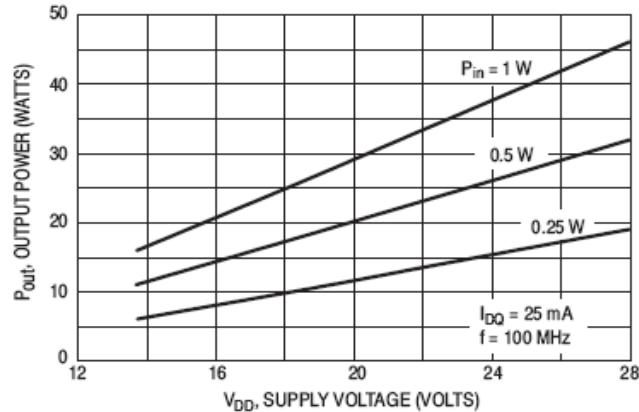


Figure 5. Output Power versus Supply Voltage

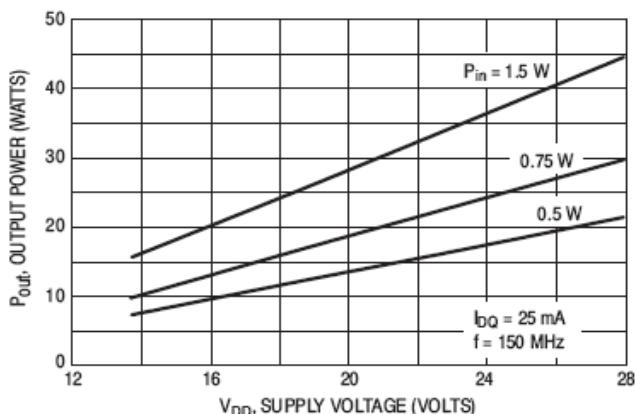


Figure 6. Output Power versus Supply Voltage

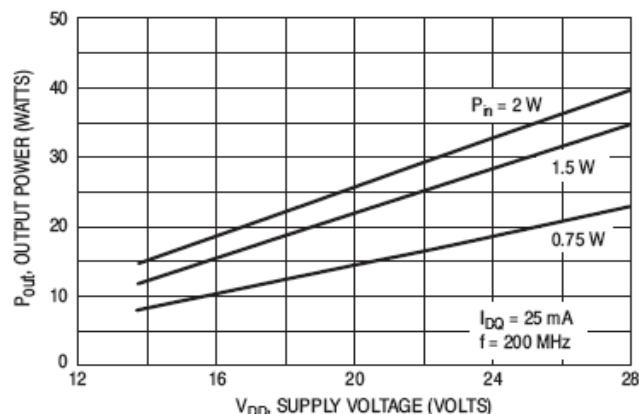


Figure 7. Output Power versus Supply Voltage

## The RF MOSFET Line 30W, to 400MHz, 28V

Rev. V2

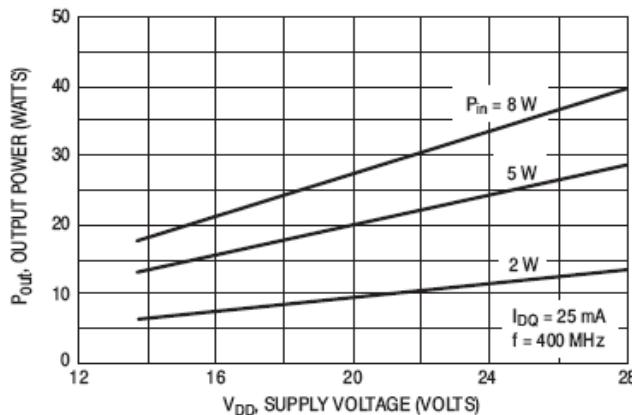


Figure 8. Output Power versus Supply Voltage

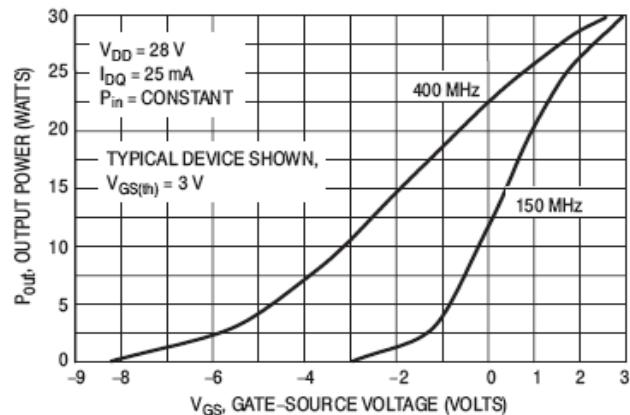


Figure 9. Output Power versus Gate Voltage

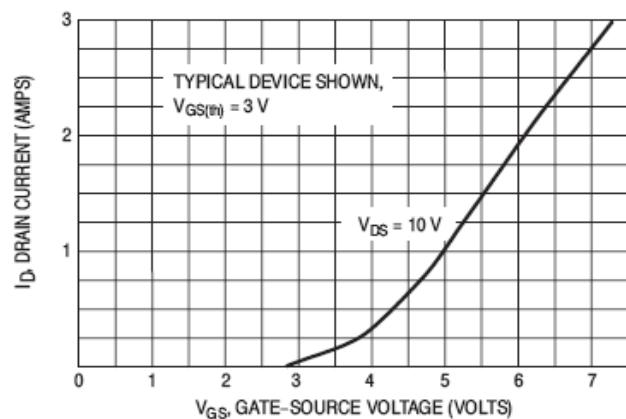


Figure 10. Drain Current versus Gate Voltage  
(Transfer Characteristics)

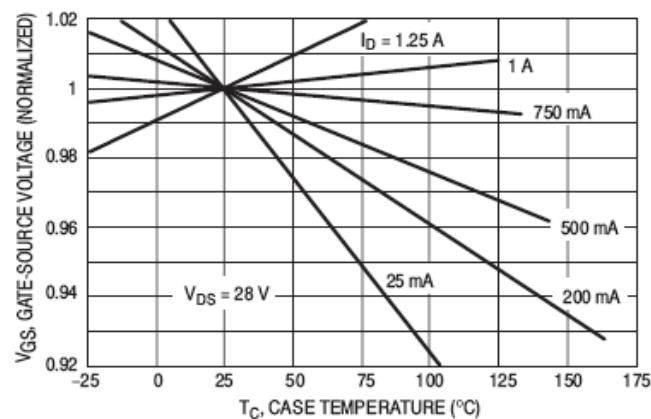


Figure 11. Gate Source Voltage versus  
Case Temperature

## The RF MOSFET Line 30W, to 400MHz, 28V

Rev. V2

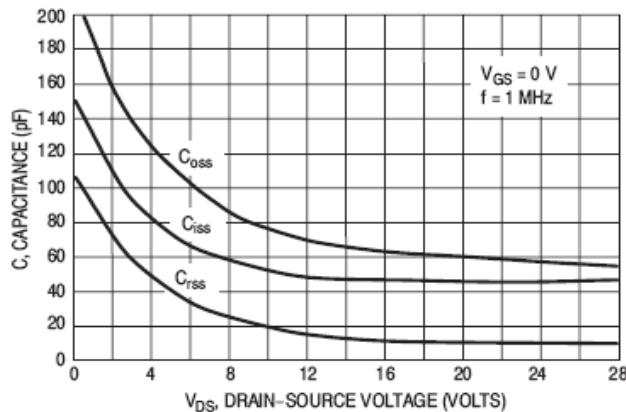


Figure 12. Capacitance versus  
Drain-Source Voltage

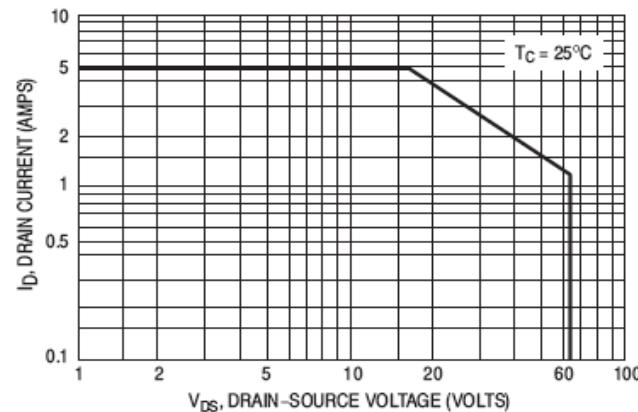
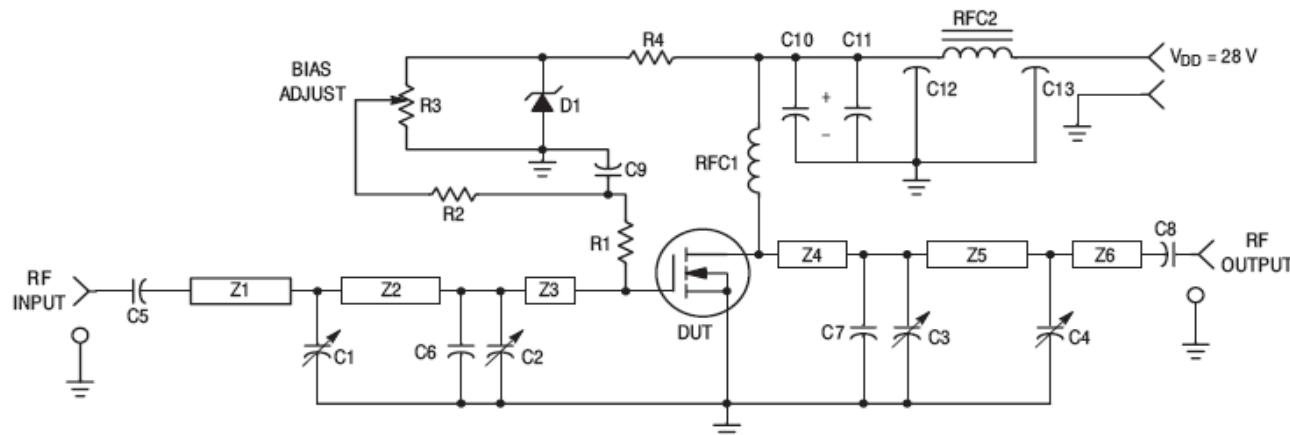


Figure 13. DC Safe Operating Area



C1, C2, C3, C4 — 0–20 pF Johanson, or equivalent  
 C5, C8 — 270 pF, 100 Mil Chip  
 C6, C7 — 24 pF Mini-Unelco, or equivalent  
 C9 — 0.01  $\mu$ F, 100 V, Disc Ceramic  
 C10 — 100  $\mu$ F, 40 V  
 C11 — 0.1  $\mu$ F, 50 V, Disc Ceramic  
 C12, C13 — 680 pF Feedthru  
 D1 — 1N5925A Motorola Zener  
 R1, R2 — 10 k $\Omega$ , 1/4 W  
 R3 — 10 Turns, 10 k $\Omega$

R4 — 1.8 k $\Omega$ , 1/2 W  
 Z1 — 2.9" x 0.166" Microstrip  
 Z2, Z4 — 0.35" x 0.166" Microstrip  
 Z3 — 0.40" x 0.166" Microstrip  
 Z5 — 1.05" x 0.166" Microstrip  
 Z6 — 1.9" x 0.166" Microstrip  
 RFC1 — 6 Turns, 0.300" ID, #20 AWG Enamel, Closewound  
 RFC2 — Ferroxcube VK-200 — 19/4B  
 Board — Glass Teflon, 62 Mils

Figure 14. 400 MHz Test Circuit

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Rev. V2

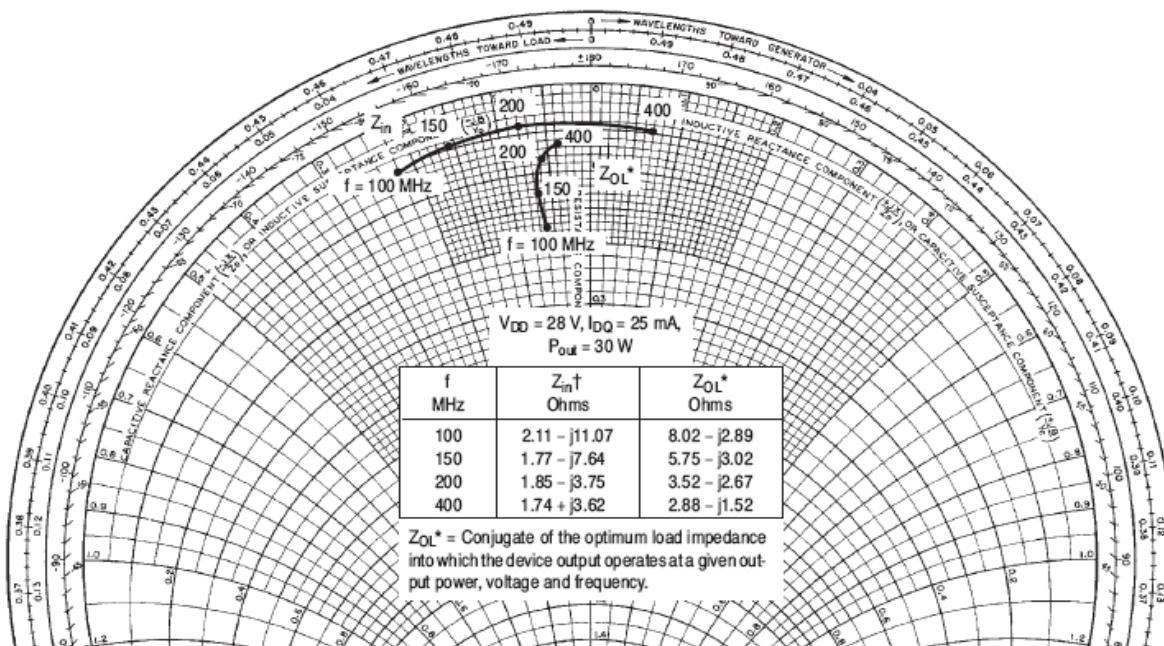


Figure 15. Large-Signal Series Equivalent Input and Output Impedance,  $Z_{in}$ ,  $Z_{OL^*}$

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Rev. V2

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ϕ	S <sub>21</sub>	∠ϕ	S <sub>12</sub>	∠ϕ	S <sub>22</sub>	∠ϕ
2.0	0.977	-32	59.48	163	0.011	67	0.661	-36
5.0	0.919	-70	48.67	142	0.024	44	0.692	-78
10	0.852	-109	33.50	122	0.032	29	0.747	-117
20	0.817	-140	19.05	106	0.037	16	0.768	-146
30	0.814	-153	13.11	99	0.038	14	0.774	-157
40	0.811	-159	9.88	95	0.038	13	0.782	-162
50	0.812	-164	7.98	92	0.038	12	0.787	-165
60	0.813	-166	6.66	89	0.038	12	0.787	-168
70	0.815	-168	5.708	86	0.038	11	0.787	-169
80	0.816	-170	5.003	84	0.038	11	0.787	-170
90	0.817	-171	4.560	83	0.038	12	0.787	-171
100	0.817	-172	4.170	81	0.039	13	0.787	-172
110	0.818	-173	3.670	80	0.039	13	0.788	-172
120	0.820	-173	3.420	79	0.039	13	0.788	-173
130	0.821	-173	3.170	79	0.039	13	0.788	-173
140	0.822	-174	2.980	78	0.039	13	0.788	-173
150	0.823	-175	2.826	77	0.039	14	0.788	-173
160	0.824	-175	2.650	76	0.039	14	0.790	-174
170	0.825	-176	2.438	75	0.039	14	0.792	-174
180	0.827	-176	2.325	73	0.039	15	0.793	-174
190	0.829	-177	2.175	72	0.039	16	0.796	-174
200	0.831	-177	2.084	71	0.039	16	0.799	-174
225	0.836	-178	1.824	69	0.039	18	0.805	-174
250	0.846	-178	1.621	66	0.039	21	0.816	-174
275	0.853	-179	1.462	64	0.039	23	0.822	-174
300	0.853	-179	1.319	61	0.040	25	0.833	-174
325	0.856	-179	1.194	59	0.040	27	0.828	-174
350	0.857	+179	1.089	56	0.040	30	0.842	-174
375	0.861	+179	1.014	54	0.042	32	0.849	-174
400	0.865	+178	0.927	51	0.043	35	0.856	-174
425	0.875	+178	0.876	49	0.045	37	0.866	-174
450	0.881	+178	0.810	46	0.046	40	0.870	-174
475	0.886	+177	0.755	44	0.046	43	0.875	-174
500	0.887	+177	0.694	41	0.051	43	0.888	-174
525	0.888	+176	0.677	39	0.052	43	0.890	-174
550	0.896	+176	0.625	36	0.055	45	0.898	-174
575	0.907	+175	0.603	34	0.058	45	0.913	-174
600	0.910	+175	0.585	32	0.061	45	0.918	-174
625	0.910	+174	0.563	30	0.065	45	0.945	-174
650	0.920	+174	0.543	28	0.069	46	0.952	-174
675	0.938	+173	0.533	26	0.074	47	0.974	-174
700	0.943	+171	0.515	24	0.078	47	0.958	-176
725	0.934	+170	0.491	22	0.079	46	0.953	-177
750	0.940	+170	0.475	22	0.084	48	0.943	-177
775	0.953	+169	0.477	21	0.090	48	0.957	-177
800	0.959	+168	0.467	17	0.093	48	0.957	-179

Table 1. Common Source Scattering Parameters

50 Ω System

V<sub>DS</sub> = 28 V, I<sub>D</sub> = 0.75 A

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Rev. V2

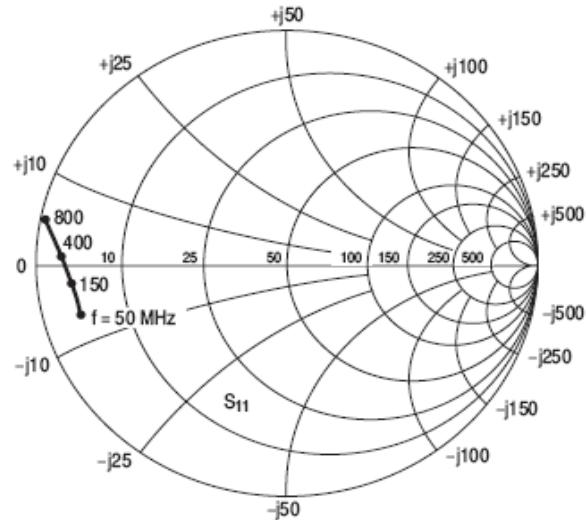


Figure 16.  $S_{11}$ , Input Reflection Coefficient  
versus Frequency  
 $V_{DS} = 28$  V  $I_D = 0.75$  A

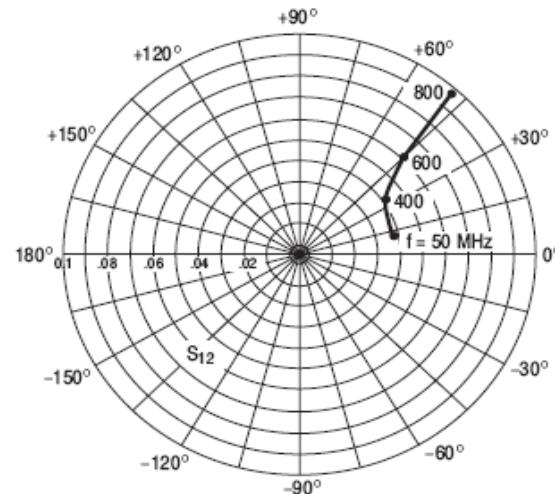


Figure 17.  $S_{12}$ , Reverse Transmission Coefficient  
versus Frequency  
 $V_{DS} = 28$  V  $I_D = 0.75$  A

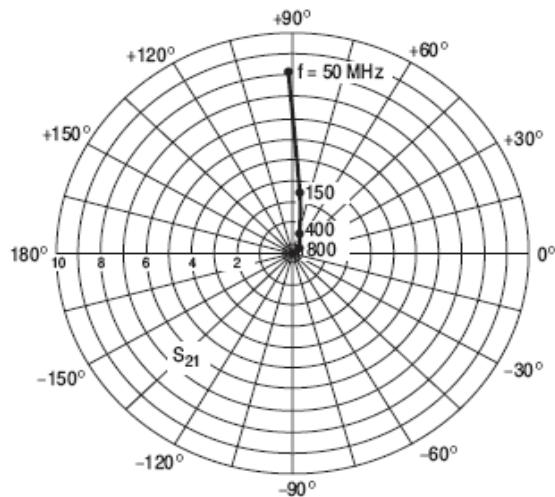


Figure 18.  $S_{21}$ , Forward Transmission Coefficient  
versus Frequency  
 $V_{DS} = 28$  V  $I_D = 0.75$  A

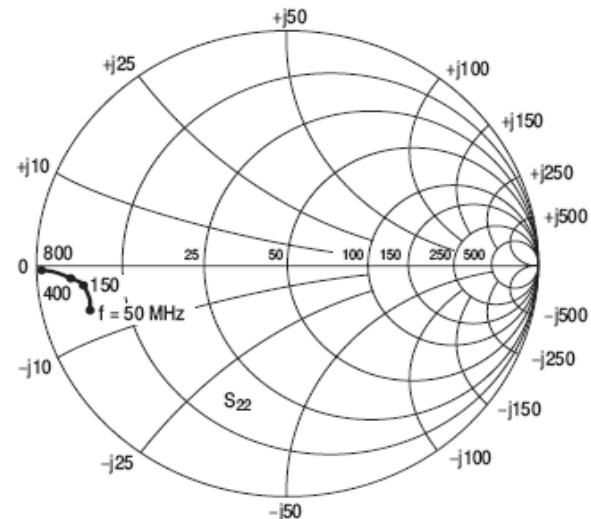


Figure 19.  $S_{22}$ , Output Reflection Coefficient  
versus Frequency  
 $V_{DS} = 28$  V  $I_D = 0.75$  A

### RF POWER MOSFET CONSIDERATIONS

#### DESIGN CONSIDERATIONS

The MRF137 is a RF power N-Channel enhancement-mode field-effect transistor (FET) designed especially for VHF power amplifier applications. M/A-COM RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

#### DC BIAS

The MRF137 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 10 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance.

The value of quiescent drain current ( $IdQ$ ) is not critical for many applications. The MRF137 was characterized at  $IdQ = 25$  mA, which is the suggested minimum value of  $IdQ$ . For special applications such as linear amplification,  $IdQ$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple

resistive divider network. Some special applications may require a more elaborate bias system.

#### GAIN CONTROL

Power output of the MRF137 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 9.)

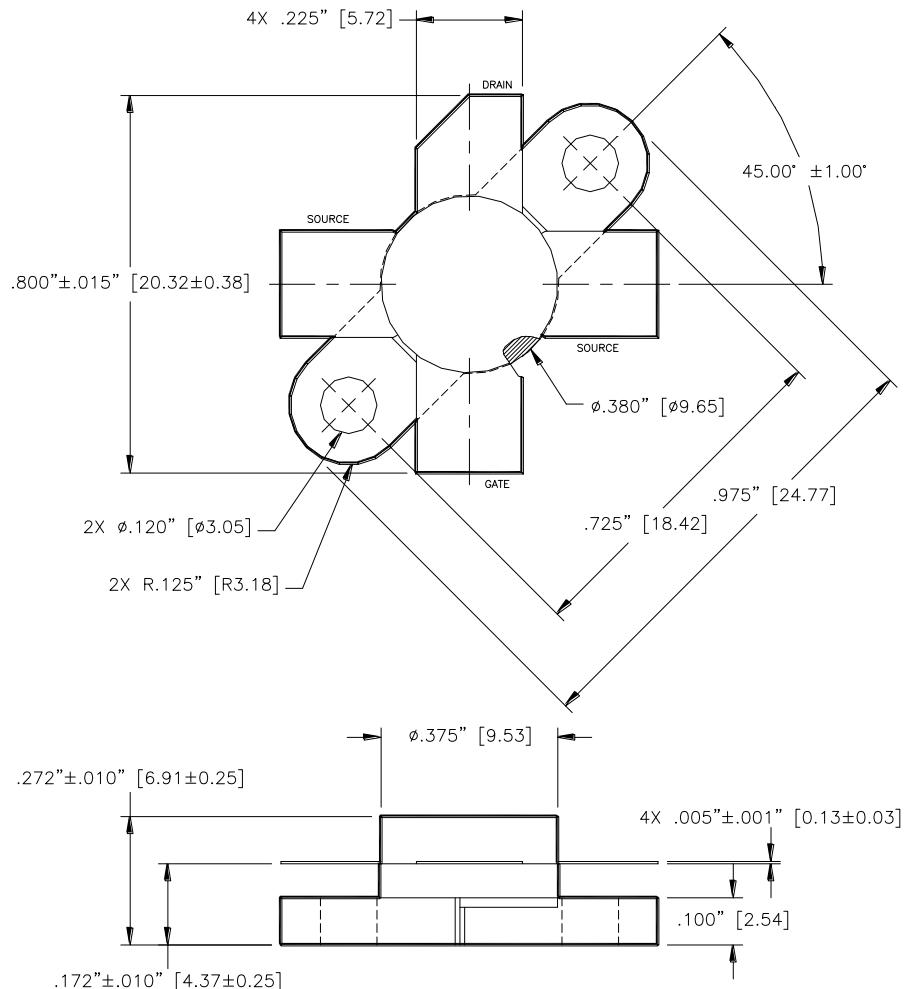
#### AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF137. See M/A-COM Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF137, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF137 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See M/A-COM Application Note AN215A for a discussion of two port network theory and stability.

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Rev. V2



Unless otherwise noted, tolerances are inches ±.005" [millimeters ±0.13mm]

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