AN-2009 LM3421 SEPIC LED Driver Evaluation Board for Automotive Applications

1 Introduction

This document describes an evaluation board consisting of the LM3421 controller configured as a SEPIC constant current LED driver. It is capable of converting input voltages from 8 V to 18 V and illuminating up to six LEDs with approximately 350 mA of drive current.

Additional features include analog and pulse-width modulated (PWM) dimming, over-voltage protection, under-voltage lock-out and cycle-by-cycle current limit.

A bill of materials is included that describes the parts used in this evaluation board. A schematic and layout have also been included along with measured performance characteristics.

2 Key Features

- Designed to CISPR-25, Class 3 limits
- 0 V to 10 V analog dimming function
- PWM dimming function
- Input under-voltage protection
- Over-voltage protection
- Cycle-by-cycle current limit
- NoPB and RoHS compliant bill of materials

3 Applications

- Emergency lighting modules
- LED light-bars, beacons and strobe lights
- Automotive tail-light modules

4 Performance Specifications

Based on an LED, V_f = 3.15 V.

Symbol	Parameter	Min	Typ	Max
V_{IN}	Operating Input Supply Voltage	8	12	18
$V_{IN(MAX)}$	Input Supply Voltage Surge Voltage	-	50 V	-
V_{OUT}	LED String Voltage	-	18.9 V (6 LEDs)	-
I_{LED}	LED String Average Current	-	345 mA	-
-	Efficiency (V_{IN}=12 V, I_{LED}=345 mA, 6 LEDs)	-	85.4%	
f_{SW}	Switching Frequency	-	132 kHz	-
-	LED Current Regulation	-	< 1% Variation	
I_{LIMIT}	Current Limit	-	2.5 A	-
V_{UVLO}	Input Undervoltage Lock-out Threshold (V_{IN} Rising)	-	7.2 V	-
$V_{UVLO(HYS)}$	Input Undervoltage Lock-out Hysteresis	-	1 V	-
V_{OVP}	Output Over-Voltage Protection Threshold	-	37 V	-
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis	-	3.5 V	-

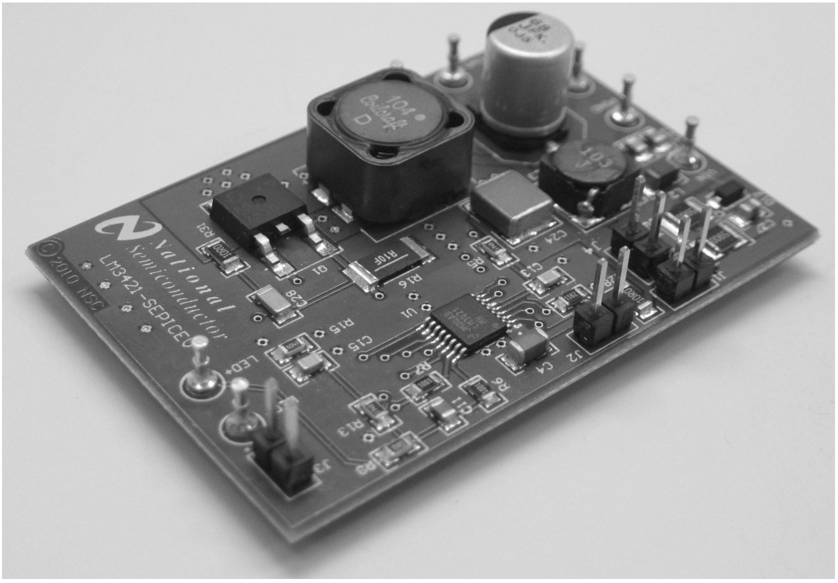


Figure 1. Demo Board

5 General Information

This evaluation board uses the LM3421 controller configured as a SEPIC converter for use in automotive based LED lighting modules. The described circuit can also be used as a general starting point for designs requiring robust performance in EMI sensitive environments.

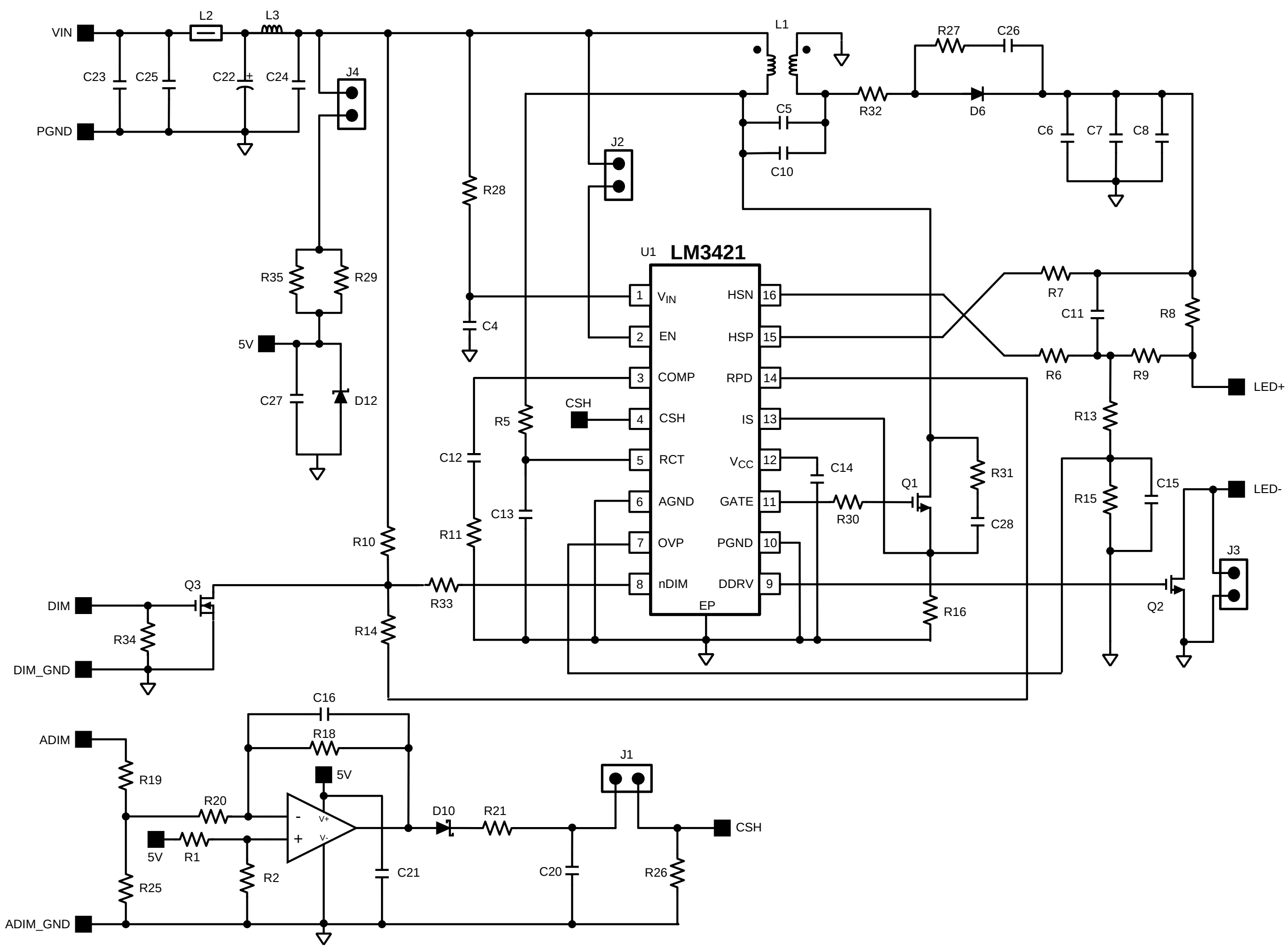
The design is based on the LM3421 controller integrated circuit (IC). Inherent to the LM3421 design is an adjustable high-side current sense voltage that allows for tight regulation of the LED current with the highest efficiency possible. Additional features include analog dimming, over-voltage protection, under-voltage lock-out and cycle-by-cycle current limit.

The operating input voltage range is from 8 V to 18 V. The design, however, is able to withstand input voltages up to 50 V to account for power surges and load dump situations. . Up to six LEDs can be powered with approximately 350 mA of current, which is sufficient to drive a variety of available high brightness (HB) LEDs on the market.

In order to comply with EMI requirements for automotive applications, an input filter and snubber components have also been designed into the circuit. This minimizes the time needed to optimize the design for specific EMI qualifications pertaining to individual automobile manufacturers and ensures faster product time to market.

The demo board consists of a 1.6” x 2.4” four-layer printed circuit board (PCB). Test terminals in the form of turrets are available to connect the input power supply and an LED string as well as apply an analog or PWM dimming signal.

[1][2]6 Demo Board Schematic



(1) Although this evaluation board can be used as a reference design for automotive applications, it is up to you to verify and qualify that the final design and Bill of Materials (BOM) meets any AECQ-100 requirements.

(2) The Analog dimming circuit must not be connected when applying surge voltages greater than 21 V.

7 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

Designator	Value	Package	Description	Manufacturer	Part Number
C4	1.0 µF	1206	Ceramic, C Series, 100 V, 20%	TDK	C3216X7R2A105M
C5	-	-	DNP	-	-
C6	10 µF	2220	CAP, CERM, 50 V, +/-10%, X7R	TDK	C5750X7R1H106K
C7	10 µF	2220	CAP, CERM, 50 V, +/-10%, X7R	TDK	C5750X7R1H106K
C8	0.10 µF	805	Ceramic, X7R, 100 V, 10%	TDK	C2012X7R2A104K
C10	4.7 µF	2220	Ceramic, X7R, 100 V, 10%	MuRata	GRM55ER72A475KA01L
C11	0.10 µF	805	Ceramic, X7R, 50 V, 10%	Yageo America	CC0805KRX7R9BB104
C12	0.22 µF	805	Ceramic, X7R, 50 V, 10%	TDK	C2012X7R1H224K
C13	1000 pF	805	Ceramic, C0G/NP0, 50 V, 1%	AVX	08055A102FAT2A
C14	2.2 µF	805	Ceramic, X5R, 16 V, 10%	AVX	0805YD225KAT2A
C15	47 pF	805	Ceramic, C0G/NP0, 50 V, 5%	MuRata	GQM2195C1H470JB01D
C16	0.1 µF	805	Ceramic, X7R, 25 V, 10%	MuRata	GRM21BR71E104KA01L
C20	1.0 µF	805	Ceramic, X7R, 25 V, 10%	MuRata	GRM216R61E105KA12D
C21	1.0 uF	805	Ceramic, X5R, 25 V, 10%	MuRata	GRM216R61E105KA12D
C22	68 µF	Radial Can - SMD	CAP ELECT 68UF 63 V FK	Panasonic	EEE-FK1J680UP
C23	0.01 µF	805	CAP, CERM, 100 V, +/-10%, X7R	TDK	C2012X7R2A103K
C24	4.7 µF	2220	CAP, CERM, 100 V, +/-10%, X7R	TDK	C5750X7R2A475K
C25	1000 pF	805	CAP, CERM, 100 V, +/-10%, X7R	TDK	C2012X7R2A102K
C26	1.2 nF	1206	CAP, CERM, 100 V, +/-20%, X7R	AVX	12061A122JAT2A
C27	0.10 µF	805	Ceramic, X7R, 25 V, 10%	TDK	C2012X7R1E104K
C28	2.7 nF	1206	CAP, CERM, 100 V, +/-20%, X7R	AVX	12065C272KAT2A
D6	-	SOD-123	Diode Schottky, 60 V, 1A	RΩ	RB160M-60TR
D10	-	SOD-123	Vr = 100 V, Io = 0.15A, Vf = 1.25 V	Diodes Inc.	1N4148W-7-F
D12	-	SOD-123	SMT Zener Diode	Diodes Inc.	MMSZ5231B-7-F
J1	-	Through hole	Header, 100mil, 1x2, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S
J2	-	Through hole	Header, 100mil, 1x2, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S
J3	-	Through hole	Header, 100mil, 1x2, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S
J4	-	Through hole	Header, 100mil, 1x2, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S
L1	100 µH	SMD	Coupled inductor	Coilcraft	MSD1278-104ML
L2	-	1206	6A Ferrite Bead, 160 Ω @ 100 MHz	Steward	HI1206T161R-10
L3	10 µH	SMD	Inductor, Shielded Drum Core, Ferrite, 2.1A, 0.038Ω	Coilcraft	MSS7341-103MLB
Q1	-	DPAK	MOSFET N-CH 100 V 6.2A	Fairchild Semiconductor	FDD3860
Q2	-	SOT-23	MOSFET, N-CH, 30 V, 4.5A	Vishay-Siliconix	SI2316BDS-T1-E3
Q3	-	SOT-23	MOSFET, N-CH, 60 V, 0.24A	Vishay-Siliconix	2N7002E-T1-E3
R1	40.2 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080540K2FKEA
R2	40.2 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080540K2FKEA
R5	174 kΩ	805	1%, 0.125W	Panasonic	ERJ-6ENF1743V
R6	1.0 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW08051k00FKEA
R7	1.0 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW08051k00FKEA
R8	0.2 Ω	2010	1%, 0.5W	Vishay-Dale	WSL2010R3000FEA
R9	10 Ω	805	1%, 0.125W	Yageo America	RC0805FR-0710RL

Table 1. Bill of Materials (BOM) (continued)

Designator	Value	Package	Description	Manufacturer	Part Number
R10	21.5 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080521K5FKEA
R11	100 Ω	805	5%, 0.125W	Vishay-Dale	CRCW0805100RJNEA
R13	174 kΩ	805	1%, 0.125W	Panasonic	ERJ-6ENF1743V
R14	4.32 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW08054K32FKEA
R15	6.04 kΩ	805	1%, 0.125W	Panasonic	ERJ-6ENF6041V
R16	0.10 Ω	2512	1%, 1W	Vishay-Dale	WSL2512R1000FEA
R18	60.4 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080560K4FKEA
R19	40.2 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080540K2FKEA
R20	40.2 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080540K2FKEA
R21	22.1 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080522K1FKEA
R25	40.2 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080540K2FKEA
R26	11.8 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080511K8FKEA
R27	0 Ω	1206	1%, 0.25W	Yageo America	RC1206JR-070RL
R28	10.0 Ω	1206	1%, 0.25W	Vishay-Dale	CRCW120610R0FKEA
R29	590 Ω	1210	1%, 0.5W	Vishay/Dale	CRCW1210590RFEA
R30	10 Ω	805	1%, 0.125W	Vishay-Dale	CRCW080510R0FKEA
R31	2.2 Ω	1206	1%, 0.25W	Vishay-Dale	CRCW12062R20FKEA
R32	0 Ω	1206	5%, 0.25W	Yageo America	RC1206JR-070RL
R33	4.99 kΩ	805	0.1%, 0.125W	Yageo America	RT0805BRD074K99L
R34	10.0 kΩ	805	1%, 0.125W	Vishay-Dale	CRCW080510K0FKEA
R35	590 Ω	1210	1%, 0.5W	Vishay/Dale	CRCW1210590RFEA
TP1 - TP8	-	Through Hole	Terminal, Turret, TH, Double	Keystone Electronics	1573-2
U1	-	HTSSOP-16 EP	N-Channel Controller for Constant Current LED Drivers	Texas Instruments	LM3421
U3	-	SC70-6	2.4 V R-R Out CMOS Video OpAmp with Shutdown	Texas Instruments	LMH6601

8 LM3421 Device Pin-Out

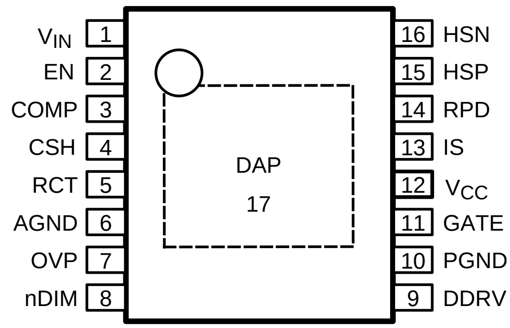


Figure 2. Pin Description 16-Lead HTSSOP EP (Top View)

Table 2. Pin Descriptions

Pin No	Name	Description
1	V_{IN}	Bypass with 100 nF capacitor to AGND as close to the device as possible in the circuit board layout.
2	EN	Connect to AGND for zero current shutdown or apply > 2.4 V to enable device.
3	COMP	Connect a capacitor to AGND to set the compensation.
4	CSH	Connect a resistor to AGND to set the signal current. For analog dimming, connect a controlled current source or a potentiometer to AGND as detailed in Section 13.3.
5	RCT	External RC network sets the predictive “off-time” and thus the switching frequency.
6	AGND	Connect to PGND through the DAP copper pad to provide ground return for CSH, COMP, RCT, and TIMR.
7	OVP	Connect to a resistor divider from V_O to program output over-voltage lockout (OVLO). Turn-off threshold is 1.24 V and hysteresis for turn-on is provided by 23 µA current source.
8	nDIM	Connect a PWM signal for dimming as detailed in the Section 13.4 and/or a resistor divider from V_{IN} to program input under-voltage lockout (UVLO). Turn-on threshold is 1.24 V and hysteresis for turn-off is provided by 23 µA current source.
9	DDRV	Connect to the gate of the dimming MosFET.
10	PGND	Connect to AGND through the DAP copper pad to provide ground return for GATE and DDRV.
11	GATE	Connect to the gate of the main switching MosFET.
12	V_{CC}	Bypass with 2.2 µF–3.3 µF ceramic capacitor to PGND.
13	IS	Connect to the drain of the main N-channel MosFET switch for $R_{DS\text{-}ON}$ sensing or to a sense resistor installed in the source of the same device.
14	RPD	Connect the low side of all external resistor dividers (V_{IN} UVLO, OVP) to implement “zero-current” shutdown.
15	HSP	Connect through a series resistor to the positive side of the LED current sense resistor.
16	HSN	Connect through a series resistor to the negative side of the LED current sense resistor.
EP (17)	EP	Star ground connecting AGND and PGND.

9 Evaluation Board Connection Overview

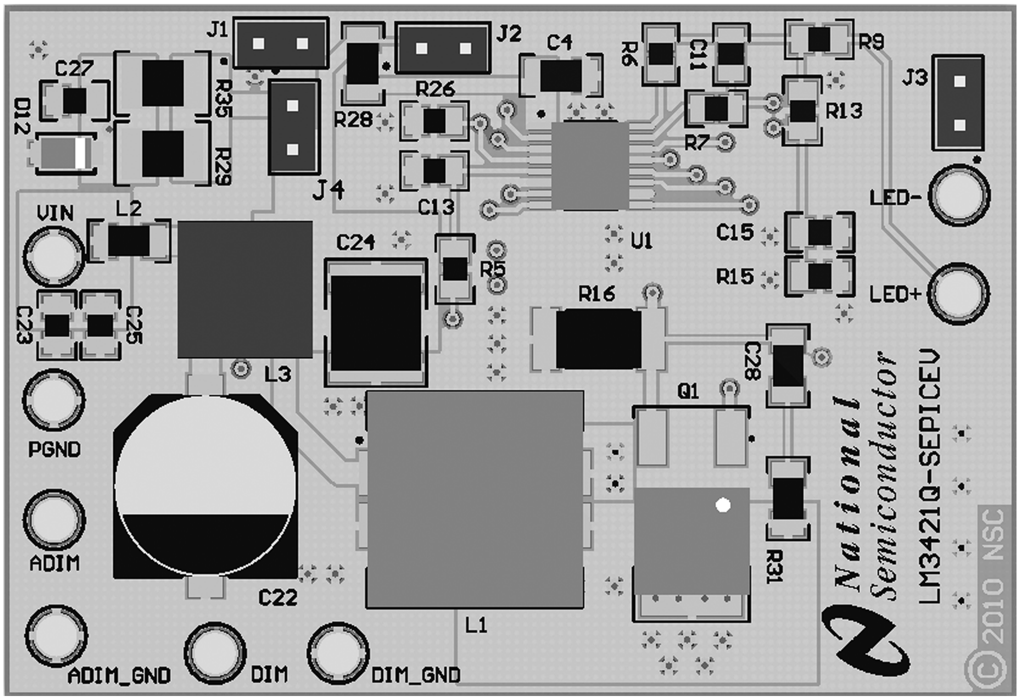


Figure 3. Wiring and Jumper Connection Diagram

Name	I/O	Description
V_{IN}	Input	Power supply voltage.
PGND	Input	Ground.
DIM	Input	PWM Dimming Input Apply a pulse-width modulated dimming voltage signal with varying duty cycle. Maximum dimming voltage level is 20 V. Maximum dimming frequency is 1 kHz.
DIM_GND	Input	PWM dimming ground.
ADIM	Input	**0 V - 10 V Dimming Input** Apply a 0 V - 10 V analog dimming voltage signal. For more details, see Section 13.
ADIM_GND	Input	Analog dimming ground.
LED+	Output	**LED Constant Current Supply** Supplies voltage and constant-current to anode of LED array.
LED-	Output	**LED Return Connection (not GND)** Connects to cathode of LED array. Do NOT connect to GND.

10 Evaluation Board Modes of Operation Overview

The available modes of operation for this evaluation board are enabled utilizing the jumper configurations described in Table 3.

Table 3. Modes of Operation

J1	J2	J3	J4	Mode of Operation
-	OPEN	-	-	LM3421 is disabled and placed into low-power shutdown.
OPEN	CLOSED	CLOSED	OPEN	LM3421 is enabled and powered on. The evaluation board will now run under standard operation.
CLOSED	CLOSED	CLOSED	CLOSED	LM3421 is enabled and powered on. The analog dimming function is now enabled.
OPEN	CLOSED	OPEN	OPEN	LM3421 is enabled and powered on. The PWM dimming function is now enabled.

11 Typical Performance Characteristics

T_A = 25°C and LED V_f = 3.15 V, unless otherwise specified.

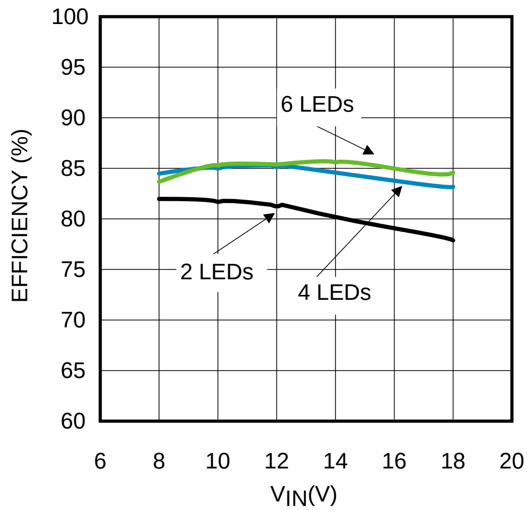


Figure 4. Efficiency vs. Input Voltage
f_{SW} = 132 kHz, I_{LED} = 345 mA

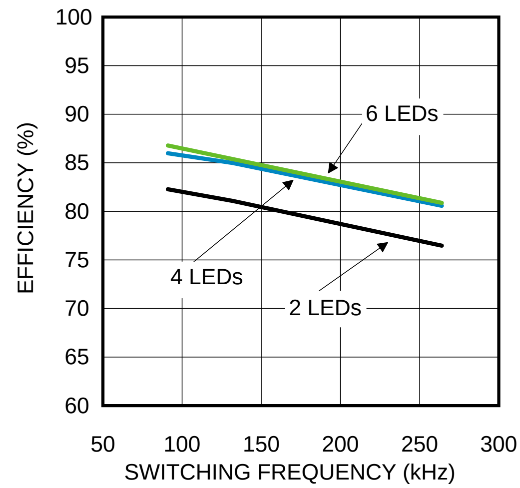


Figure 5. Efficiency vs. Switching Frequency
V_{IN} = 12 V, I_{LED} = 345 mA

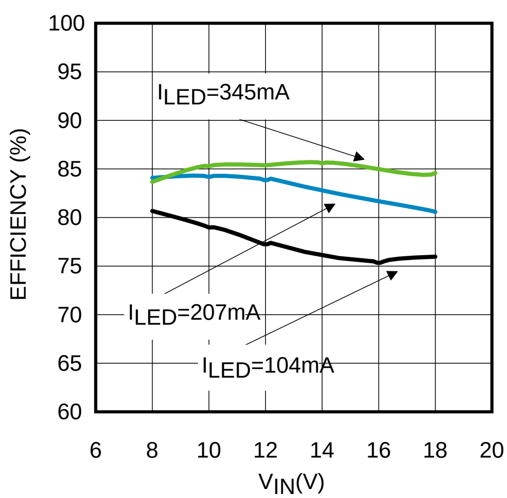


Figure 6. Efficiency vs. Input Voltage
f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 18.8 V

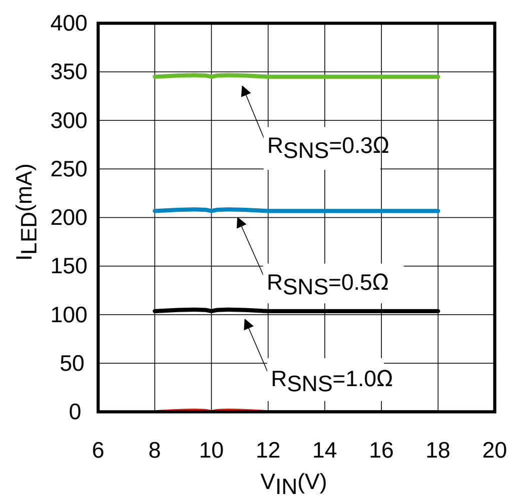


Figure 7. LED Current vs. Input Voltage
f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 18.8 V

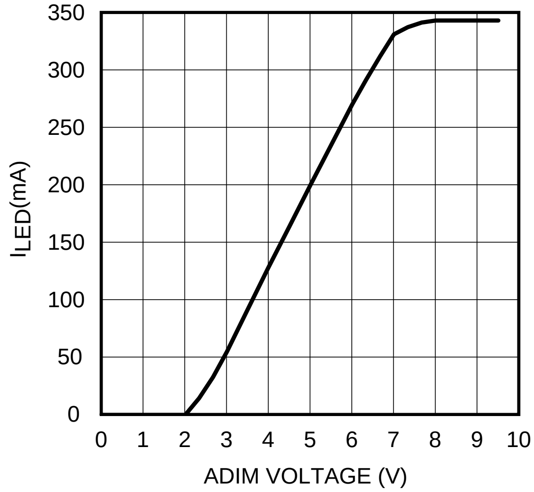


Figure 8. Analog Dimming
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

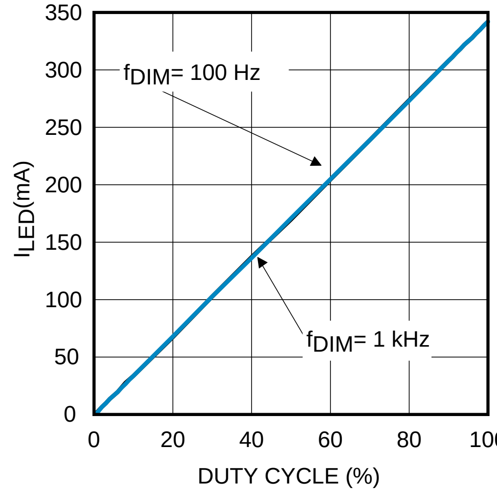


Figure 9. PWM Dimming
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

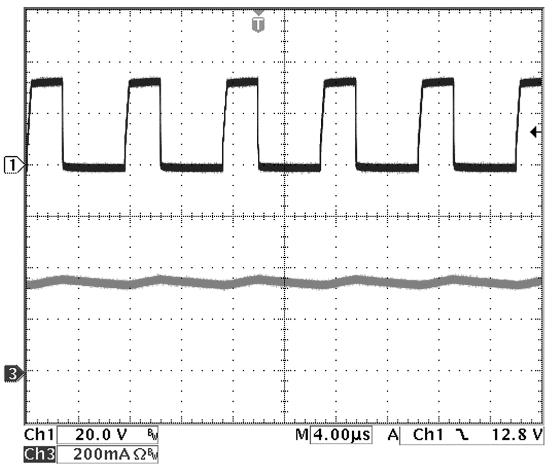


Figure 10. Steady-State Waveforms
Top Plot: V_{SW}, Bottom Plot: I_{LED}
(V_{IN} =12 V, I_{LED} = 342 mA, 6 LEDs, V_{OUT} = 20.4 V)

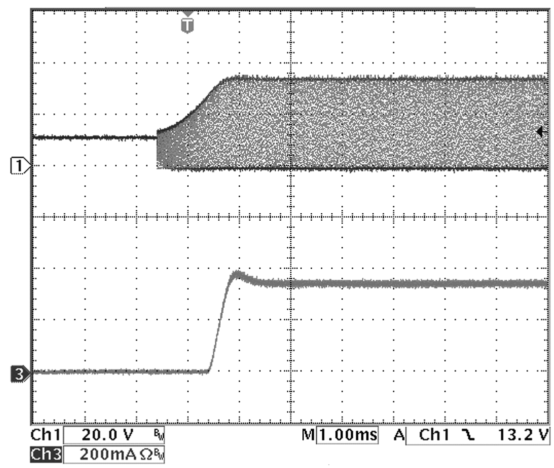


Figure 11. Start-Up Waveforms
Top Plot: V_{SW}, Bottom Plot: I_{LED}
(V_{IN} =12 V, I_{LED} = 342 mA, 6 LEDs, V_{OUT} = 20.4 V)

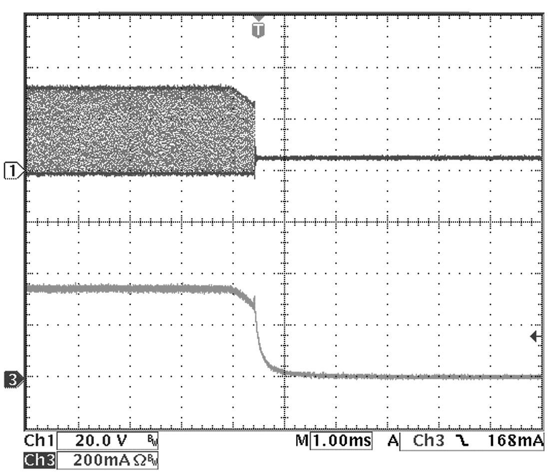


Figure 12. Shutdown Waveforms
Top Plot: V_{SW}, Bottom Plot: I_{LED}
(V_{IN} =12 V, I_{LED} = 342 mA, 6 LEDs, V_{OUT} = 20.4 V)

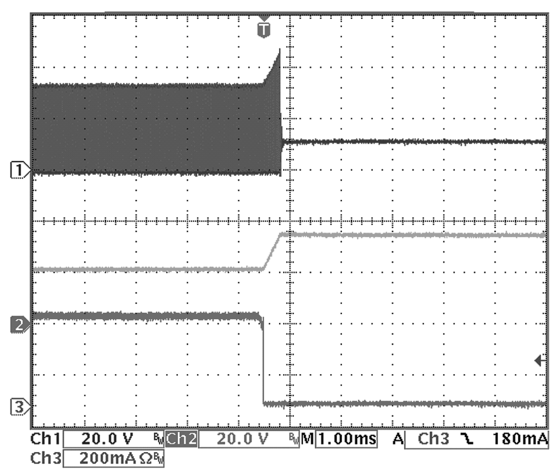


Figure 13. Over-Voltage Protection Response
Top Plot: V_{SW}, Middle Plot: V_{OUT}, Bottom Plot: I_{LED}
(V_{IN} =12 V, I_{LED} = 342 mA, 6 LEDs, V_{OUT} = 20.4 V)

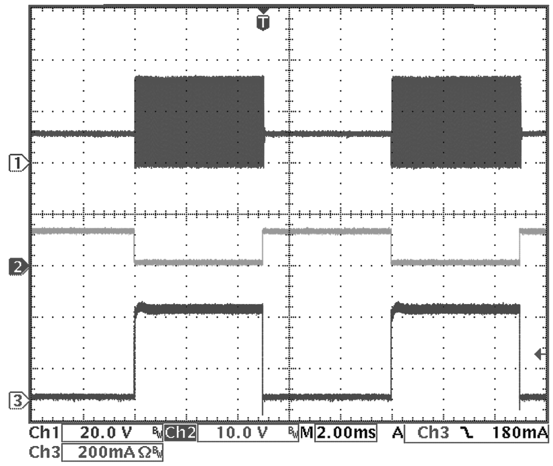


Figure 14. 100Hz, 50% Duty Cycle PWM Dimming
Top Plot: V_{SW}, Middle Plot: V_{DIM}, Bottom Plot: I_{LED}
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

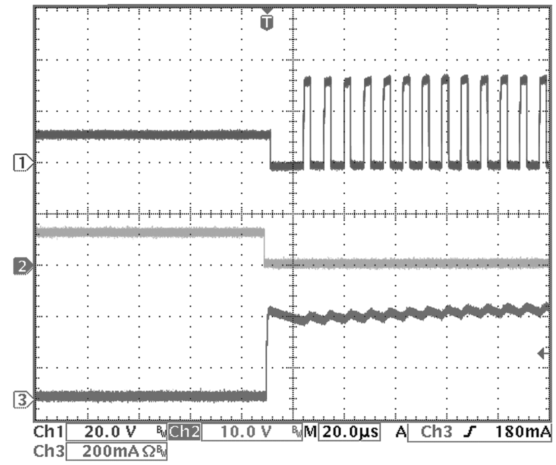


Figure 15. 100Hz, 50% Duty Cycle PWM Dimming (rising edge)
Top Plot: V_{SW}, Middle Plot: V_{DIM}, Bottom Plot: I_{LED}
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

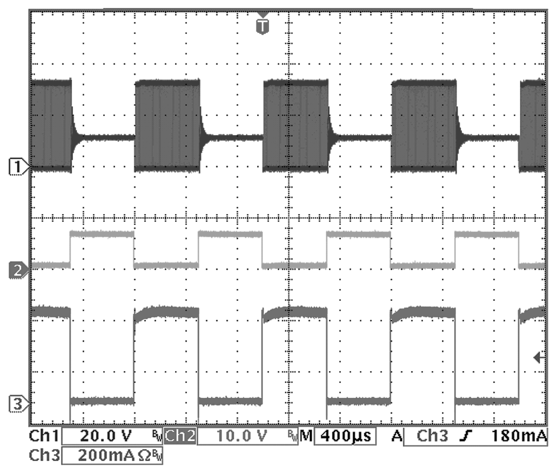


Figure 16. 1 kHz, 50% Duty Cycle PWM Dimming
Top Plot: V_{SW}, Middle Plot: V_{DIM}, Bottom Plot: I_{LED}
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

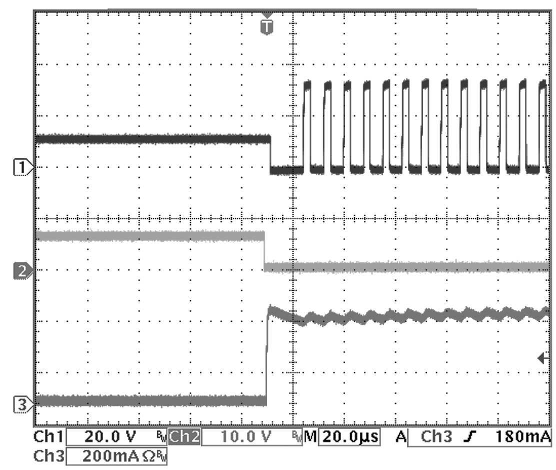


Figure 17. 1 kHz, 50% Duty Cycle PWM Dimming (rising edge)
Top Plot: V_{SW}, Middle Plot: V_{DIM}, Bottom Plot: I_{LED}
V_{IN} = 12 V, f_{SW} = 132 kHz, 6 LEDs, V_{OUT} = 20.4 V

12 PCB Layout

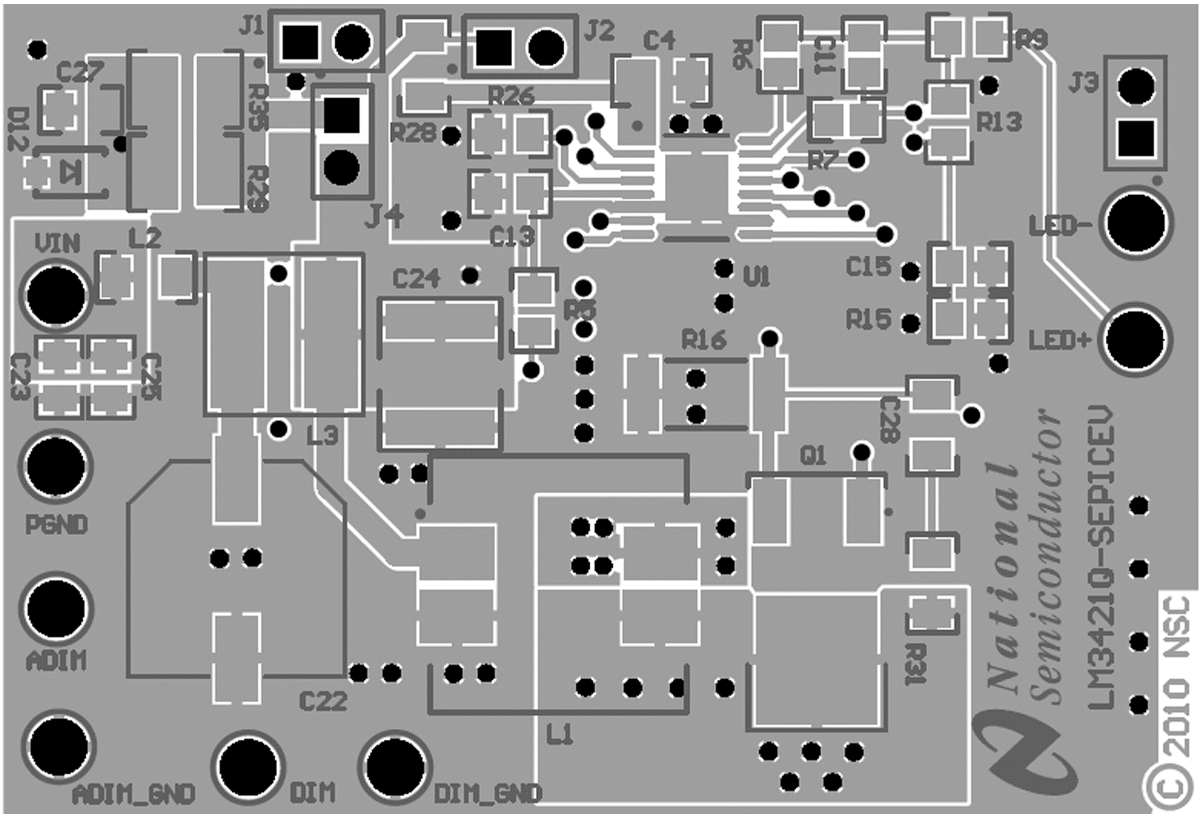


Figure 18. Top Layer

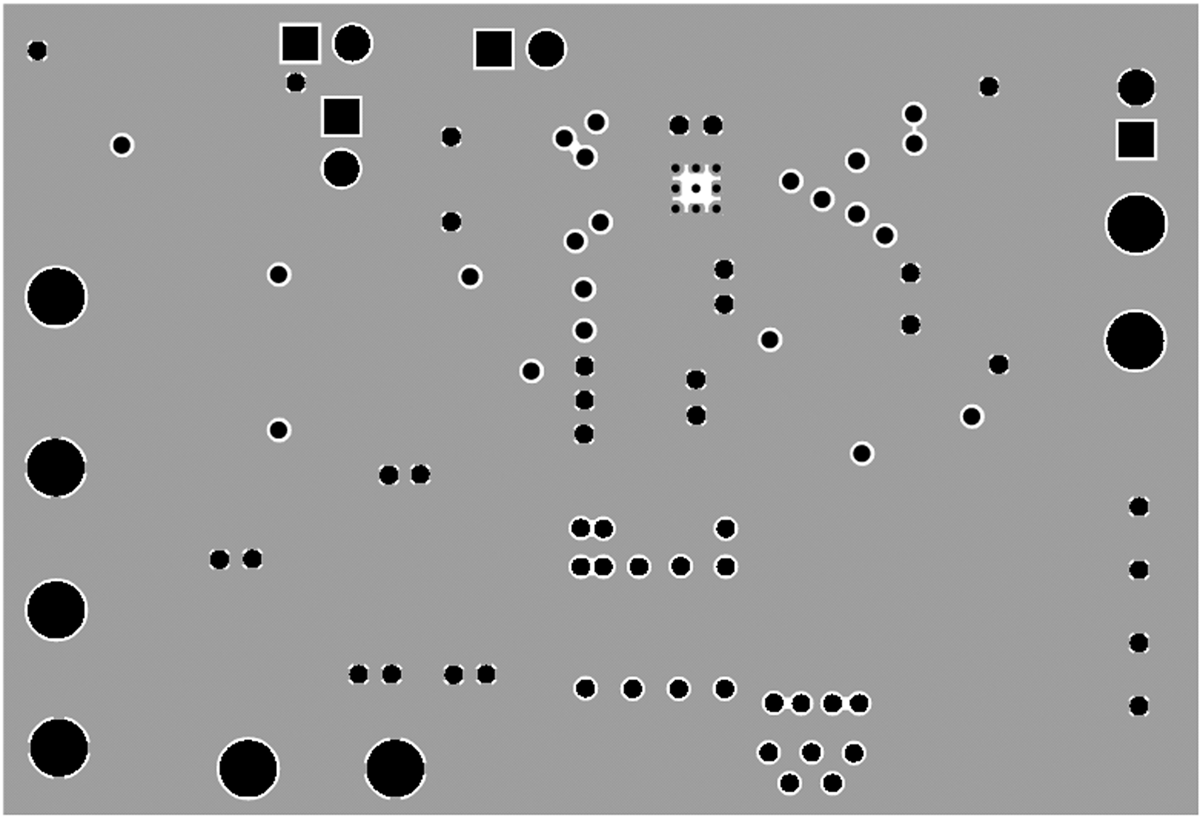


Figure 19. Mid-Layer 1

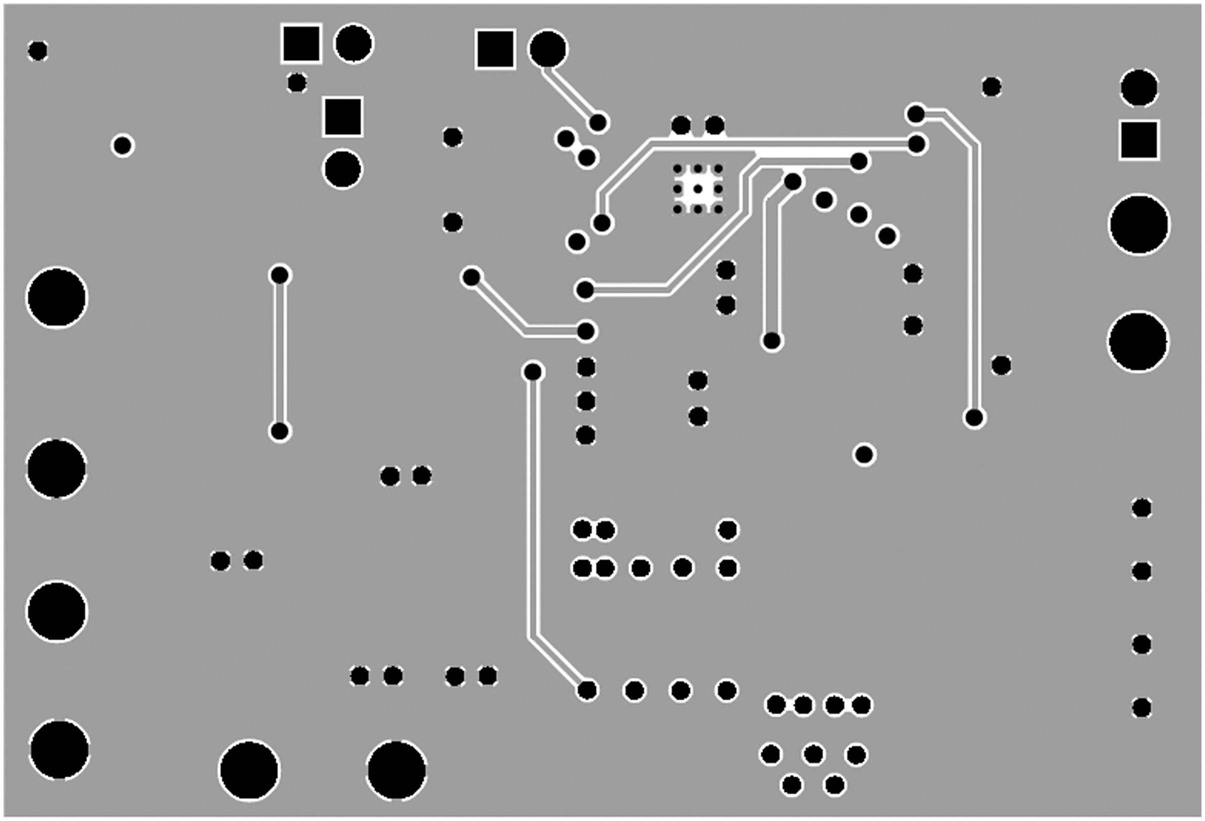


Figure 20. Mid-Layer 2

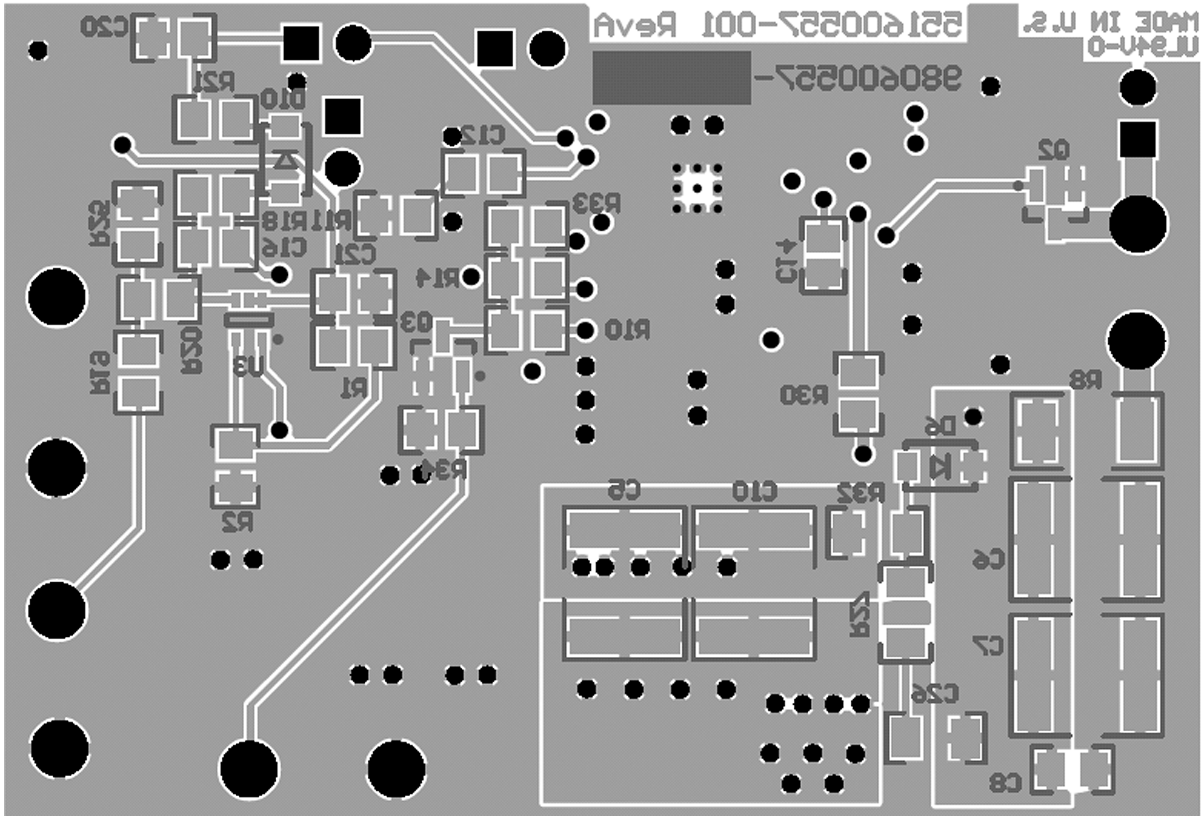


Figure 21. Bottom Layer

13 Theory of Operation

13.1 Input EMI Line Filter

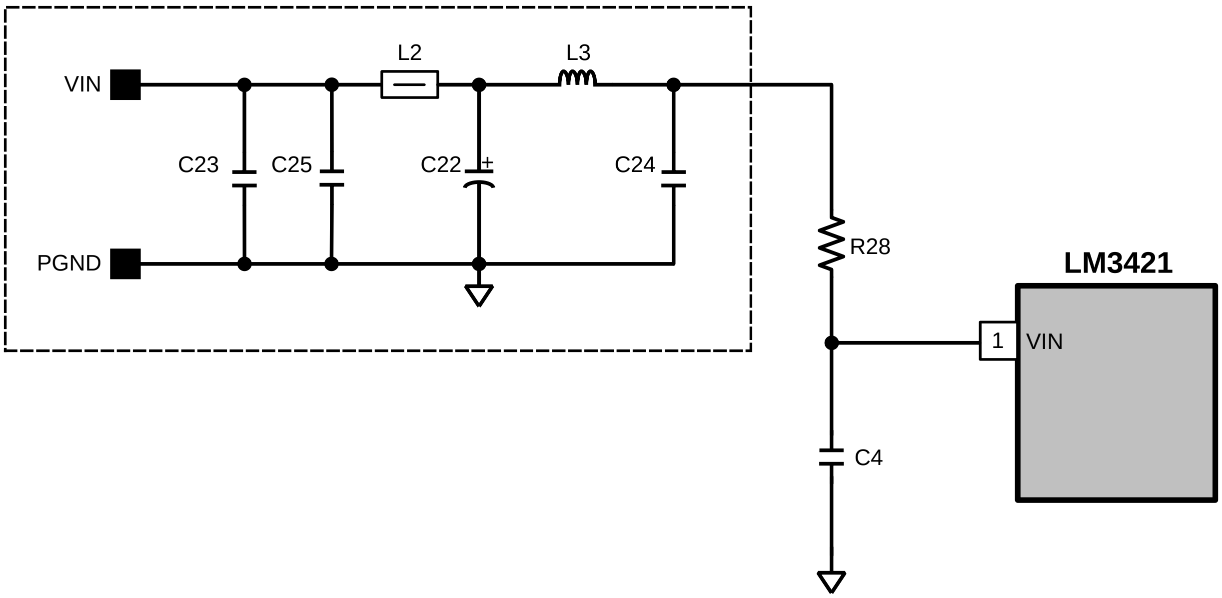


Figure 22. Input Filter Circuit

A low-pass input filter (highlighted in Figure 22) has been added to the front-end of the circuit. Its primary purpose is to minimize EMI conducted from the LM3421 circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the LED driver switching frequency (f_{SW} = 132 kHz) are primarily addressed with this filter. The ferrite bead, L2, has been chosen to help attenuate EMI frequencies above 10 MHz in conjunction with snubber circuitry that has been designed into the driver circuitry, which is discussed in the next section.

This low pass filter has a cut-off frequency that is determined by the inductor and capacitor resonance of L3 and C22 as described in Equation 1:

$$f_0 = \frac{1}{2\pi\sqrt{L3 \times C22}} \tag{1}$$

The input filter needs to attenuate the fundamental frequency and associated harmonics of the demo board's switching frequency, which is designed to be 132 kHz. Plugging the chosen values of L3 and C22 as 10 µH and 68uF respectively gives a roll-off frequency of 6.1 kHz. The ferrite bead chosen has a nominal impedance of 160 Ω at 100 Mhz for 1A of current and will help attenuate higher frequency noise.

Conducted EMI scans of an earlier prototype evaluation board with and without an input filter are shown in Figure 23 and Figure 24.

NOTE: These scans were originally done per CISPR-22, however, for the purpose of evaluating filter performance this EMI data is acceptable. The actual EMI performance for this evaluation board is discussed later in this document.

Frequencies from 300 kHz to 10 MHz show noticeable attenuation of peak frequencies with the input filter in place. Harmonics of the driver switching frequency are reduced up to 22 dBµV/m.

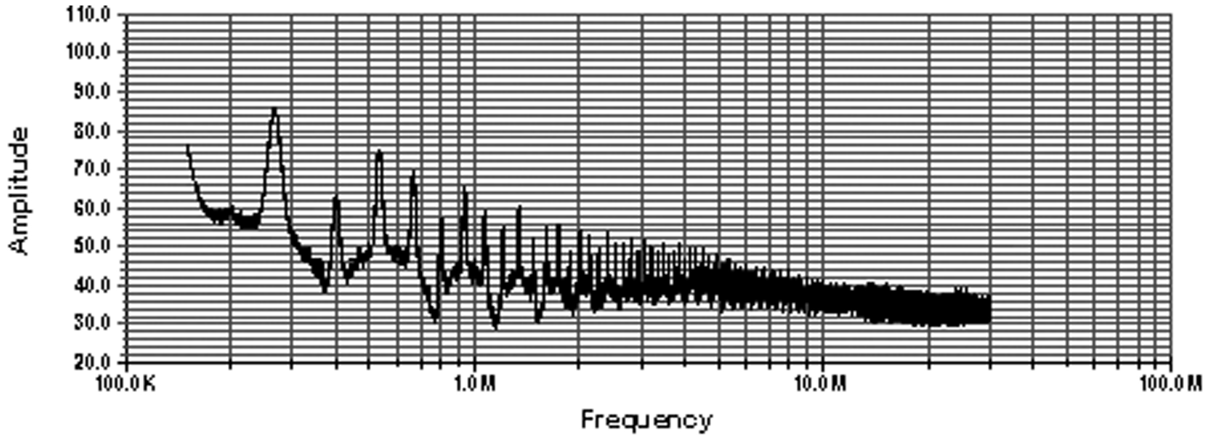


Figure 23. Conducted EMI Scan (peak) WITHOUT Input Filter and With Snubber Circuitry

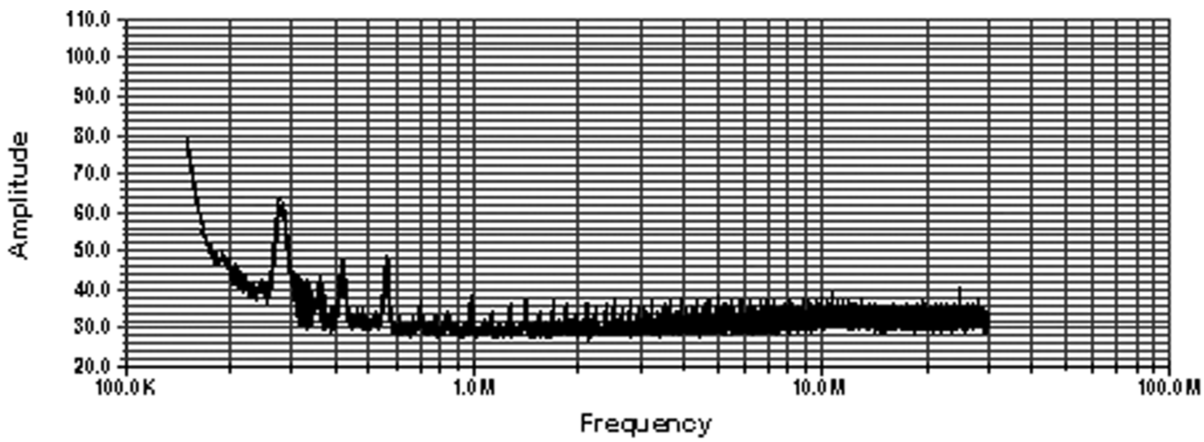


Figure 24. Conducted EMI Scan (peak) WITH Input Filter and With Snubber Circuitry

13.2 Snubber Circuitry

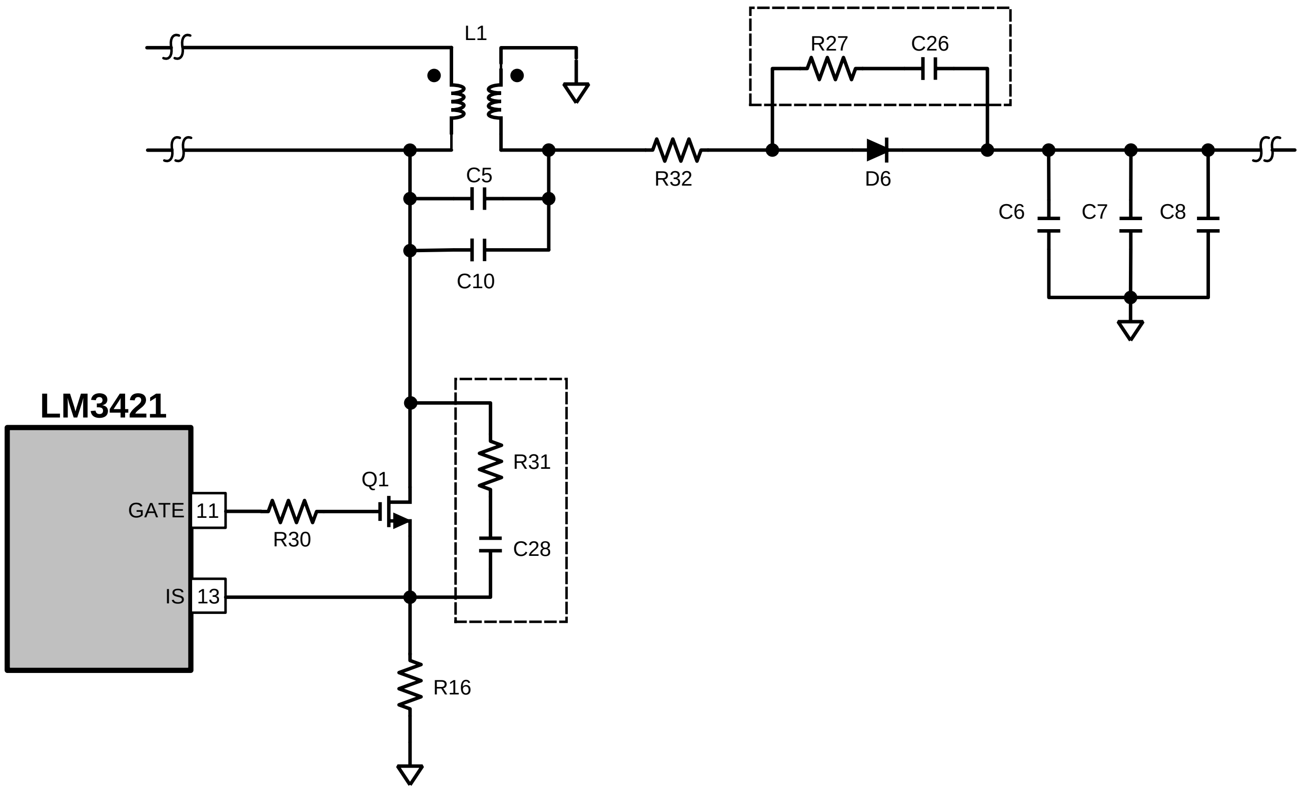


Figure 25. Snubber Circuitry

Snubber circuitry (highlighted in Figure 25 has been added around the switching elements of Q1 and D6 in the form of series resistor-capacitor (RC) pairs. The purpose of these snubbers is to reduce the rising/falling edge rate of the switching voltage waveform when Q1 and D6 transition from an "on" to "off" state and vice versa. This helps reduce both conducted and radiated EMI in the higher test frequency ranges. For lower EMI frequencies particularly during conducted EMI testing, the input filter is utilized as the primary EMI attenuator as previously discussed.

Conducted EMI scans of an earlier prototype evaluation board with and without snubber circuitry are shown in Figure 26 and Figure 27.

NOTE: These scans were originally done per CISPR-22, however, for the purpose of evaluating filter performance this EMI data is acceptable. The actual EMI performance for this evaluation board will be discussed later in this document.

From 10 MHz to 30 MHz, the snubbers reduce peak power for all frequencies with noticeable attenuation of peak power between 20 MHz and 30 MHz.

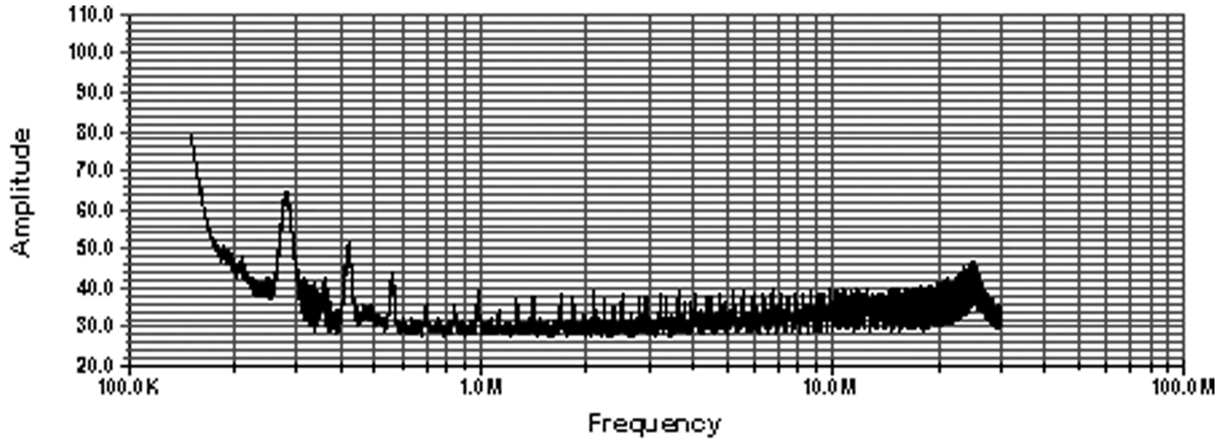


Figure 26. Conducted EMI Scan (peak) With Input Filter and WITHOUT Snubber Circuitry

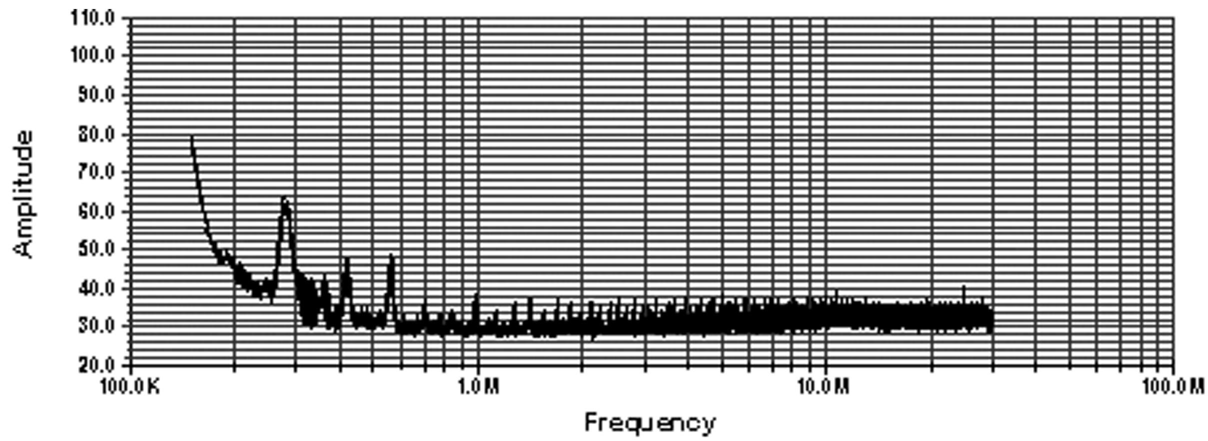


Figure 27. Conducted EMI Scan (peak) With Input Filter and WITH Snubber Circuitry

Radiated EMI scans of the demo board with and without the snubber circuitry are shown in Figure 28 and Figure 29. From 30 MHz to near 200 MHz, the snubbers reduce peak power with attenuation values ranging from 5 to 10 dBµV/m.

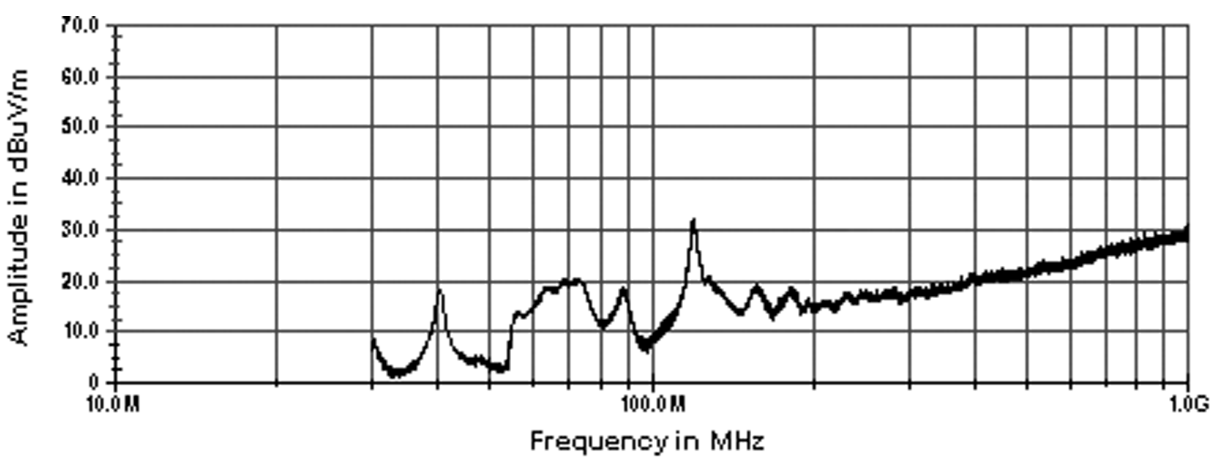


Figure 28. Radiated EMI Scan (peak) With Input Filter and WITHOUT Snubber Circuitry

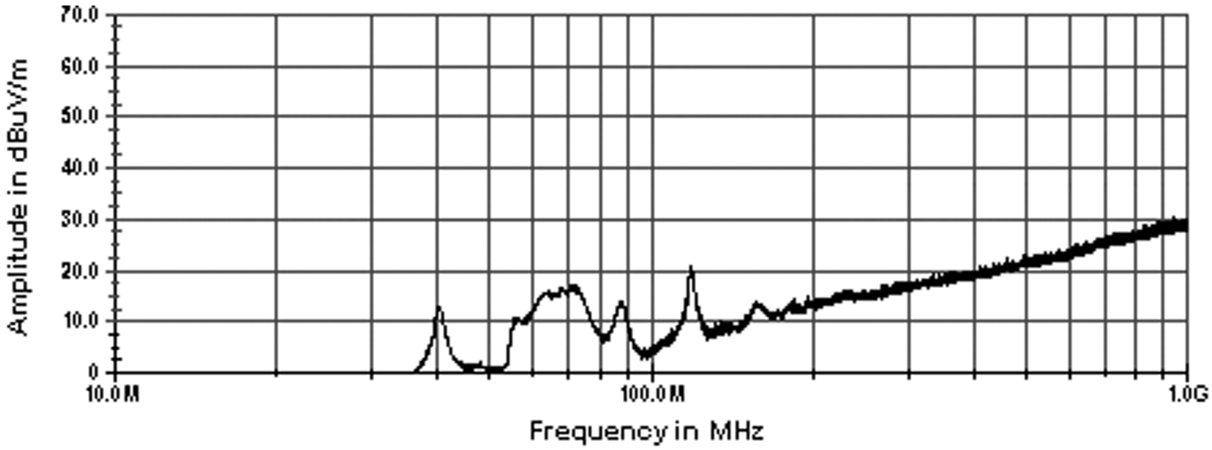


Figure 29. Radiated EMI Scan (peak) With Input Filter and WITH Snubber Circuitry

Although the snubber circuits help reduce the EMI signature of the evaluation board, they do so at the cost of lowering the maximum achievable driver efficiency. Since each board design and application is unique, it is recommended that the user investigate different snubber configurations and values to provide the optimal balance of EMI performance and system efficiency.

13.3 Analog Dimming

The analog dimming circuitry is highlighted in Figure 30. Closing jumpers J1 and J4 connects the analog dimming circuitry to the LED driver and thus enables this feature. Analog dimming of the LED current is performed by adjusting the CSH pin current (I_{CSH}) from the LM3421. The relationship between I_{CSH} and the average LED current is described Equation 2:

$$I_{LED} = \frac{(I_{CSH})(R_{HSP})}{R_{SNS}} \quad (2)$$

For the demo board, R_{HSP} is 1 kΩ and R_{SNS} is 0.3 Ω, so the equation becomes,

$$I_{LED} = \frac{(I_{CSH})(R_{HSP})}{R_{SNS}} = \frac{(I_{CSH})(1\,k\Omega)}{0.3\Omega} \quad (3)$$

When no analog dimming is being applied, the I_{CSH} current is described by Equation 4:

$$I_{CSH} = \frac{1.24V}{R_{CSH}} \quad (4)$$

The value of R_{CSH} is 11.8kΩ and this gives I_{CSH} as 105µA.

The method used to adjust I_{CSH} for analog dimming is with an external variable current source consisting of an on-board op-amp circuit. When a 0 V to 10 V voltage signal is applied to the ADIM test point, the op-amp will adjust its output current accordingly. This output current is sourced into the node consisting of the CSH pin and resistors, R21 and R26, which adjusts the I_{CSH} current from the original 105 µA based on the 0 V to 10 V analog dimming signal. A low analog dimming voltage will source more current into the CSH pin effectively dimming the LEDs while a high analog dim voltage will source less current resulting in less dimming. ADIM should be a precise external voltage reference.

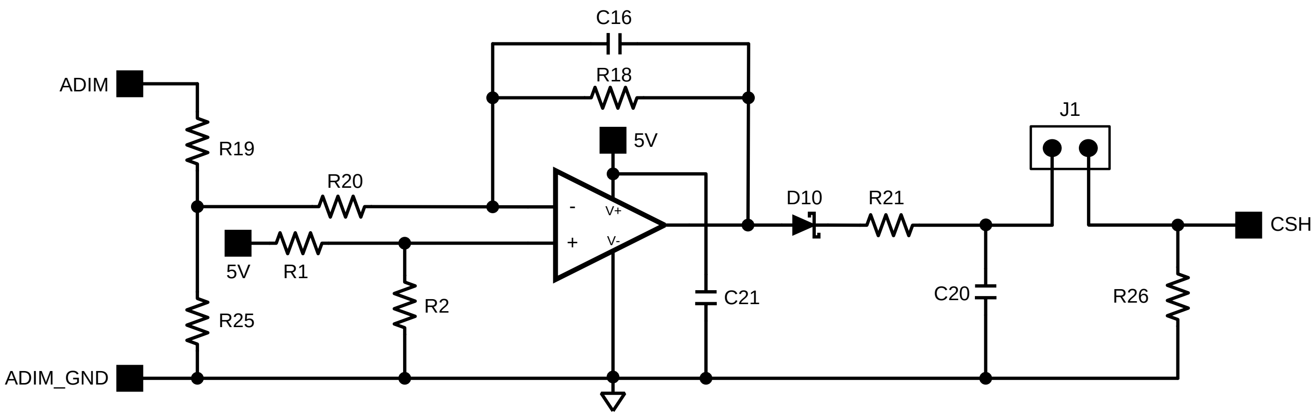


Figure 30. Analog Dimming Circuit

13.4 PWM Dimming

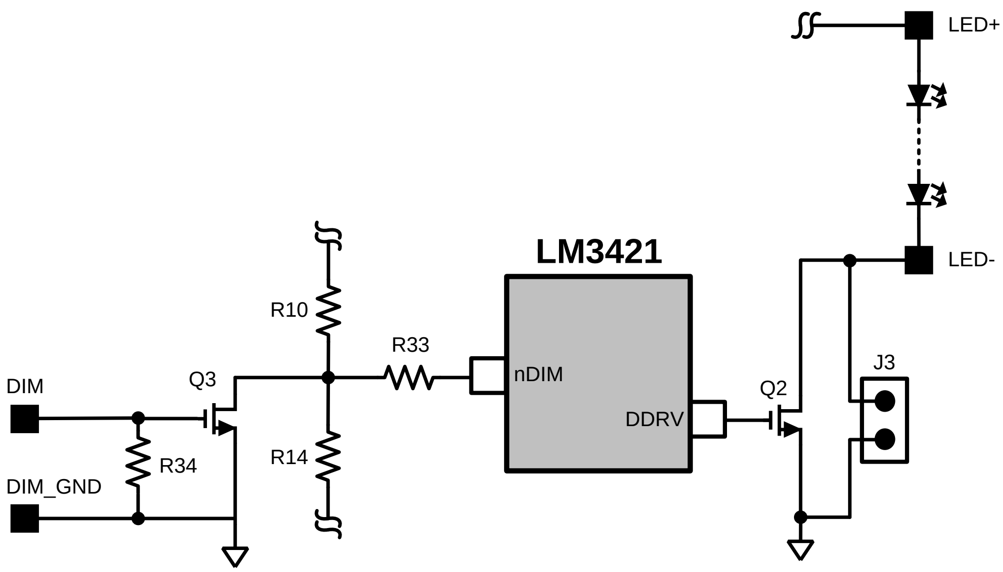


Figure 31. PWM Dimming Circuit

The circuitry associated with pulse-width modulation (PWM) dimming is highlighted in Figure 31 and closing jumper J3 enables this function. A logic-level PWM signal can be applied to the DIM pin which in turn drives the nDIM pin thought the MosFET Q3. A pull down resistor, R34, has also been added to properly turn off, Q3, if no signal is present. The nDIM pin controls the dimming NFET, Q2, which is in series with the LED stack. The brightness of the LEDs can be varied by modulating the duty cycle of the PWM signal. LED brightness is approximately proportional to the PWM signal duty cycle, so for example, 30% duty cycle equals approximately 30% LED brightness.

14 Conducted EMI Analysis

Several automobile manufacturers base their conducted EMI limit requirements on the CISPR-25, Class 3 standard. However, each manufacturer in the end specifies their own individual method for EMI qualification, and so there is not at this time a universally adopted set of EMI limits and performance requirements. This makes it challenging to design a single LED driver circuit to comprehensively meet the EMI requirements for each and every auto manufacturer. Therefore, the Class 3 limits described by CISPR-25 were used as a reference point for the EMI performance of the LM3421 SEPIC design. From this data, specific auto manufacturer EMI limits and requirements can be applied to the data to determine if additional optimization of the reference design is required for compliance.

Conducted EMI tests were performed with a six LED load running 345 mA of LED current with an input power supply voltage of 12 V. In the following EMI scan of Figure 32, the CISPR-25 Class 3 "peak" limits are designated as blue and the "average" limits are designated in green. No enclosure was used around the board. Due to limitations in the data gathering equipment only the peak EMI data from 100 kHz to 30 MHz could be acquired, and so the conducted EMI performance of the evaluation board at other frequencies and versus quasi-peak and average CISPR25 limits can only be roughly interpreted.

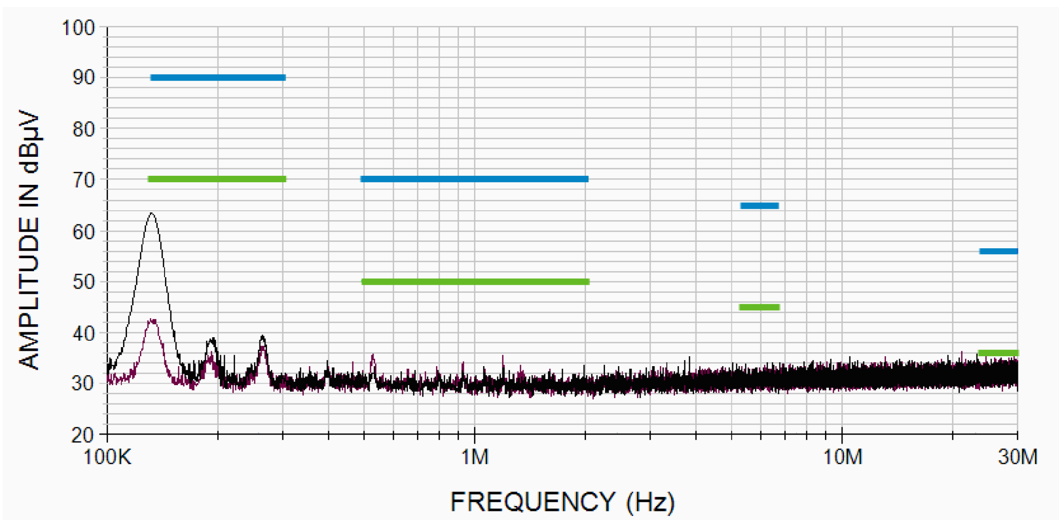


Figure 32. Conducted "Peak" Scan per CISPR-25 With Class 3 Limits

15 Radiated EMI Analysis

Similar to the conducted EMI testing described previously, several automobile manufacturers base their radiated EMI limit requirements on the CISPR-25, Class 3 standard. However, each manufacturer in the end specifies their own individual method for EMI qualification, and so there is not at this time a universally adopted set of EMI limits and performance requirements. This makes it challenging to design a single LED driver circuit to comprehensively meet the EMI requirements for each and every auto manufacturer. Therefore, the Class 3 limits described by CISPR-25 were used as a reference point for the EMI performance of the LM3421 SEPIC design. From this data, specific auto manufacturer EMI limits and requirements can be applied to the data to determine if additional optimization of the reference design is required for compliance.

Radiated EMI tests were performed with a six LED load running 345 mA of LED current with an input power supply voltage of 12 V. No enclosure was used around the board. In the EMI scan of Figure 33, the CISPR-25 Class 3 "peak" limits are shown in blue. For the EMI scan of Figure 34, the CISPR-25 Class 3 "average" limits are shown in green. Some frequency bands have multiple limits associated with them. In these instances, the frequency bands have multiple RF spectrum allocations (for example, FM, CB, VHF, and so forth), and so all applicable limits are being shown even if they overlap. Due to limitations in the data gathering equipment only the peak EMI data from 10 MHz to 1GHz could be acquired, and so the radiated EMI performance of the evaluation board at other frequencies and versus quasi-peak and average CISPR25 limits can only be roughly interpreted.

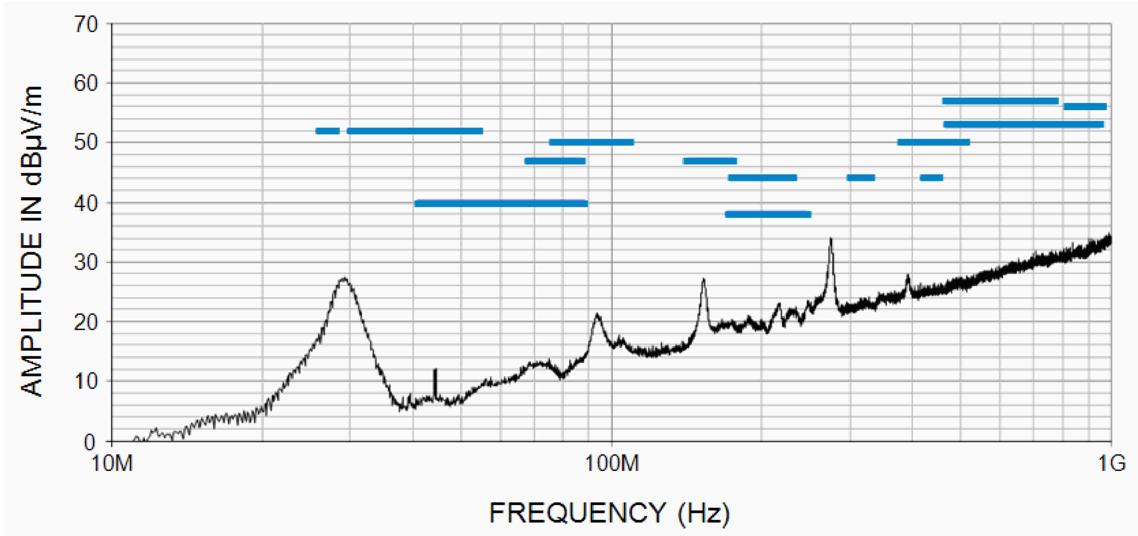


Figure 33. Radiated “Peak” Scan Data per CISPR-25 With Class 3 "Peak" Limits

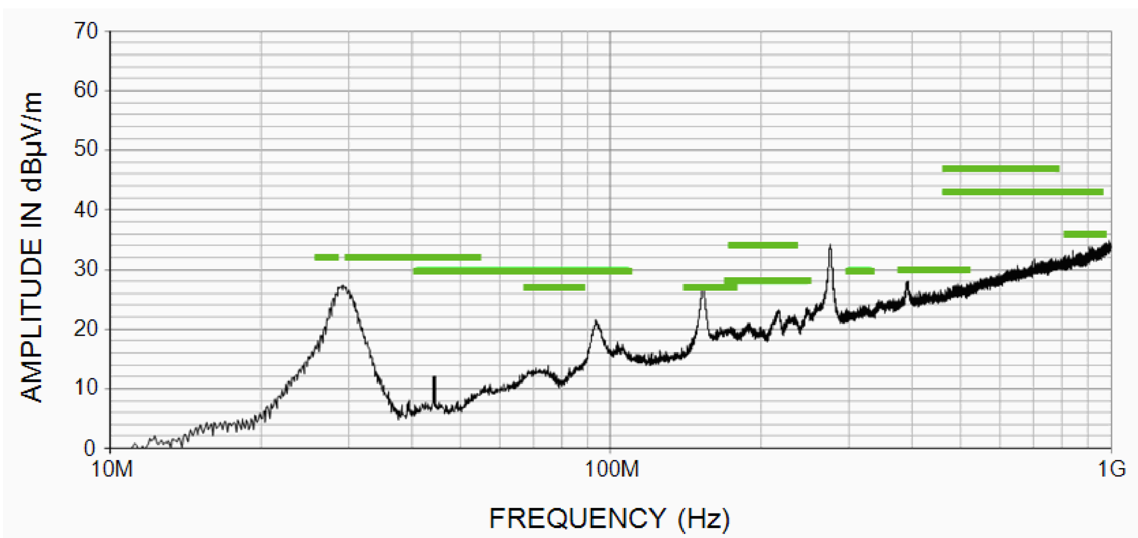


Figure 34. Radiated “Peak” Scan Data per CISPR-25 With Class 3 "Average" Limits

16 Thermal Analysis

Thermal scans were taken of the stand-alone LED demo board at room temperature with no airflow. Primary hot spots on the top and bottom layers are associated with the snubber resistors R27 and R31. Test Conditions: V_{IN} = 12.1 V, I_{IN}=651 mA, V_{OUT} = 20.4 V (6 LEDs), I_{LED} = 336 mA, P_{IN} = 7.88W, P_{OUT} = 6.85W, Efficiency = 86.9%, Time = 75 minutes, T_a = Room temp, No airflow, No enclosure

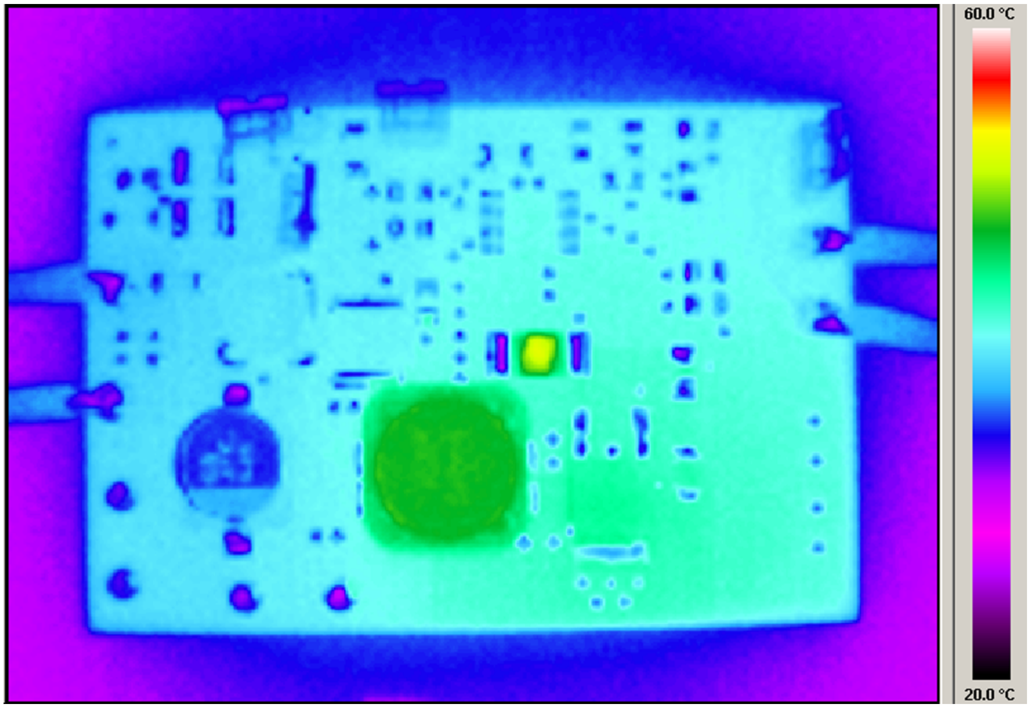


Figure 35. Thermal Scan, Top Layer

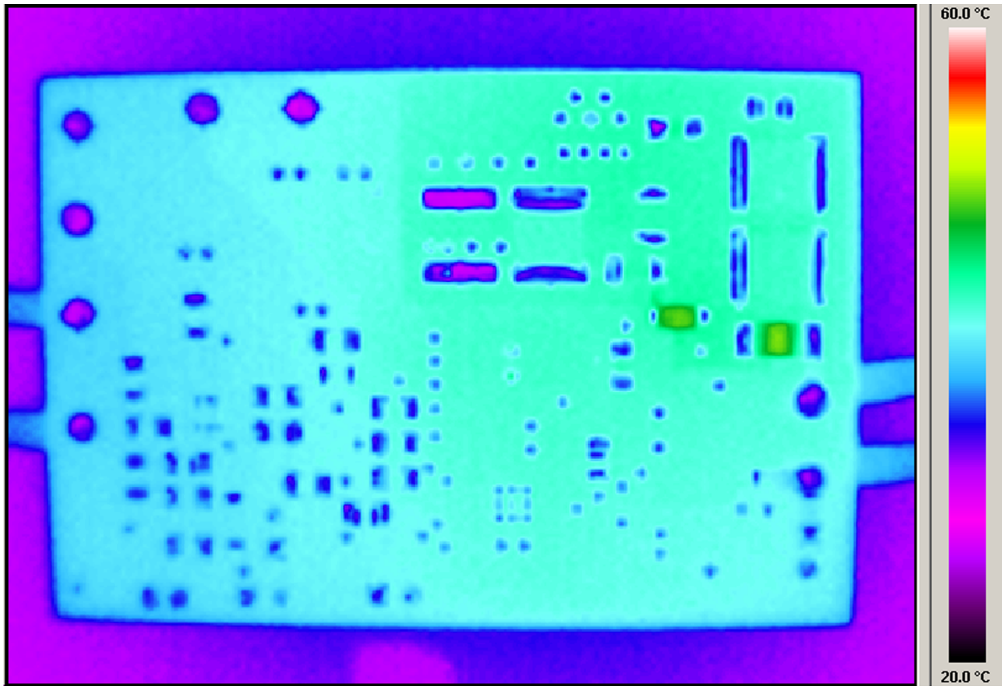


Figure 36. Thermal Scan, Bottom Layer

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