

S18C & S18CH SERIES

400-200 VOLTS RANGE

175 AMP RMS, CENTER AMPLIFYING GATE

PHASE CONTROL TYPE STUD MOUNTED SCRs

VOLTAGE RATINGS

VOLTAGE CODE (1)	$V_{RRM}, V_{DRM} - (V)$ Max. rep. peak reverse and off-state voltage	$V_{RSM} - (V)$ Max. non-rep. peak reverse voltage $t_p \leq 5ms$	NOTES
	$T_J = -40^\circ C$ to max. rated	$T_J = 25^\circ C$ to max. rated	
4A	400	500	Gate open
2A	200	300	

(1) To complete the part number, refer to the Ordering Information table.

MAXIMUM ALLOWABLE RATINGS

PARAMETER	SERIES	VALUE	UNITS	NOTES
T_J Junction temperature	S18C	-40 to 125	$^{\circ}\text{C}$	
	S18CH	-40 to 150		
T_{stg} Storage temperature	ALL	-40 to 150	$^{\circ}\text{C}$	
$I_T(\text{AV})$ Max. av. current	ALL	110	A	180 $^{\circ}$ half sine wave
@ Max. T_C	S18C	80	$^{\circ}\text{C}$	
	S18CH	115		
$I_T(\text{RMS})$ Max. RMS current	ALL	175	A	
I_{TSM} Max. peak non-rep. surge current	ALL	2060	A	50Hz half cycle sine wave Initial $T_J = 125^{\circ}\text{C}$, rated V_{RRM} applied after surge.
		3100		60Hz half cycle sine wave
		3520		50Hz half cycle sine wave Initial $T_J = 125^{\circ}\text{C}$, no voltage applied after surge.
		3690		60Hz half cycle sine wave
I^2t Max. I^2t capability	ALL	44	kA^2s	$t = 10\text{ms}$ Initial $T_J = 125^{\circ}\text{C}$, rated V_{RRM} applied after surge.
		40		$t = 8.3\text{ms}$
		62		$t = 10\text{ms}$ Initial $T_J = 125^{\circ}\text{C}$, no voltage applied after surge.
		57		$t = 8.3\text{ms}$
$I^2\sqrt{t}$ Max. $I^2\sqrt{t}$ capability	ALL	820	$\text{kA}^2\sqrt{\text{s}}$	Initial $T_J = 125^{\circ}\text{C}$, no voltage applied after surge. I^2t for time $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$. $0.1 \leq t_x \leq 10\text{ms}$.
di/dt Max. non-rep. rate-of-rise of current	ALL	800	A/ μs	$T_J = 125^{\circ}\text{C}$, $V_D = V_{\text{DRM}}$, $I_{\text{TH}} = 1600\text{A}$. Gate pulses: 20V, 20n, 10 μs , 0.5 μs rise. Max. repetitive di/dt is approximately 40% of non-repetitive value.
P_{GH} Max. peak gate power	ALL	10	W	$t_p \leq 5\text{ms}$
$P_{\text{G(AV)}}$ Max. av. gate power	ALL	2	W	
$+I_{\text{GH}}$ Max. peak gate current	ALL	3	A	$t_p \leq 5\text{ms}$
$-V_{\text{GH}}$ Max. peak neg. gate voltage	ALL	5	V	
T Mounting torque	ALL	$15.5 [137] \pm 10\%$	N·m	Non-lubricated threads.
		$14 [120] \pm 10\%$	(lbf-in)	Lubricated threads.



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CHARACTERISTICS

PARAMETER	SERIES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TH} Peak on-state voltage	ALL	—	1.10	1.22	V	Initial $T_J = 25^\circ\text{C}$, 60Hz half sine, $I_{peak} = 345\text{A}$.
$V_{T(TO)1}$ Low-level threshold	ALL	—	—	0.743	V	$T_J = \text{max. rated}$ $\text{Av. power} = V_{T(TO)} \cdot I_{T(AV)} + r_T \cdot (I_{T(RMS)})^2$ Use low level values for $I_{TH} \leq \pi I_{T(AV)}$
$V_{T(TO)2}$ High-level threshold		—	—	0.884		
r_{T1} Low-level resistance	ALL	—	—	1.200	$\text{m}\Omega$	
r_{T2} High-level resistance		—	—	0.785		
I_L Latching current	ALL	—	180	—	mA	$T_C = 25^\circ\text{C}$, 12V anode. Gate pulses: 10V, 20 μs , 100 μs .
I_H Holding current	ALL	—	60	500	mA	$T_C = 25^\circ\text{C}$, 12V anode. Initial $I_T = 3\text{A}$.
t_d Delay time	ALL	—	0.5	1.5	μs	$T_C = 25^\circ\text{C}$, $V_D = V_{DRM}$, 50A resistive load. Gate pulses: 10V, 20 μs , 10 μs , 1 μs rise.
t_q Turn-off time	S18C	—	40	—	μs	$T_J = \text{max. rated}$, $I_{TH} = 200\text{A}$, $di_R/dt = 10\text{A}/\mu\text{s}$, $V_R = 50\text{V}$, $dv/dt = 20\text{V}/\mu\text{s}$ lin. to rated V_{DRM} . Gate: 0V, 100 Ω .
	S18CH	—	55	—		
t_a Reverse current rise	ALL	—	7.9	—	μs	$T_J = 125^\circ\text{C}$, $I_{TH} = 200\text{A}$, $di_R/dt = 1\text{A}/\mu\text{s}$
t_b Reverse current fall	ALL	—	2.6	—	μs	
$I_{RM(REC)}$ Reverse current	ALL	—	7.9	—	A	
Q_{RR} Recovered charge	ALL	—	42	—	μC	
dv/dt Critical rate-of-rise of voltage	ALL	500	700	—	$\text{V}/\mu\text{s}$	$T_J = 125^\circ\text{C}$. Exp. to 100% or lin. Higher dv/dt values to 80% V_{DRM} , gate open. available.
		1000	—	—		$T_J = 125^\circ\text{C}$. Exp. to 67% V_{DRM} , gate open.
I_{RM} , I_{DM} Peak reverse and off-state current	S18C	—	7	20	mA	$T_J = 125^\circ\text{C}$. Rated V_{RRM} and V_{DRM} , gate open.
	S18CH	—	15	50		$T_J = 150^\circ\text{C}$
I_{GT} DC gate current to trigger	ALL	—	—	300	mA	$T_C = -40^\circ\text{C}$ +12V anode. For recommended gate drive see "Gate Characteristics" figure.
		25	50	150		$T_C = 25^\circ\text{C}$
V_{GT} DC gate voltage to trigger	ALL	—	—	3.3	V	$T_C = -40^\circ\text{C}$
		—	1.2	2.5		$T_C = 25^\circ\text{C}$
V_{GD} DC gate voltage not to trigger	ALL	—	—	0.3	V	$T_C = 125^\circ\text{C}$. Max. value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	ALL	—	—	0.250	$^\circ\text{C}/\text{W}$	DC operation
		—	—	0.292	$^\circ\text{C}/\text{W}$	180° sine wave
		—	—	0.302	$^\circ\text{C}/\text{W}$	120° rectangular wave
R_{thCS} Thermal resistance, case-to-sink	ALL	—	—	0.100	$^\circ\text{C}/\text{W}$	Mounting surface smooth, flat and greased.
wt Weight	ALL	—	100[3.5]	—	g[oz.]	
Case Style	ALL	TO-209AC (TO-94)		JEDEC		

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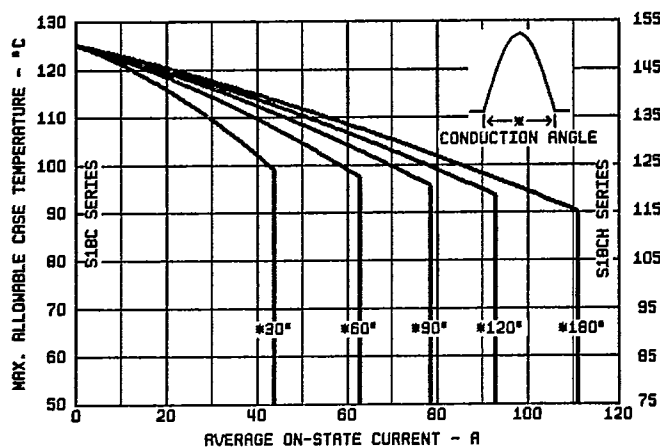


Fig. 1 — Case Temperature Ratings — Sinusoidal Waveforms, 50 to 400 Hz

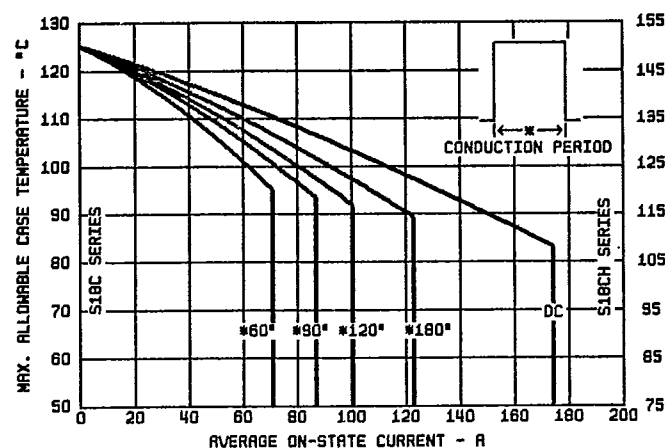


Fig. 2 — Case Temperature Ratings — Rectangular Waveforms, 50 to 400 Hz

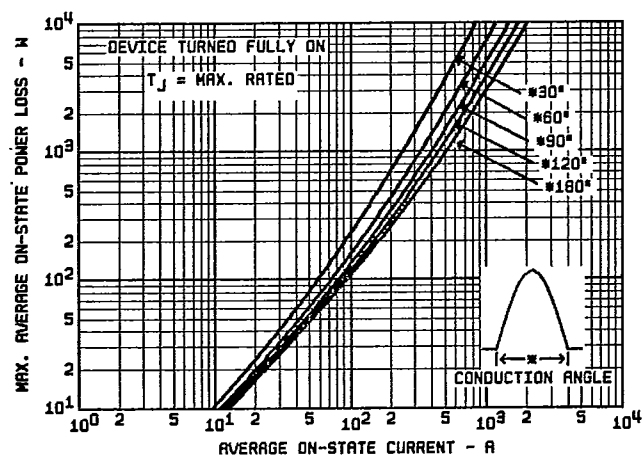


Fig. 3 — Power Loss Characteristics — Sinusoidal Waveforms

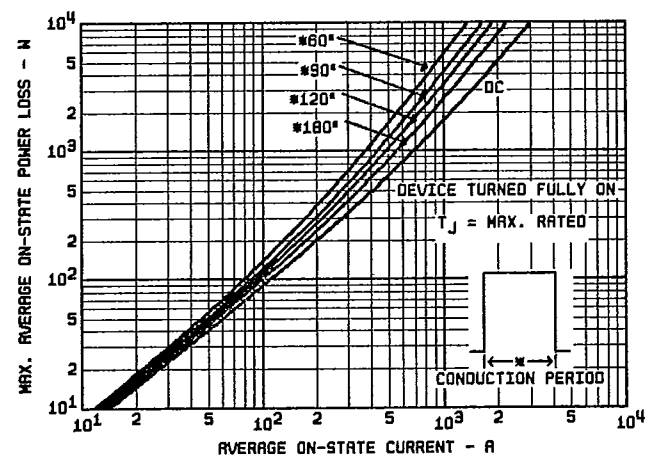


Fig. 4 — Power Loss Characteristics — Rectangular Waveforms

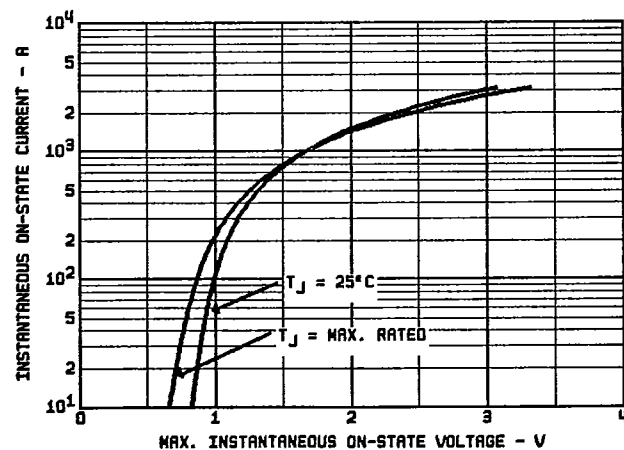


Fig. 5 — On-State Characteristics

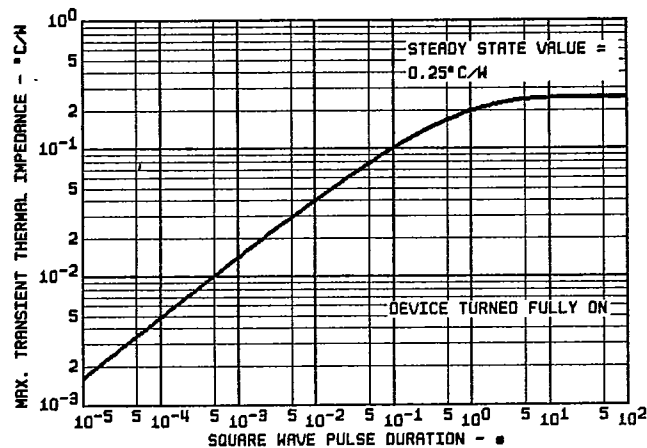


Fig. 6 — Transient Thermal Impedance, Junction-to-Case

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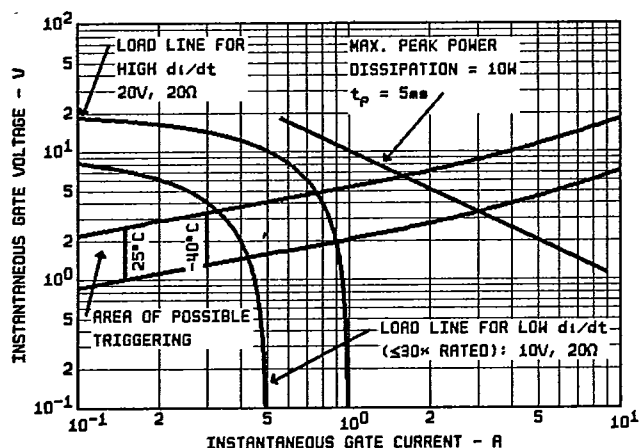


Fig. 7 — Gate Characteristics

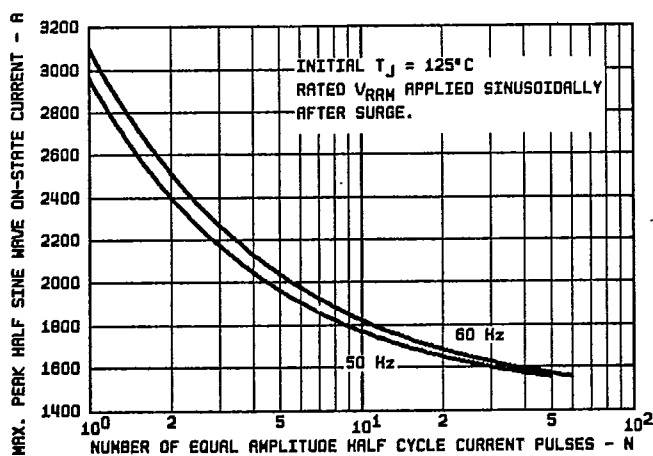


Fig. 8 — Non-Repetitive Surge Current Ratings

ORDERING INFORMATION

TYPE	PACKAGE		TEMPERATURE		VOLTAGE		LEADS & TERMINALS		BASE MODIFICATION (2)	
	CODE	DESCRIPTION	CODE	MAX. T_J	CODE	V_{DRM}	CODE	DESCRIPTION	CODE	DESCRIPTION
S18	CG	1/2" stud, glass seal. Standard in USA	—	125°C	4A	400V	0	Flexible leads, eyelet terminals. Standard in USA. (Fig. 1)	M	Metric threads.
			H	150°C	2A	200V				
	C	1/2" stud, ceramic housing. Standard in Europe.					1	Flexible leads, fast-on terminals. Standard in Europe. (Fig. 2)		
							2	Flag terminals (1). (Fig. 3 and 4)		

[1] Mounting torque on screw in flag terminal: 1.4 N·m (12 lbf-in)

(2) Use only if required

For example, for a device with standard USA case, max. $T_J = 150^\circ\text{C}$, $V_{DRM} = 200\text{V}$, order as:

TYPE	PACKAGE	TEMPERATURE	VOLTAGE	LEADS & TERMINALS
S18	CG	H	2A	0

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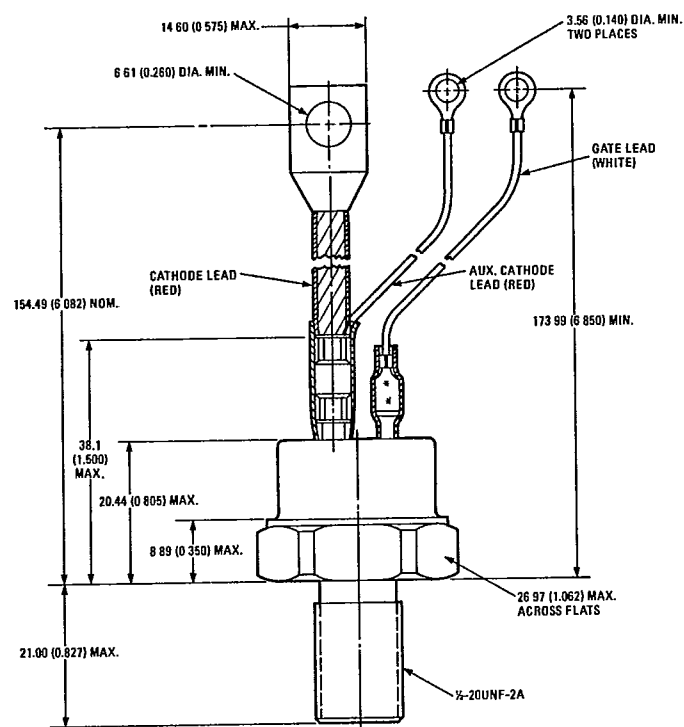


Fig. 1 — Conforms to JEDEC Outline TO-209AC (TO-94)
Dimensions in Millimeters and (Inches)

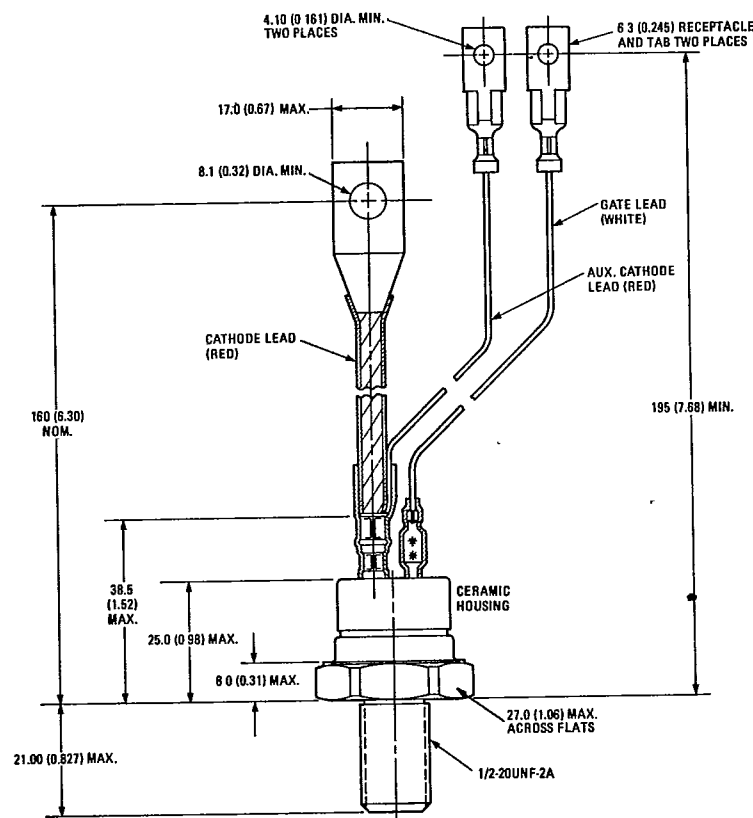
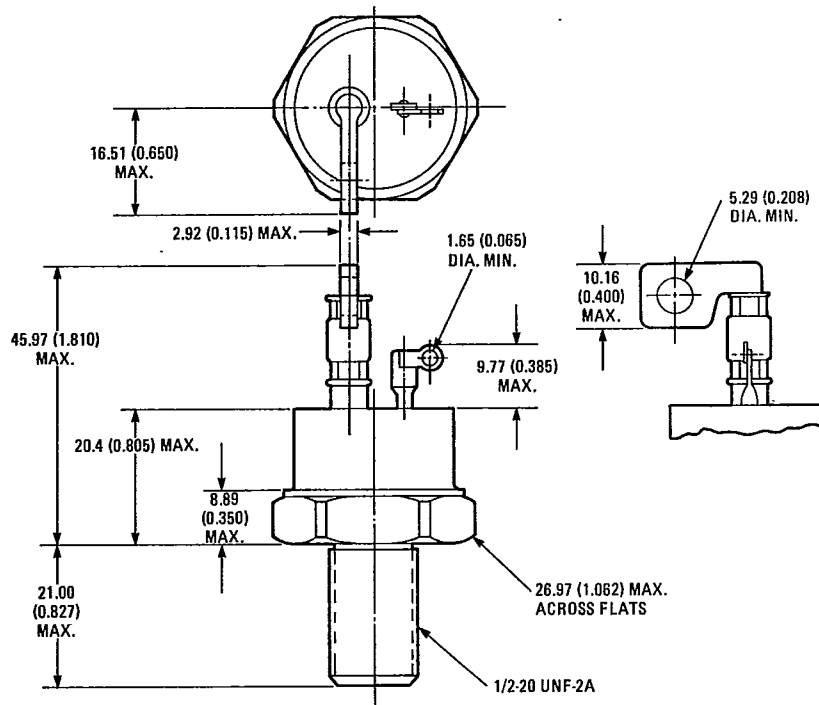


Fig. 2 — Similar to TO-209AC (TO-94)
Dimensions in Millimeters and (Inches)

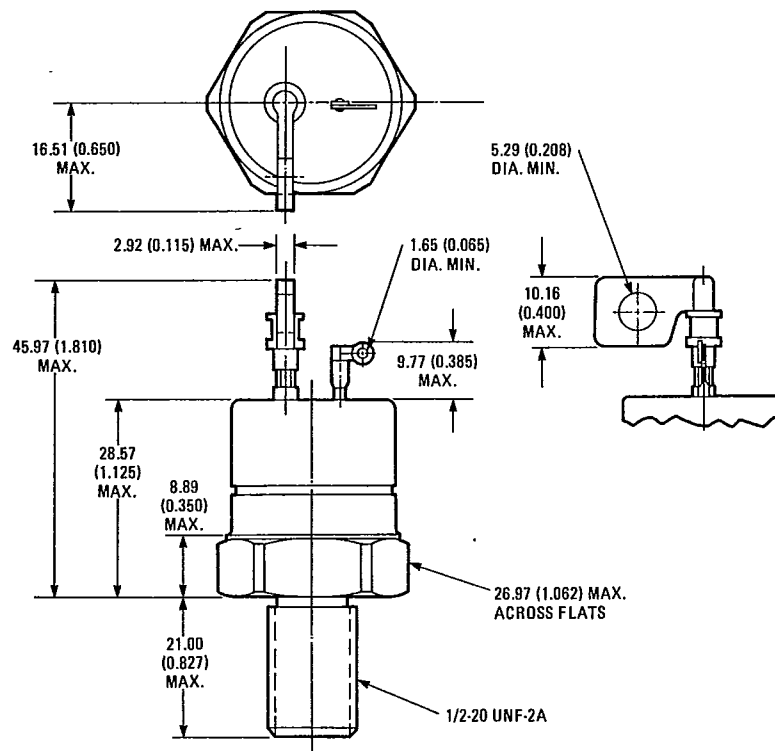


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**Fig. 3 — Conforms to JEDEC Outline TO-208AD (TO-83)
(Standard in U.S.A.)**

Dimensions in Millimeters and (Inches)



**Fig. 4 — Conforms to JEDEC Outline TO-208AD (TO-83)
(Standard in Europe)**

Dimensions in Millimeters and (Inches)