Status: **Active**

Product Quick Links

Specifications
Product Options
Technical Support
Contact Sales

853S1208I
Differential-to-LVPECL Fanout Buffer with Divider and Glitchless Switch

The 853S1208I is a low skew, 8 output LVPECL Fanout Buffer with selectable divider. The 853S1208I has 2 selectable inputs that accept a variety of differential input types. The device provides the capability to suppress any glitch at the outputs of the device during an input clock switch to enhance clock redundancy in fault tolerant applications. The divide select inputs, DIV_SELA and DIV_SELB, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The output enable pins assigned to each output, support enabling and disabling each output individually. The 853S1208I is characterized at full 3.3V or 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the 853S1208I ideal for high performance applications.

Features

- Eight differential LVPECL output pairsEach output has individual synchronous output enable
- Two selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx pairs can accept the following differentialinput levels: LVPECL, LVDS, SSTL
- Maximum output frequency: 700MHz
- Independent bank control for ÷1 or ÷2 operation
- Glitchless output behavior during input switch
- Output skew: TBD
- Bank skew: TBD
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Product Specification

ADDITIVE PHASE JITTER RMS (PS)	OUTPUT SKEW (PS)	CORE VOLTAGE (V)	INPUTS (#)	INPUT SIGNAL	INPUT FREQ (MHZ)	OUTPUT VOLTAGE (V)	OUTPUTS (#)	OUTPUT TYPE	OUTPUT FREQ RANGE (MHZ)
		2.5, 3.3	2	SSTL, LVDS, LVPECL	0.000000 - 700.000000	2.5, 3.3	8	LVPECL	0.000000 - 700.000000

Product Options

ORDERABLE PART ID	PART STATUS	PKG. CODE	PKG. TYPE	LEAD COUNT (#)	TEMP. GRADE	PB (LEAD) FREE	ORDER
853S1208AYILF	Active	DXG48	PTQFP	48	I	Y	Check Inventory

Documents

There are no public documents available for this product. Click here to request documentation.

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