

TOSHIBA Photocoupler GaAlAs Ired & Photo IC

## 6N138, 6N139

Current Loop Driver.

Low Input Current Line Receiver.

CMOS Logic Interface.

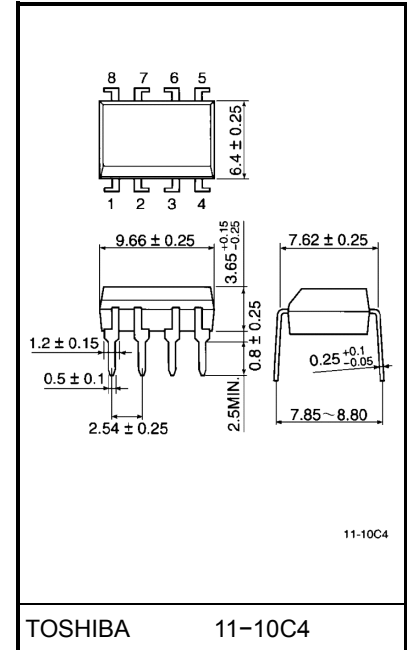
The TOSHIBA 6N138 and 6N139 consists of a GaAlAs infrared

emitting diode coupled with a split-Darlington output configuration.

A high speed GaAlAs Ired manufactured with an unique LPE junction, has the virtue of fast rise and fall time at low drive current.

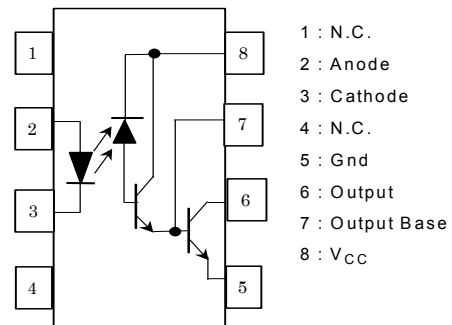
- Isolation voltage: 2500Vrms (min.)
- Current transfer ratio
  - : 6N138 – 300% (min.) ( $I_F=1.6\text{mA}$ )
  - : 6N139 – 400% (min.) ( $I_F=0.5\text{mA}$ )
- Switching time: 6N138 –  $t_{PHL}=10\mu\text{s}$  (max.)  
 –  $t_{PLH}=35\mu\text{s}$  (max.)  
 6N139 –  $t_{PHL}=1\mu\text{s}$  (max.)  
 –  $t_{PLH}=7\mu\text{s}$  (max.)
- UL recognized: UL1577, file no. E67349

Unit in mm

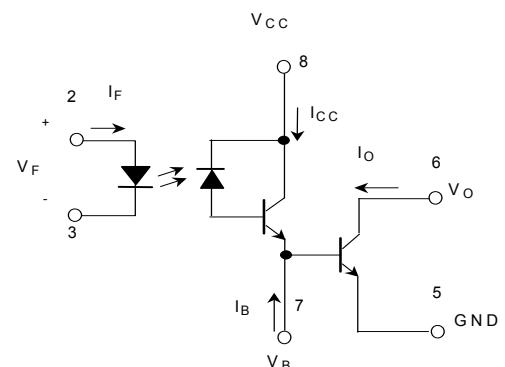


Weight: 0.54 g

### Pin Configuration (top view)



### Schematic



## Maximum Ratings (\*) (Ta = 0°C to + 70°C)

| Characteristic                               |                                   | Symbol         | Rating     | Unit      |
|----------------------------------------------|-----------------------------------|----------------|------------|-----------|
| LED                                          | Forward current (Note 1)          | $I_F$          | 20         | mA        |
|                                              | Pulse forward current             | $I_{FP}^{(*)}$ | 40         | mA        |
|                                              | Total pulse forward current       | $I_{FP}^{(*)}$ | 1          | A         |
|                                              | Reverse voltage                   | $V_R$          | 5          | V         |
|                                              | Diode power dissipation (Note 2)  | $P_D$          | 35         | mW        |
| Detector                                     | Output current (Note 3)           | $I_O$          | 60         | mA        |
|                                              | Emitter-base reverse voltage      | $V_{EB}$       | 0.5        | V         |
|                                              | Supply voltage                    | $V_{CC}^{(*)}$ | -0.5 to 18 | V         |
|                                              | Output voltage                    | $V_O^{(*)}$    | -0.5 to 18 | V         |
|                                              | Output power dissipation (Note 4) | $P_O$          | 100        | mW        |
| Operating temperature range                  |                                   | $T_{opr}$      | 0 to 70    | °C        |
| Storage temperature range                    |                                   | $T_{stg}$      | -55 to 125 | °C        |
| Lead solder temperature (10s) <sup>(*)</sup> |                                   | $T_{sol}$      | 260        | °C        |
| Isolation voltage (1min., R.H.≤ 60%)         |                                   | $BV_S^{(**)}$  | 2500       | $V_{rms}$ |
|                                              |                                   |                | 3540       | $V_{dc}$  |

(\*) JEDEC registered data

(\*\*) Not registered JEDEC

(\*1) 50% duty cycle, 1ms pulse width

(\*2) Pulse width 1μs, 300pps

(\*3) 6N138··· -0.5 to 7V

(\*4) 1.6mm below seating plane

## Electrical Characteristics

Over Recommended Temperature (Ta = 0°C to 70°C, unless otherwise noted)

| Characteristic                             |       | Symbol                            | Test Condition                                                        | Min. | (*5)Typ.         | Max. | Unit    |
|--------------------------------------------|-------|-----------------------------------|-----------------------------------------------------------------------|------|------------------|------|---------|
| Current transfer ratio<br>(Note 5, 6)      | 6N139 | CTR(*)                            | I <sub>F</sub> =0.5mA, V <sub>O</sub> =0.4V<br>V <sub>CC</sub> =4.5V  | 400  | 800              | —    | %       |
|                                            | 6N138 |                                   | I <sub>F</sub> =1.6mA, V <sub>O</sub> =0.4V<br>V <sub>CC</sub> =4.5V  | 500  | 900              | —    |         |
|                                            |       |                                   |                                                                       |      | 300              | 600  |         |
| Logic low output voltage<br>(Note 6)       | 6N139 | V <sub>OL</sub>                   | I <sub>F</sub> =1.6mA, I <sub>O</sub> =6.4mA<br>V <sub>CC</sub> =4.5V | —    | 0.1              | 0.4  | V       |
|                                            |       |                                   | I <sub>F</sub> =5mA, I <sub>O</sub> =15mA<br>V <sub>CC</sub> =4.5V    | —    | 0.1              | 0.4  |         |
|                                            |       |                                   | I <sub>F</sub> =12mA, I <sub>O</sub> =24mA<br>V <sub>CC</sub> =4.5V   | —    | 0.2              | 0.4  |         |
|                                            | 6N138 |                                   | I <sub>F</sub> =1.6mA, I <sub>O</sub> =4.8mA<br>V <sub>CC</sub> =4.5V | —    | 0.1              | 0.4  |         |
| Logic high output current<br>(Note 6)      | 6N139 | I <sub>OH</sub> (*)               | I <sub>F</sub> =0mA, V <sub>O</sub> =V <sub>CC</sub> =18V             | —    | 0.05             | 100  | μA      |
|                                            | 6N138 |                                   | I <sub>F</sub> =0mA, V <sub>O</sub> =V <sub>CC</sub> =7V              | —    | 0.05             | 250  |         |
| Logic low supply current<br>(Note 6)       |       | I <sub>CCL</sub>                  | I <sub>F</sub> =1.6mA, V <sub>O</sub> =Open<br>V <sub>CC</sub> =5V    | —    | 0.2              | —    | mA      |
| Logic high supply current<br>(Note 6)      |       | I <sub>CCH</sub>                  | I <sub>F</sub> =0mA, V <sub>O</sub> =Open, V <sub>CC</sub> =5V        | —    | 10               | —    | nA      |
| Input forward voltage                      |       | V <sub>F</sub> (*)                | I <sub>F</sub> =1.6mA, T <sub>a</sub> =25°C                           | —    | 1.65             | 1.7  | V       |
| Input reverse breakdown voltage            |       | BV <sub>R</sub> (*)               | I <sub>R</sub> =10μA, T <sub>a</sub> =25°C                            | 5    | —                | —    | V       |
| Temperature coefficient of forward voltage |       | ΔV <sub>F</sub> / ΔT <sub>a</sub> | I <sub>F</sub> =1.6mA                                                 | —    | −1.9             | —    | mV / °C |
| Input capacitance                          |       | C <sub>IN</sub>                   | f=1MHz, V <sub>F</sub> =0                                             | —    | 60               | —    | pF      |
| Resistance (input–output)                  |       | R <sub>I-O</sub>                  | V <sub>I-O</sub> =500V<br>R.H.≤ 60% (Note 7),                         | —    | 10 <sup>12</sup> | —    | Ω       |
| Capacitance (input–output)                 |       | C <sub>I-O</sub>                  | f=1MHz (Note 7)                                                       | —    | 0.6              | —    | pF      |

(\*\*) JEDEC registered data.

(\*5) All typicals at  $T_a=25^\circ\text{C}$  and  $V_{CC}=5\text{V}$ , unless otherwise noted.

## Switching Specifications (Ta=25°C, VCC=5V, unless otherwise specified)

| Characteristic                                                     |       | Symbol          | Test Circuit | Test Condition                                         | Min. | Typ. | Max. | Unit        |
|--------------------------------------------------------------------|-------|-----------------|--------------|--------------------------------------------------------|------|------|------|-------------|
| Propagation delay time to logic low at output (Note 6, 8)          | 6N139 | $t_{pHL}^{(*)}$ | 1            | $I_F=0.5mA, R_L=4.7k\Omega$                            | —    | 5    | 25   | $\mu s$     |
|                                                                    |       |                 |              | $I_F=12mA, R_L=270\Omega$                              | —    | 0.2  | 1    |             |
|                                                                    | 6N138 |                 |              | $I_F=1.6mA, R_L=2.2k\Omega$                            | —    | 1    | 10   |             |
| Propagation delay time to logic high at output (Note 6, 8)         | 6N139 | $t_{pLH}^{(*)}$ | 1            | $I_F=0.5mA, R_L=4.7k\Omega$                            | —    | 5    | 60   | $\mu s$     |
|                                                                    |       |                 |              | $I_F=12mA, R_L=270\Omega$                              | —    | 1    | 7    |             |
|                                                                    | 6N138 |                 |              | $I_F=1.6mA, R_L=2.2k\Omega$                            | —    | 4    | 35   |             |
| Common mode transient immunity at logic high level output (Note 9) |       | $CM_H$          | 2            | $I_F=0mA, R_L=2.2k\Omega$<br>$V_{CM}=400V_{p-p}$       | —    | 500  | —    | $V / \mu s$ |
| Common mode transient immunity at logic low level output (Note 9)  |       | $CM_L$          | 2            | $I_F=1.6mA$<br>$R_L=2.2k\Omega$<br>$V_{CM}=400V_{p-p}$ | —    | –500 | —    | $V / \mu s$ |

(\*)JEDEC registered data.

(Note 1): Derate linearly above 50°C free-air temperature at a rate of 0.4mA / °C

(Note 2): Derate linearly above 50°C free-air temperature at a rate of 0.7mW / °C

(Note 3): Derate linearly above 25°C free-air temperature at a rate of 0.7mA / °C

(Note 4): Derate linearly above 25°C free-air temperature at a rate of 2.0mW / °C

(Note 5): DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.

(Note 6): Pin 7 open.

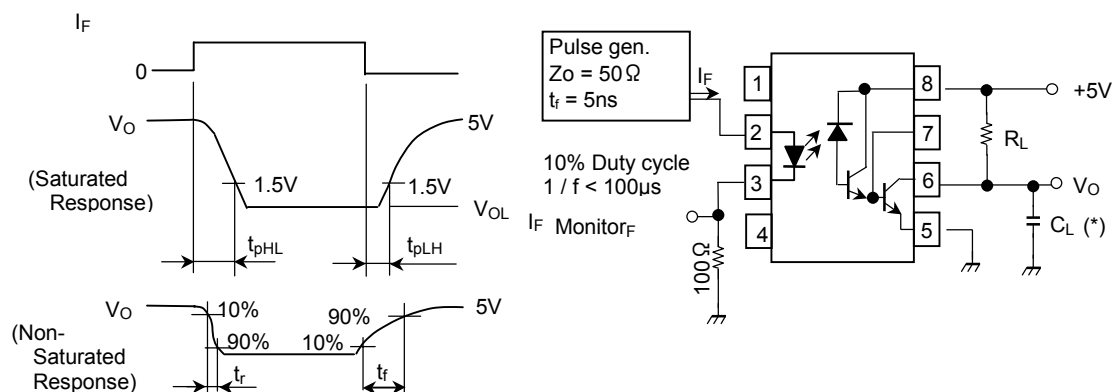
(Note 7): Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.

(Note 8): Use of a resistor between pin 5 and 7 will decrease gain and delay time.

(Note 9): Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dv_{CM} / dt$  on the leading edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0V$ ).

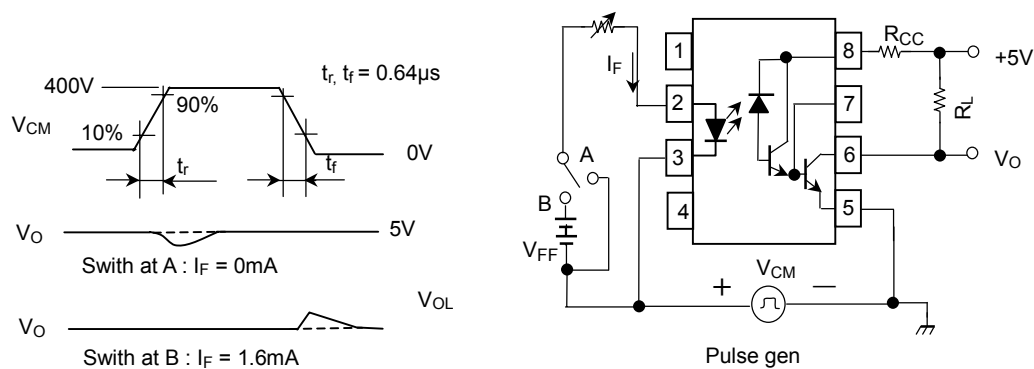
Common mode transient immunity in Logic Low level is the maximum tolerable (negative)  $dv_{CM} / dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8V$ ).

## Test Circuit 1.



(\*) $C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

## Test Circuit 2.



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000707EBC

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