FEATURES

- PECL version of popular ECLinPS E111
- Low skew
- Guaranteed skew spec
- VBB output
- TTL enable input
- Selectable TTL or PECL clock input
- Single +5V supply
- Differential internal design
- Similar pin configuration to E111
- PECL I/O fully compatible with industry standard
- Internal 75KΩ PECL input pull-down resistors
- Available in 28-pin PLCC and SOIC packages

Precision Edge®

DESCRIPTION

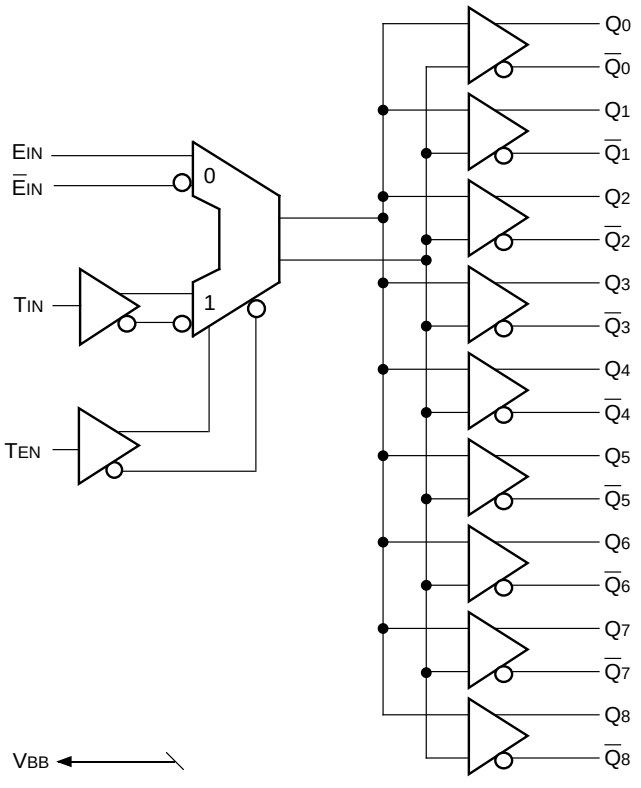
The SY100S811 is a low skew 1-to-9 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is HIGH, the TTL input is enabled and the PECL input is disabled. When the enable pin is set LOW, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the S811 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

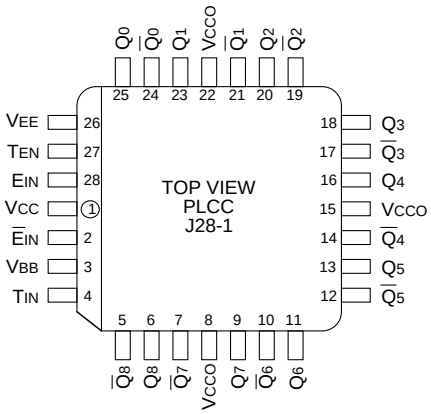
To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of PECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01µF capacitor.

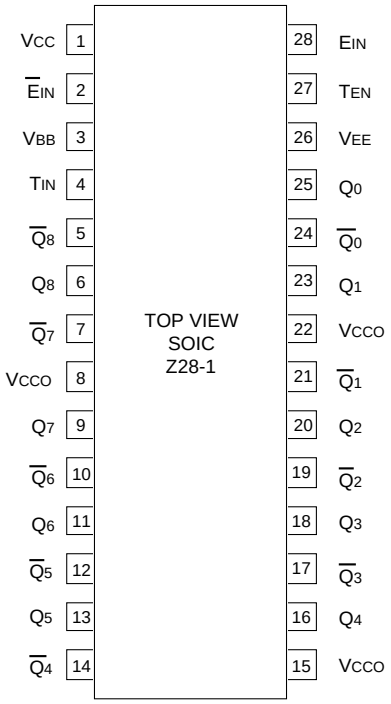
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



28-Pin SOIC (Z28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S811ZC	Z28-1	Commercial	SY100S811ZC	Sn-Pb
SY100S811ZCTR[1]	Z28-1	Commercial	SY100S811ZC	Sn-Pb
SY100S811JC	J28-1	Commercial	SY100S811JC	Sn-Pb
SY100S811JCTR[1]	J28-1	Commercial	SY100S811JC	Sn-Pb
SY100S811ZH[2]	Z28-1	Commercial	SY100S811ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S811ZHTR[1, 2]	Z28-1	Commercial	SY100S811ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S811JZ[2]	J28-1	Commercial	SY100S811JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S811JZTR[1, 2]	J28-1	Commercial	SY100S811JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
E_{IN}, $\overline{E}_{IN}$	Differential PECL Input Pair
T_{IN}	TTL Input
T_{EN}	TTL Input Enable
Q_0, $\overline{Q}_0$ – $\overline{Q}_8$, Q_8	Differential PECL Outputs
V_{BB}	V_{BB} Output
V_{CC}	PECL V_{CC} (+5.0V)
V_{EE}	PECL Ground (0V)

TRUTH TABLE

T_{EN}	E_{IN}	T_{IN}	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{BB}	Output Reference[1] Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA
V_{IH}	Input HIGH Voltage[1]	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
V_{IL}	Input LOW Voltage[1]	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
V_{OH}	Output HIGH Voltage[2]	V_{CC} –1025	V_{CC} –955	V_{CC} –870	V_{CC} –1025	V_{CC} –955	V_{CC} –870	V_{CC} –1025	V_{CC} –955	V_{CC} –870	mV
V_{OL}	Output LOW Voltage[2]	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620	mV
I_{CC}	Power Supply[3] Current	—	53	65	—	53	65	—	60	74	mA

Notes:

1. $V_{CC} = V_{CCO} = 5.0V$
2. $V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.) Loading with 50Ω to V_{CC} –2V.
3. All inputs and outputs open.

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current[1],[2]	—	—	20	—	—	20	—	—	20	µA
		—	—	100	—	—	100	—	—	100	
I_{IL}	Input LOW Current[3]	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA
V_{IK}	Input Clamp Voltage[4]	—	—	–1.2	—	—	–1.2	—	—	–1.2	V

Notes:

1. $V_{IN} = 2.7V$
2. $V_{IN} = 5.0V$
3. $V_{IN} = 0.5V$
4. $I_{IN} = -18mA$

AC ELECTRICAL CHARACTERISTICS[1–6]

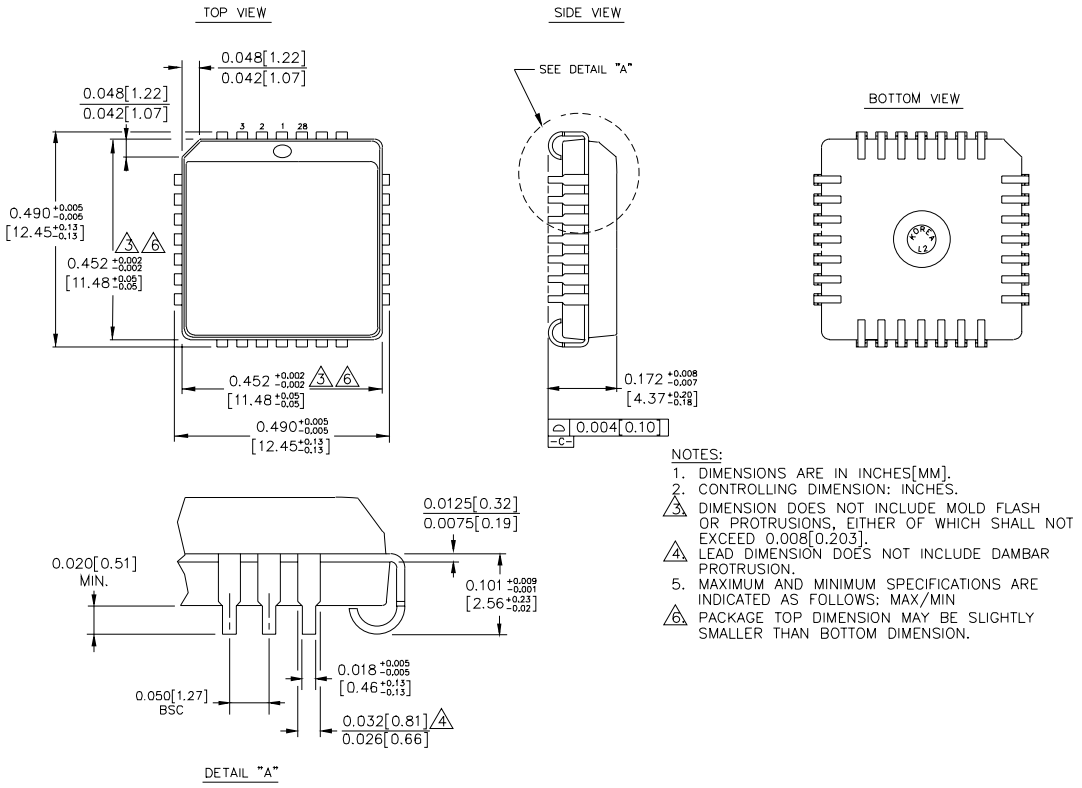
$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation Delay to Output[1]										ps
t_{PHL}	E_{IN} (differential)[2]	430	—	630	430	—	630	430	—	630	
	E_{IN} (single-ended)[3]	330	—	730	330	—	730	330	—	730	
	T_{IN}	350	—	950	350	—	950	350	—	950	
t_{skew}	Within-Device skew[4]	—	25	50	—	25	50	—	25	50	ps
V_{PP}	Minimum PECL Input Swing[5]	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	PECL Common Mode Range[6]	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V
t_r	Output Rise/Fall Times	275	375	600	275	375	600	275	375	600	ps
t_f	20% to 80%										

Notes:

1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S811, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

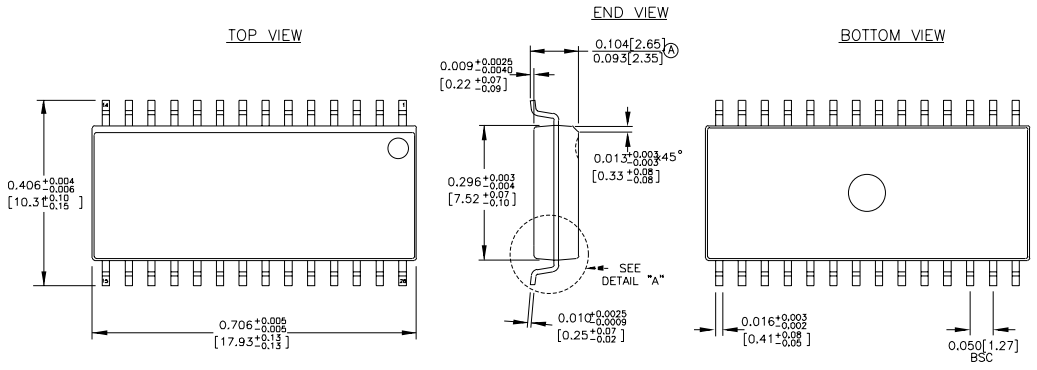
28-PIN PLCC (J28-1)



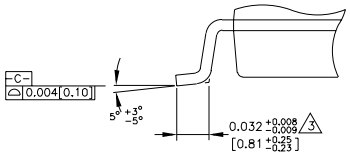
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

28-PIN SOIC .300" WIDE (Z28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN



DETAIL "A"

Rev. 02

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