Complete 12-Bit A/D Converter

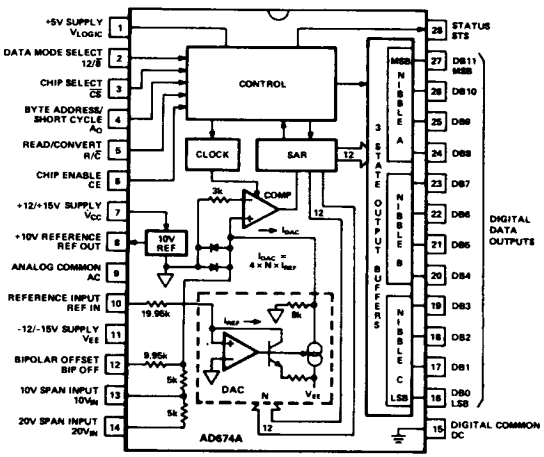
AD674A*

FEATURES

Complete 12-Bit A/D Converter with Reference and Clock
Faster Version of AD574A
8- and 16-Bit Bus Interface
No Missing Codes Over Temperature
15 μs max Conversion Time
±12 V and ±15 V Operation
Unipolar and Bipolar Inputs

NOT RECOMMENDED FOR NEW DESIGNS, REPLACE WITH AD674B (SEE PAGE 2–109)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD674A is a complete 12-bit successive-approximation analog-to-digital converter with three-state output buffer circuitry for direct interface to an 8- and 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit requires only power supplies and control signals for operation.

The AD674A is pin compatible with the industry-standard AD574A but offers faster conversion time and bus-access speed.

The AD674A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost. The chips are laser trimmed at the wafer stage to obtain full rated performance without external trims.

The AD674A is available in six different grades. The AD674AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD674AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically sealed ceramic DIP.

The S, T, and U grades are also available with optional processing to MIL-STD-883C, Class B in a 28-pin DIP or 28-pin LCC package. The Analog Devices Military Products Databook should be consulted for details on /883B testing of the AD674A.

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

This an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PRODUCT HIGHLIGHTS

1. The AD674A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeroes).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 1% maximum error and 15 ppm/°C typical T.C. The reference is available externally and can drive up to 2.0 mA beyond the requirements of the reference and bipolar offset resistors.

AD674A—SPECIFICATIONS (@ +25°C with V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, V_{EE} = −15 V or −12 V unless otherwise indicated)

Model	AD674AJ Min	AD674AJ Typ	AD674AJ Max	AD674AK Min	AD674AK Typ	AD674AK Max	AD674AL Min	AD674AL Typ	AD674AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to Zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to Zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (With fixed 50 Ω resistor from REF OUT to REF IN) (Adjustable to Zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of FS
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using Internal Reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max Change in Full-Scale Calibration										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	µA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE} ≤500 µA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK} ≤1.6 mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	µA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[1]			2.0			2.0			2.0	mA
(External load should not change during conversion)										

NOTES

[1]The reference should be buffered for operation on ±12 V supplies.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD674AS Min	AD674AS Typ	AD674AS Max	AD674AT Min	AD674AT Typ	AD674AT Max	AD674AU Min	AD674AU Typ	AD674AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to Zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to Zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (With fixed 50 Ω resistor from REF OUT to REF IN) (Adjustable to Zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of FS
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using Internal Reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max Change in Full-Scale Calibration										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE} ≤500 μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK} ≤1.6 mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[1] (External load should not change during conversion)			2.0			2.0			2.0	mA

NOTES

[1]The reference should be buffered for operation on ±12 V supplies.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
Momentary Short to V_{CC}
Chip Temperature . . . . . 175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

NOTE
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONVERT START TIMING - FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			200	ns
t_{HEC}	CE Pulse Width	50			ns
t_{SSC}	$\overline{CS}$ to CE Setup	50			ns
t_{HSC}	$\overline{CS}$ Low During CE High	50			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50			ns
t_C	Conversion Time				
	8-Bit Cycle	6	8	10	µs
	12-Bit Cycle	9	12	15	µs

READ TIMING - FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}	Output Float Delay			150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	30	55	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

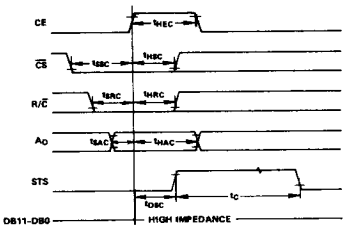


Figure 1. Convert Start Timing

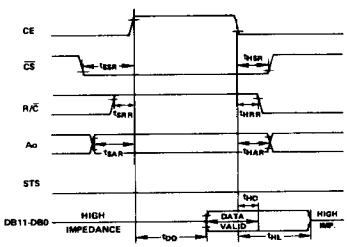


Figure 2. Read Cycle Timing

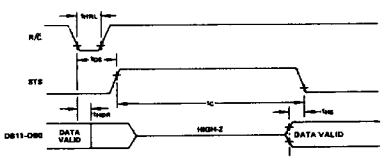


Figure 3. Low Pulse for R/$\overline{C}$-Outputs Enabled After Conversion

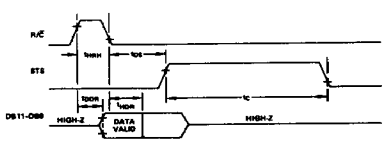


Figure 4. High Pulse for R/$\overline{C}$-Outputs Enable While R/$\overline{C}$ High, Otherwise High-Z

ORDERING GUIDE

Model	Temperature Range	Linearity Error (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})	Full Scale T.C. (ppm/°C)	Package Option*
AD674AJD	0 to +70°C	±1 LSB	11 Bits	50.0	D-28
AD674AKD	0 to +70°C	±1/2 LSB	12 Bits	27.0	D-28
AD674ALD	0 to +70°C	±1/2 LSB	12 Bits	10.0	D-28
AD674ASD	−55°C to +125°C	±1 LSB	11 Bits	50.0	D-28
AD674ATD	−55°C to +125°C	±1 LSB	12 Bits	25.0	D-28
AD674AUD	−55°C to +125°C	±1 LSB	12 Bits	12.5	D-28

*D = Ceramic DIP. For outline information see Package Information section.