


SANYO Semiconductors

DATA SHEET

CMOS IC LV51144T — 1-Cell Lithium-Ion Battery Protection IC

Overview

The LV51144T is protection IC for rechargeable Li-ion battery by high withstand voltage CMOS process.

The LV51144T protect single-cell Li-ion battery from over-charge, over-discharge, charge over-current and discharge over-current.

Features

- High accuracy detection voltage

Over-charge detection(no hysteresis)	±25mV
Over-discharge detection(no hysteresis)	±25%
Charge over-current detection	±30mV
Discharge over-current detection	±20mV
- Delay time (internal adjustment)
- Low current consumption

Operation	Typ. 3.0μA
Over-discharge condition	Max. 0.1μA
- 0V cell battery charging function
- The over-discharge detection is released only when the charger is connected.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		V _{SS} -0.3 to V _{SS} +7	V
Input voltage of V _M	V _M		V _{DD} -28 to V _{DD} +0.3	V
Output voltage of C _O	V _{CO}		V _M -0.3 to V _{DD} +0.3	V
Output voltage of D _O	V _{DO}		V _{SS} -0.3 to V _{DD} +0.3	V
Power dissipation	P _D		350	mW
Operating temperature	T _{opr}		-40 to +85	°C
Storage temperature	T _{stg}		-55 to +125	°C

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LV51144T

Electrical Characteristics at Topr = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Detection voltage							
Over-charge detection voltage	VC		1	3.625	3.650	3.675	V
Over-discharge detection voltage (*2)	Vdc		1	2.438	2.500	2.563	V
Charge over-current detection voltage	Vlc		2	-0.230	-0.200	-0.170	V
Discharge over-current detection voltage	Vldc		2	0.180	0.200	0.220	V
Load short-circuiting detection voltage	Vshort	Based on VDD, VDD = 3.5V	2	-1.7	-1.3	-1.0	V
Input voltage							
Input voltage between VDD and VSS	VDD	Internal circuit operating voltage	-	1.8		7.0	V
0V battery charge starting charger voltage	Vcha	Acceptable	3		0.9	1.4	V
Current consumption							
Current consumption on operation	Iopr	VDD = 3.5V, VM = 0V	4		3.0	6.0	μA
Current consumption on shutdown	Isdn	VDD = VM = 1.8V	4			0.1	μA
Output resistance							
CO : Pch ON resistance	Rcop	CO = 3.0V, VDD = 3.5V, VM = 0V	5	1.5	3.0	4.5	kΩ
CO : Nch ON resistance	Rcon	CO = 0.5V, VDD = 4.6V, VM = 0V	5	0.5	1.0	1.5	kΩ
DO : Pch ON resistance	Rdop	DO = 3.0V, VDD = 3.5V, VM = 0V	5	1.7	3.5	5.0	kΩ
DO : Nch ON resistance	Rdon	DO = 0.5V, VDD = VM = 1.8V	5	1.7	3.5	5.0	kΩ
Discharge over-current release resistance	Rdwn	VDD = 3.5V, VM = 1.0V	5	15.0	30.0	60.0	kΩ
Detection delay time							
Over-charge detection delay time	tc	VDD = VC-0.2V→VC+0.2V, VM = 0V	6	0.70	1.0	1.30	s
Over-discharge detection delay time	tdc	VDD = Vdc+0.2V→Vdc-0.2V, VM = 0V	6	21.7	31.0	40.3	ms
Charge over-current detection delay time	tic	VDD = 3.0V, VM = 0V→-1.0V	6	5.6	8.0	10.4	ms
Discharge over-current detection delay time	tidc	VDD = 3.0V, VM = 0V→1.0V	6	5.6	8.0	10.4	ms
Load short-circuiting detection delay time	tshort	VDD = 3.0V, VM = 0V→3.0V	6	190	370	550	μs
Release delay time							
Release delay time 1 Over-discharge release Charge over-current release (*1) Discharge over-current release Load short-circuiting release	trel1		6	1.0	2.0	3.0	ms
Release delay time 2 Over-charge release	trel2	VDD = VC+0.2V→VC-0.2V, VM = 1.0V	6	8.0	16.0	24.0	ms

Note : *1 When the charger is connected under over-discharge , this means the time after the over-discharge detection is released.

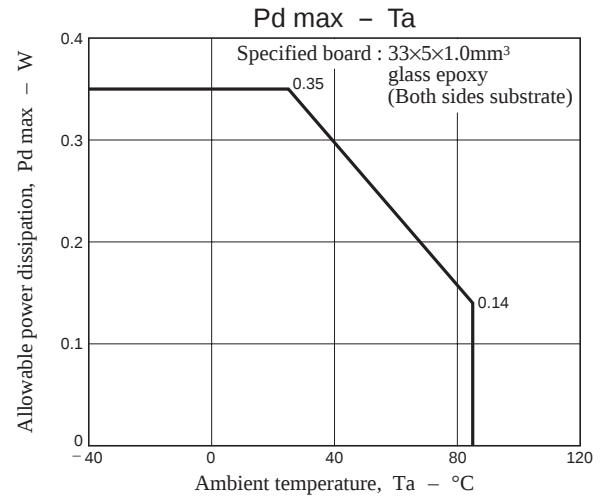
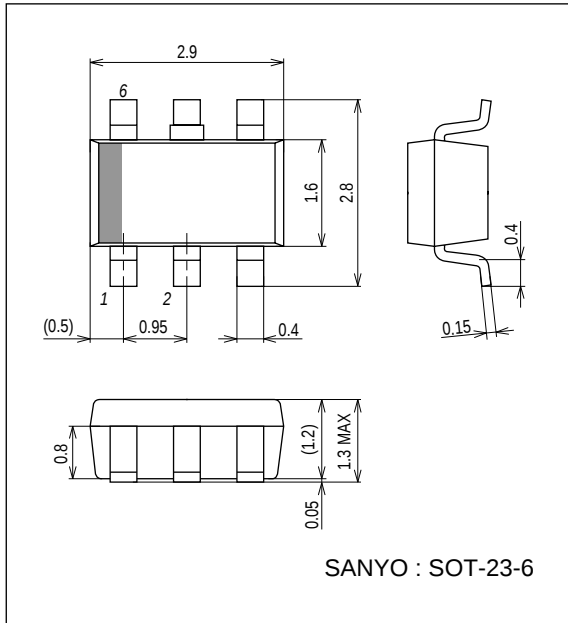
*2 The over-discharge detection is released at this voltage only when the charger is connected.

The over-discharge detection isn't released if the charger isn't connected.

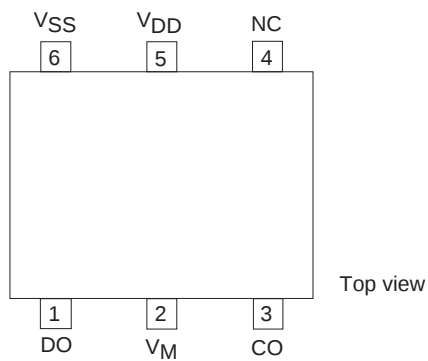
Package Dimensions

unit : mm (typ)

3356



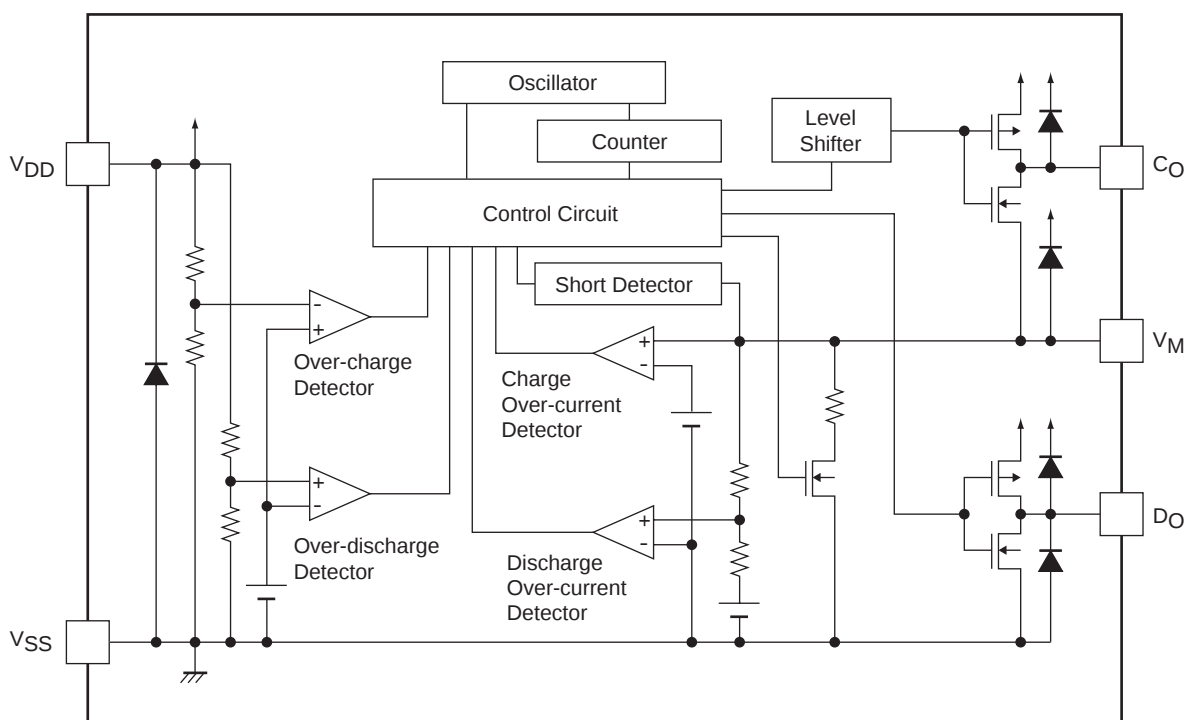
Pin Assignment



Pin Function

Pin No.	Pin Name	Description
1	D _O	FET gate connection for discharge control (CMOS output)
2	V _M	Voltage monitoring for charger negative
3	C _O	FET gate connection for charge control (CMOS output)
4	NC	N/C
5	V _{DD}	Positive power input
6	V _{SS}	Negative power input

Block Diagram



Measurement Conditions

- Over-charge detection voltage --- [Circuit 1]
Set $V_1 = 3.0V$ and $V_2 = 0V$. Over-charge detection voltage V_C is V_1 at which V_{CO} goes "Low" from "High" when V_1 is gradually increased from $3.0V$. Then IC is released from the over-charge state and V_{CO} goes "High" from "Low" at the voltage "Measured V_C " when V_1 is gradually decreased.
- Over-discharge detection voltage --- [Circuit 1]
Set $V_1 = 3.0V$ and $V_2 = 0V$. Over-discharge detection voltage V_{dc} is V_1 at which V_{DO} goes "Low" from "High" when V_1 is gradually decreased from $3.0V$. Next, set V_2 under to charge over-current detection voltage V_{ic} . Then IC is released from the over-discharge state at V_{dc} and V_{DO} goes "High" from "Low".
- Charge over-current detection voltage --- [Circuit 2]
Set $V_1 = 3.0V$ and $V_2 = 0V$. Charge over-current detection voltage V_{ic} is V_2 at which V_{CO} goes "Low" from "High" when V_2 is gradually decreased from $0V$.
- Discharge over-current detection voltage --- [Circuit 2]
Set $V_1 = 3.0V$ and $V_2 = 0V$. Discharge over-current detection voltage V_{ldc} is V_2 at which V_{DO} goes "Low" from "High" when V_2 is gradually increased from $0V$.
- Load short-circuiting detection voltage --- [Circuit 2]
Set $V_1 = 3.0V$ and $V_2 = 0V$. Load short-circuiting detection voltage V_{short} is V_2 at which V_{DO} goes "Low" from "High" within a time between the minimum and the maximum value of load short-circuiting detection delay time t_{short} , when V_2 is increased rapidly within $10\mu s$.
- 0V battery charge starting charger voltage --- [Circuit 3]
Set $V_1 = V_2 = 0V$ and decrease V_2 gradually. 0V battery charge starting charger voltage V_{cha} is V_2 when V_{CO} goes "High" ($V_1 - 0.1V$ or higher).

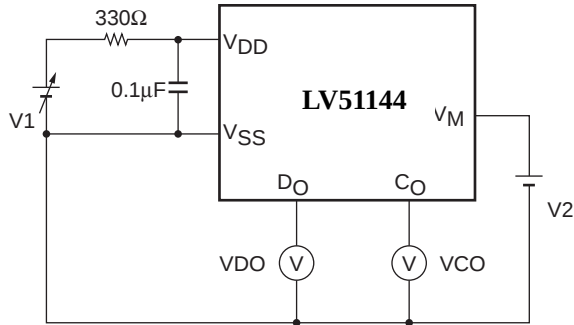
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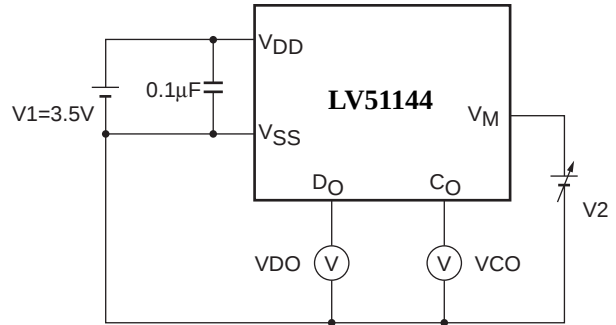
- **Current consumption on operation and shutdown --- [Circuit 4]**
Set $V_1 = 3.5V$ and $V_2 = 0V$ on normal condition. I_{DD} shows current consumption on operation I_{opr} .
Set $V_1 = V_2 = 1.8V$ on over-discharge condition. I_{DD} shows current consumption on shutdown I_{sdn} .
- **Co : Pch ON resistance, Co : Nch ON resistance --- [Circuit 5]**
Set $V_1 = 3.5V$, $V_2 = 0V$ and $V_3 = 3.0V$. $(V_1-V_3)/|I_{Co}|$ is Pch ON resistance R_{cop} .
Set $V_1 = 4.6V$, $V_2 = 0V$ and $V_3 = 0.5V$. $V_3/|I_{Co}|$ is Nch ON resistance R_{con} .
- **Do : Pch ON resistance, Do : Nch ON resistance --- [Circuit 5]**
Set $V_1 = 3.5V$, $V_2 = 0V$ and $V_4 = 3.0V$. $(V_1-V_4)/|I_{Do}|$ is Pch ON resistance R_{dop} .
Set $V_1 = V_2 = 1.8V$ and $V_4 = 0.5V$. $V_4/|I_{Do}|$ is Nch ON resistance R_{don} .
- **Discharge over-current release resistance --- [Circuit 5]**
Set $V_1 = 3.5V$, $V_2 = 0V$ at first. And then, set $V_2 = 1.0V$. $V_2/|I_{VM}|$ is discharge over-current release resistance R_{dwn} .
- **Over-charge detection delay time, Release delay time 2 --- [Circuit 6]**
Set $V_2 = 0V$. Increase V_1 from the voltage $V_C-0.2V$ to $V_C+0.2V$ rapidly within $10\mu s$. Over-charge detection delay time t_c is the time needed for VCO to go "Low" just after the change of V_1 .
Next, set $V_2 = 1V$ and decrease V_1 from $V_C+0.2V$ to $V_C-0.2V$ rapidly within $10\mu s$. Over-charge release delay time t_{rel2} is the time needed for VCO to go "High" just after the change of V_1 .
- **Over-discharge detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V_2 = 0V$. Decrease V_1 from the voltage $V_{dc}+0.2V$ to $V_{dc}-0.2V$ rapidly within $10\mu s$. Over-discharge detection delay time t_{dc} is the time needed for VDO to go "Low" just after the change of V_1 .
Next, set $V_2 = -1V$ and increase V_1 from $V_{dc}-0.2V$ to $V_{dc}+0.2V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of over-discharge is the time needed for VDO to go "High" just after the change of V_1 .
- **Charge over-current detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V_1 = 3.0V$ and $V_2 = 0V$. Decrease V_2 from $0V$ to $-1V$ rapidly within $10\mu s$. Charge over-current delay time t_{ic} is the time needed for VCO to go "Low" just after the change of V_2 .
Next, increase V_2 from $-1V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of charge over-current is the time needed for VCO to go "High" just after the change of V_2 .
- **Discharge over-current detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V_1 = 3.0V$ and $V_2 = 0V$. Increase V_2 from $0V$ to $1V$ rapidly within $10\mu s$. Discharge over-current delay time t_{dc} is the time needed for VDO to go "Low" just after the change of V_2 .
Next, decrease V_2 from $1V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of discharge over-current is the time needed for VDO to go "High" just after the change of V_2 .
- **Load short-circuiting detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V_1 = 3.0V$ and $V_2 = 0V$. Increase V_2 from $0V$ to $3.0V$ rapidly within $10\mu s$. Load short-circuiting detection delay time t_{short} is the time needed for VDO to go "Low" just after the change of V_2 .
Next, decrease V_2 from $3.0V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of load short-circuiting is the time needed for VDO to go "High" just after the change of V_2 .

Measurement Circuits

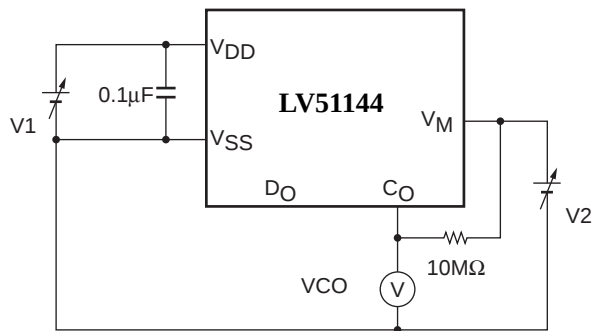
• Circuit 1



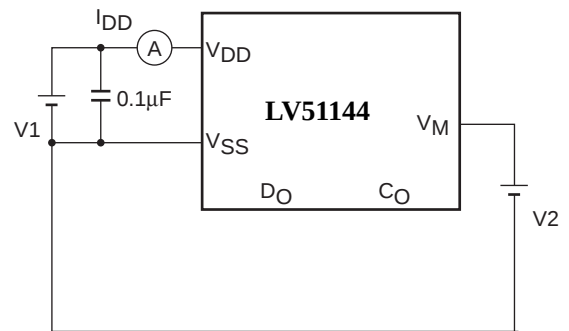
• Circuit 2



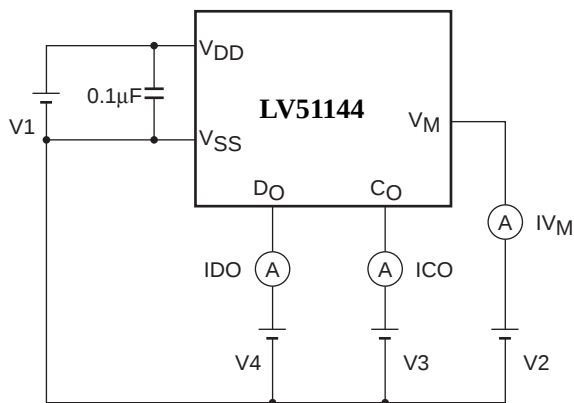
• Circuit 3



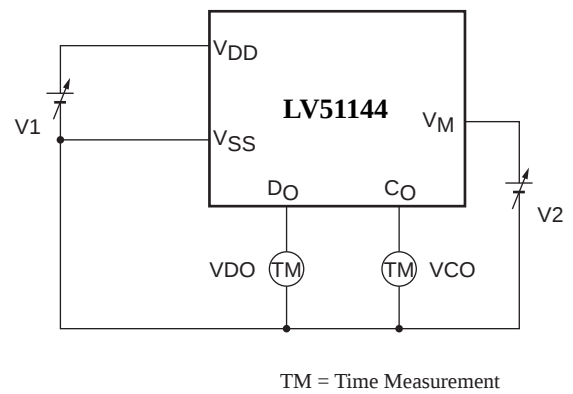
• Circuit 4



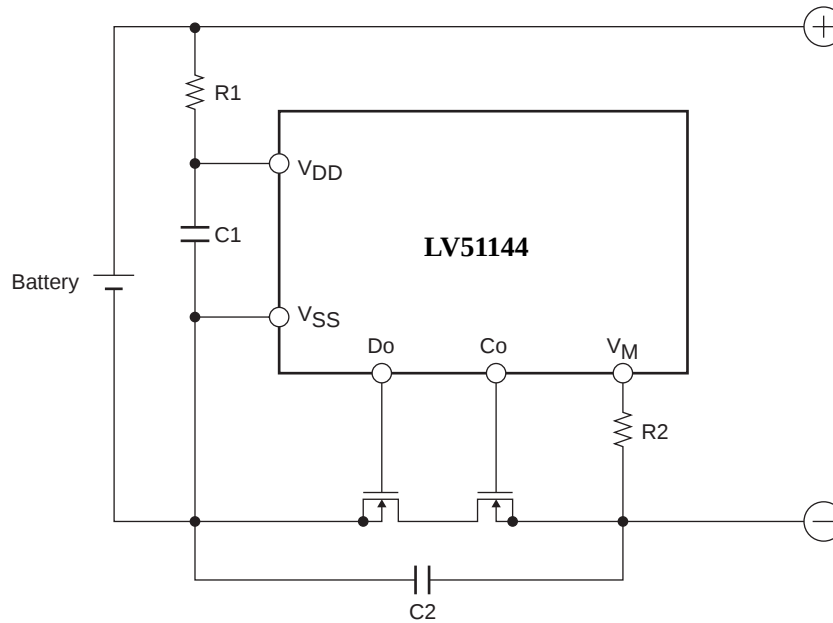
• Circuit 5



• Circuit 6



Application Circuit Example



External Components

Items	Symbol	Recommended value
Resistor 1	R1	330Ω
Capacitor 1	C1, 2	0.1μF
Resistor 2	R2	3.9kΩ

- The supply voltage (V_{DD}) to this IC is stabilized by R1 and C1. Moreover, R1 and R2 act as the current restriction resistances at the time of reverse-connecting a charger, or at the time of connecting a charger which outputs the voltage exceeding the absolute maximum rating of this IC. Be sure to connect these components.
- If the value of R1 is too large, the over-charge detection voltage will become high due to the current consumption of this IC. 330Ω is recommended.
- If the value of C1 is too small, this IC may be in a shutdown state at the time of the discharge over-current or the load short-circuiting. 0.1μF is recommended.
- Use the value within the limits shown in the table about the value of R2. In order to reduce the current at the time of reverse-connecting a charger, we recommend to choose R1 and R2 so that the sum total of resistance values is more than 4kΩ. The recommended value of R2 is 3.9kΩ.

Note 1 : The connection diagram and each value of external components shown above are just recommendation. Including a battery and FETs, determine the circuit after sufficient evaluation about your actual application. These numbers don't mean to guarantee the characteristic of the IC.

Note 2 : The IC is susceptible to static electricity and some pins are easily damaged by it. Handle the IC carefully.

Description of Operation

- Normal condition

This IC monitors the battery voltage (V_{DD}) and the voltage of V_M terminal, and controls charge and discharge.

If the battery voltage (V_{DD}) is in the range from the over-discharge detection voltage (V_{dc}) to the over-charge detection voltage (V_C) and the V_M terminal voltage is in the range from the charge over-current detection voltage (V_{Ic}) to the discharge over-current detection voltage (V_{Idc}), this IC turns on both the charge and discharge control FETs. This state is called the normal condition, and charge and discharge are possible together.

- Discharge over-current detection, Load short-circuiting detection

When the discharge current becomes equal to or higher than the specified value under the normal condition, and if the V_M terminal voltage is in the range from the discharge over current detection voltage (V_{Idc}) to the short-circuiting detection voltage (V_{short}) and that state is maintained during more than the discharge over-current detection delay time (t_{idc}), this IC turns off the discharge control FET to stop discharge. This state is called the discharge over-current condition.

At that time, if the V_M terminal voltage is equal to or higher than V_{short} and that state is maintained during more than the load short-circuiting detection delay time (t_{short}), this IC turns off the discharge control FET to stop discharge. This state is called the load short-circuiting detection condition.

While load is connected, in both conditions, the V_M terminal voltage equals to V_{DD} potential due to the load, but it falls by the discharge over-current release resistance (R_{dwn}) when the load is removed and the resistance between (+) and (-) terminals of battery pack (refer to "Application Circuit Example") becomes larger than the value which enables the automatic return.

Then the V_M terminal voltage becomes less than V_{Idc} , and if that state is maintained during more than the release delay time 1 (t_{rel1}), this IC returns to normal condition.

Note : The resistance value between (+) and (-) terminals of battery pack for automatic return changes with battery voltage (V_{DD}) or V_{Idc} . The standard is expressed with the following equation.

$$\text{Resistance value for automatic return} = R_{dwn} \times (V_{DD} / V_{Idc} - 1)$$

- Charge over-current detection

When the charge current becomes equal to or higher than the specified value under the normal condition, if the V_M terminal voltage becomes less than the charge over-current detection voltage (V_{Ic}) and that state is maintained during more than the charge over-current detection delay time (t_{ic}), this IC turns off the charge control FET to stop charge. This state is called the charge over-current detection condition.

Then the V_M terminal voltage becomes equals to or higher than V_{Ic} and that state is maintained during more than the release delay time 1 (t_{rel1}) when the charger is removed and the load is connected, this IC returns to the normal condition.

- Over-charge detection

When the battery voltage (V_{DD}) under the normal condition becomes equal to or higher than the over-charge detection voltage (V_C) and that state is maintained during more than the over-charge detection delay time (t_c), this IC turns off the charge control FET and stops charge. This state is called the over-charge detection condition. Release from the over-charge detection condition includes following three cases.

- (1) When V_{DD} falls to V_c without load and that state is maintained during more than the delay time 2 (t_{rel2}), this IC turns on the charge control FET and returns to the normal condition.
- (2) When the load is installed and discharge starts, the discharge current flows through the internal parasitic diode of the charge control FET. Then the V_M terminal voltage rises to only the V_f voltage of the internal parasitic diode from V_{SS} potential. At this time, if the V_M terminal voltage is higher than the discharge over-current detection voltage (V_{Idc}) and V_{DD} is equal to or less than V_C , this IC returns to the normal condition when this state continues more than the delay time 2 (t_{rel2}).
- (3) In case (2), if the V_M terminal voltage is higher than the discharge over-current detection voltage (V_{Idc}) and V_{DD} is equal to or higher than V_C , battery is discharged until V_{DD} becomes less than V_C , and then this IC returns to the normal condition when this state continues more than the delay time 2 (t_{rel2}).

- Over-discharge detection

When the battery voltage (V_{DD}) under the normal condition becomes equal to or less than the over-discharge detection voltage (V_{dc}) and that state continues for more than the over-discharge detection time (t_{dc}), this IC turns off the discharge control FET and stops discharging. This state is called the over-discharge detection condition. Recovery from the over-discharge detection condition is achieved only by connecting the charger.

- Return from over-discharge

When the charger is connected and charging starts, the charge current flows through the internal parasitic diode of the discharge control FET. When V_{DD} becomes higher than V_{dc} and that state continues for more than the delay time 1(t_{rel1}), this IC is released from the over-discharge detection condition automatically and returns to the normal condition.

If V_{DD} is less than V_{dc} , this IC returns to the normal condition when V_{DD} becomes equal to or higher than V_{dc} , and this state continues more than delay time 1 (t_{rel1}).

This IC stops all internal circuits (Shutdown condition) after detecting the over-discharge and reduces current consumption. (Max 0.1 μ A, at $V_{DD} = 1.8V$)

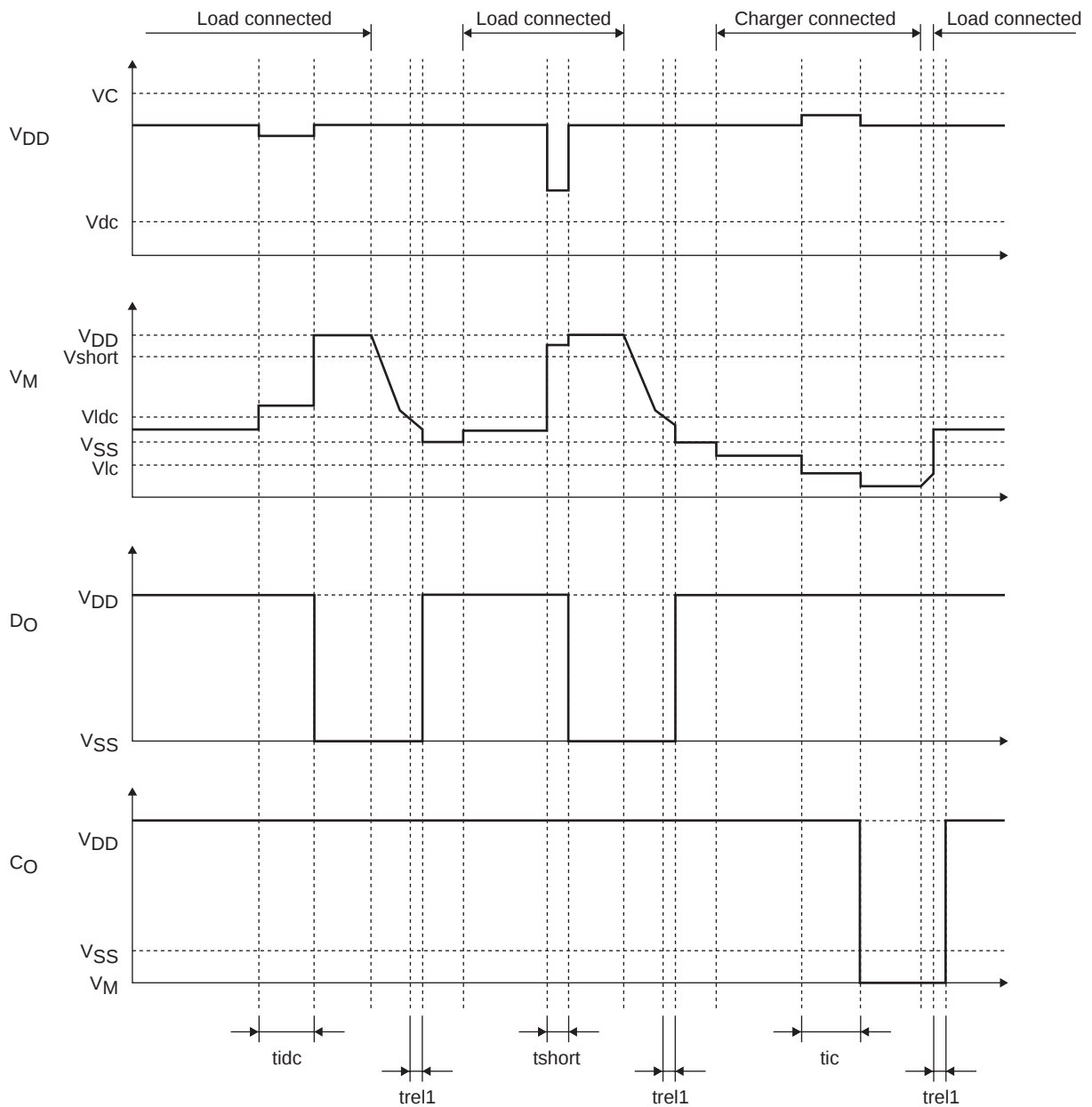
- Charge to 0V battery

- (1) 0V battery charge function

If the voltage of charger (the voltage between V_{DD} and V_M) is larger than the 0V battery charge starting charger voltage (V_{cha}), 0V battery charge becomes possible when CO terminal outputs V_{DD} terminal potential and turns on the charge control FET.

Timing Chart

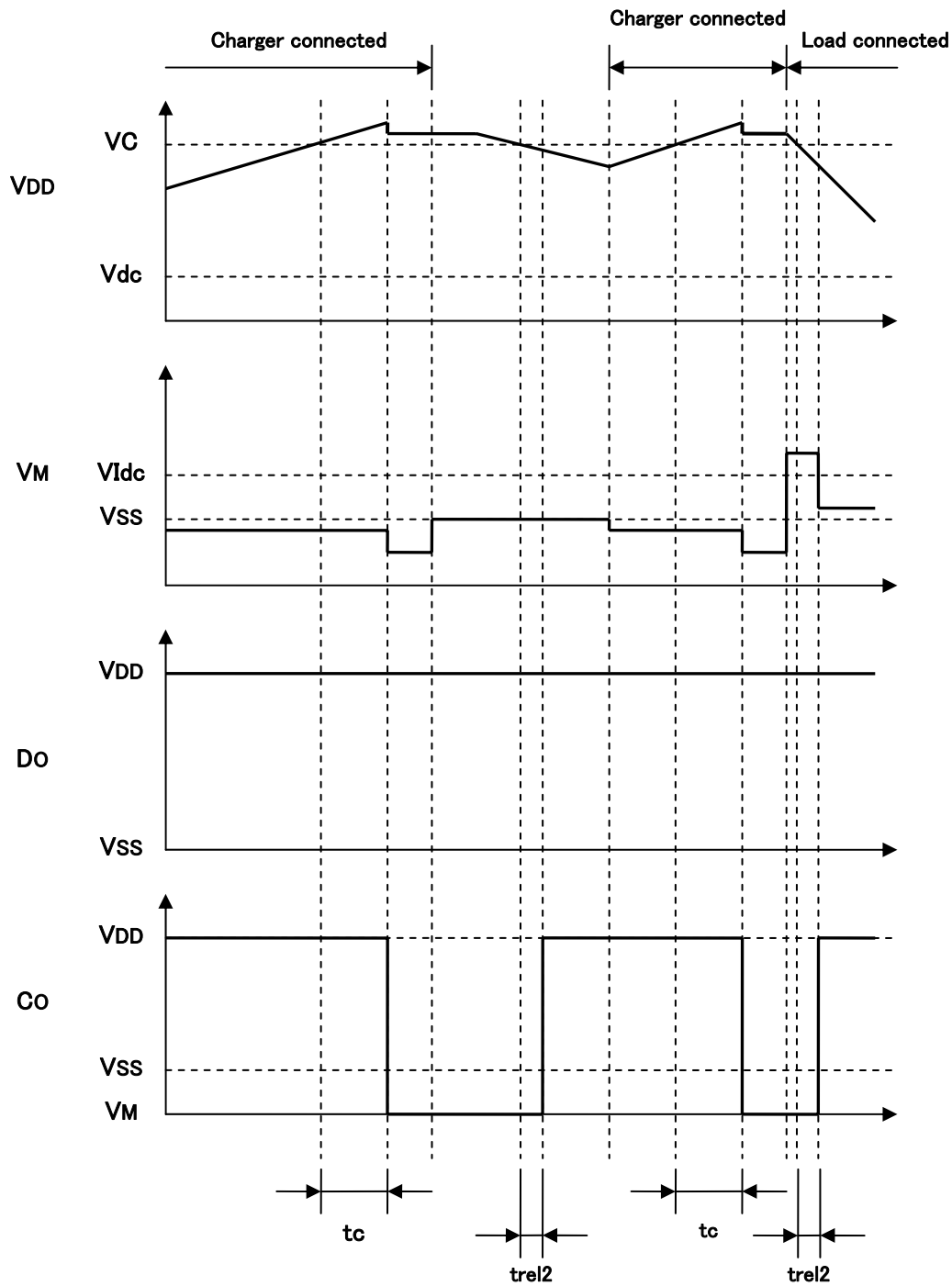
- Discharge over-current detection, Load short-circuiting detection, Charge over-current detection



V_C : Over-charge detection voltage
 V_{dc} : Over-discharge detection voltage
 V_{Ic} : Charge over-current detection voltage
 V_{Idc} : Discharge over-current detection voltage
 V_{short} : Load short-circuiting detection voltage

t_{ic} : Charge over-current detection delay time
 t_{dc} : Discharge over-current detection delay time
 t_{short} : Load short-circuiting detection delay time
 t_{rel1} : Release delay time 1

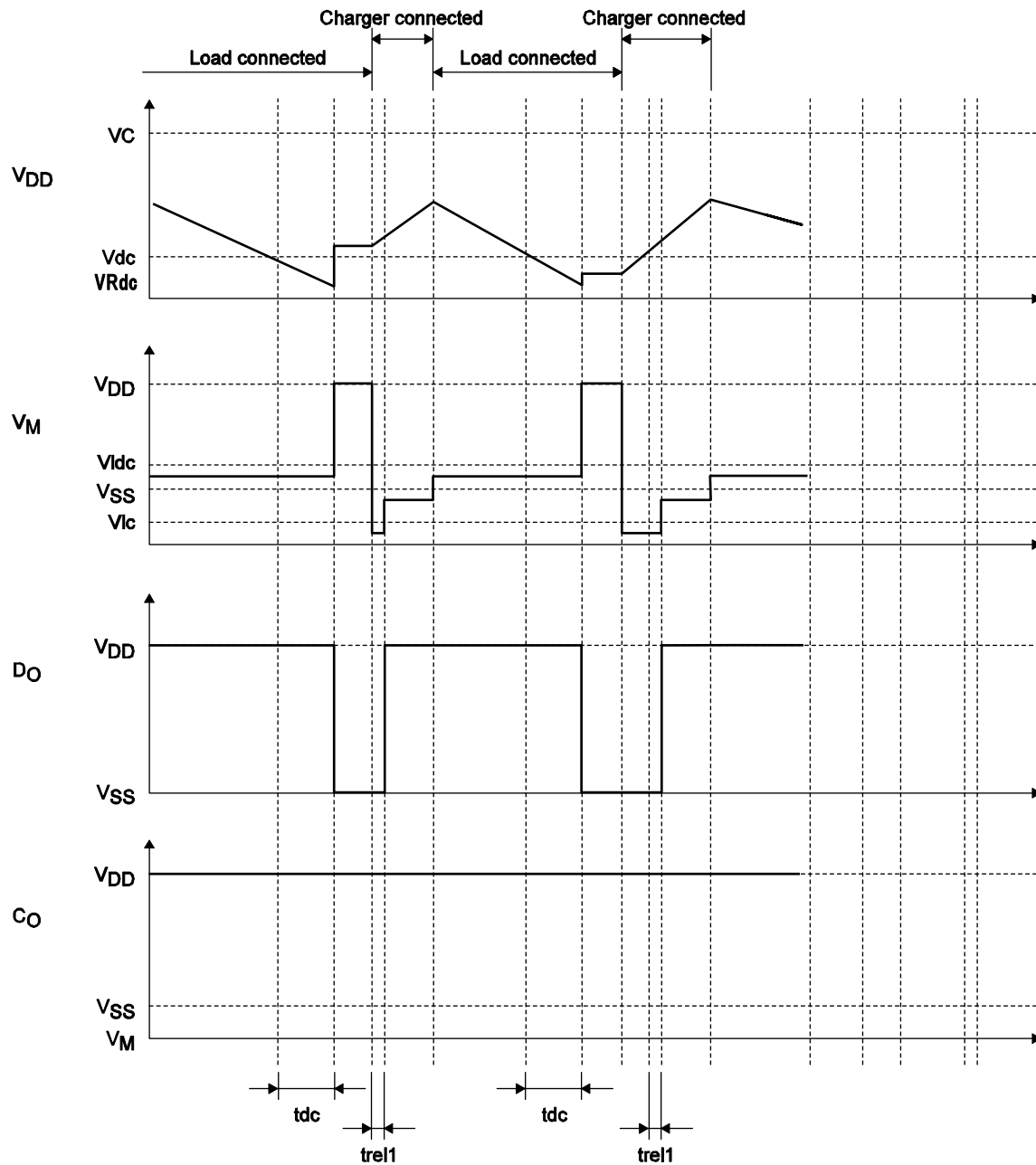
• Over-charge detection



VC : Over-charge detection voltage
Vdc : Over-discharge detection voltage
VIdc : Discharge over-current detection voltage

tc : Over-charge detection delay time
trel2 : Release delay time 2

• Over-discharge detection



V_C : Over-charge detection voltage
 V_{dc} : Over-discharge detection voltage
 V_{Rdc} : Over-discharge return voltage
 V_{ic} : Charge over-current detection voltage
 V_{dc} : Discharge over-current detection voltage

t_{dc} : Over-discharge detection delay time
 t_{rel1} : Release delay time 1

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