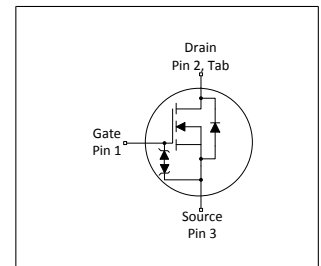
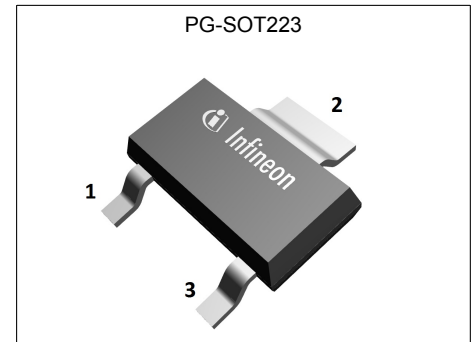


MOSFET

600V CoolMOS™ P7 Power Transistor

The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600V CoolMOS™ P7 series combines the experience of the leading SJ MOSFET supplier with high class innovation, and is the only platform that enables an $R_{DS(on)} \cdot A$ below $10\text{m}\Omega \cdot \text{mm}^2$. The 600V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series and continues to offer all the benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler



Features

- Suitable for hard and soft switching (PFC and LLC)
- Integrated Gate Resistor to enable excellent balance between efficiency and ease of use
- $R_{DS(on)} \cdot A$ below $10\text{m}\Omega \cdot \text{mm}^2$, enables low $R_{DS(on)}$ /package
- ESD diode from 180mOhms and above
- Series qualified for a variety of industrial and consumer grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Can be in a wide variety of applications and power ranges
- Increased power density solutions due to smaller packages
- Protection in various manufacturing environments
- Products tailored for either consumer or industrial applications



Potential applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	360	mΩ
$Q_{g,typ}$	13	nC
$I_{D,pulse}$	26	A
$E_{oss@400V}$	1.6	μJ
Body diode di/dt	900	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPN60R360P7S	PG-SOT223	60S360	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	9 6.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	26	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	27	mJ	$I_D=2.50\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.14	mJ	$I_D=2.50\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	2.50	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	7	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	n.a.
Continuous diode forward current	I_S	-	-	9.0	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	26	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	900	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$; DPAK / IPAK equivalent.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_g

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJS}	-	-	17.4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	160	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	75	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.14mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	1000	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.300 0.697	0.360 -	Ω	$V_{GS}=10V$, $I_D=2.7A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=2.7A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	6.2	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	555	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	10	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	20	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	214	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.7A$, $R_G=10.0\Omega$; see table 9
Rise time	t_r	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.7A$, $R_G=10.0\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	42	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.7A$, $R_G=10.0\Omega$; see table 9
Fall time	t_f	-	10	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.7A$, $R_G=10.0\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3	-	nC	$V_{DD}=400V$, $I_D=2.7A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	4	-	nC	$V_{DD}=400V$, $I_D=2.7A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	13	-	nC	$V_{DD}=400V$, $I_D=2.7A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	$V_{DD}=400V$, $I_D=2.7A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=2.7A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	145	-	ns	$V_R=400V$, $I_F=1.0A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.74	-	μC	$V_R=400V$, $I_F=1.0A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	11	-	A	$V_R=400V$, $I_F=1.0A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

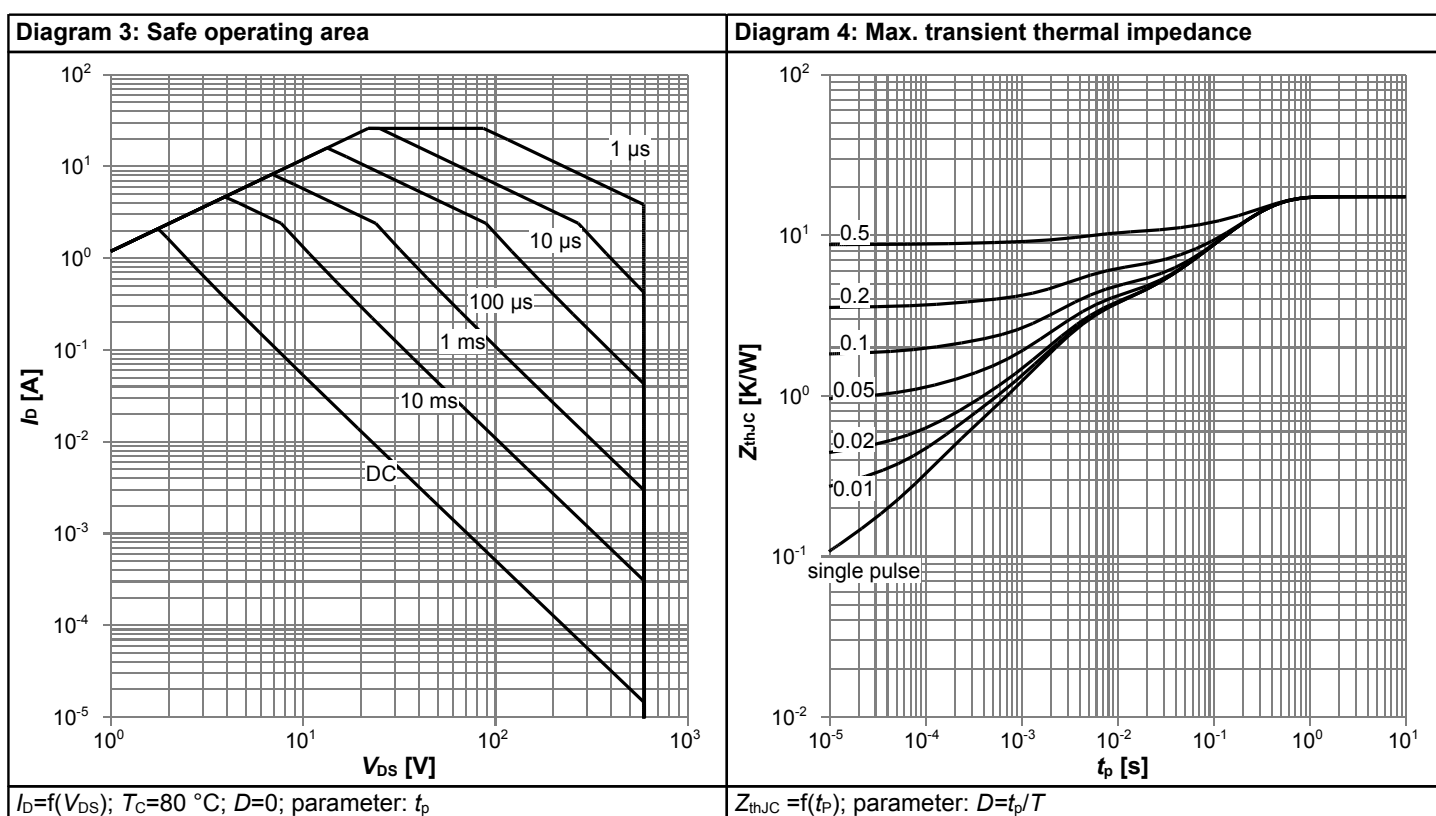
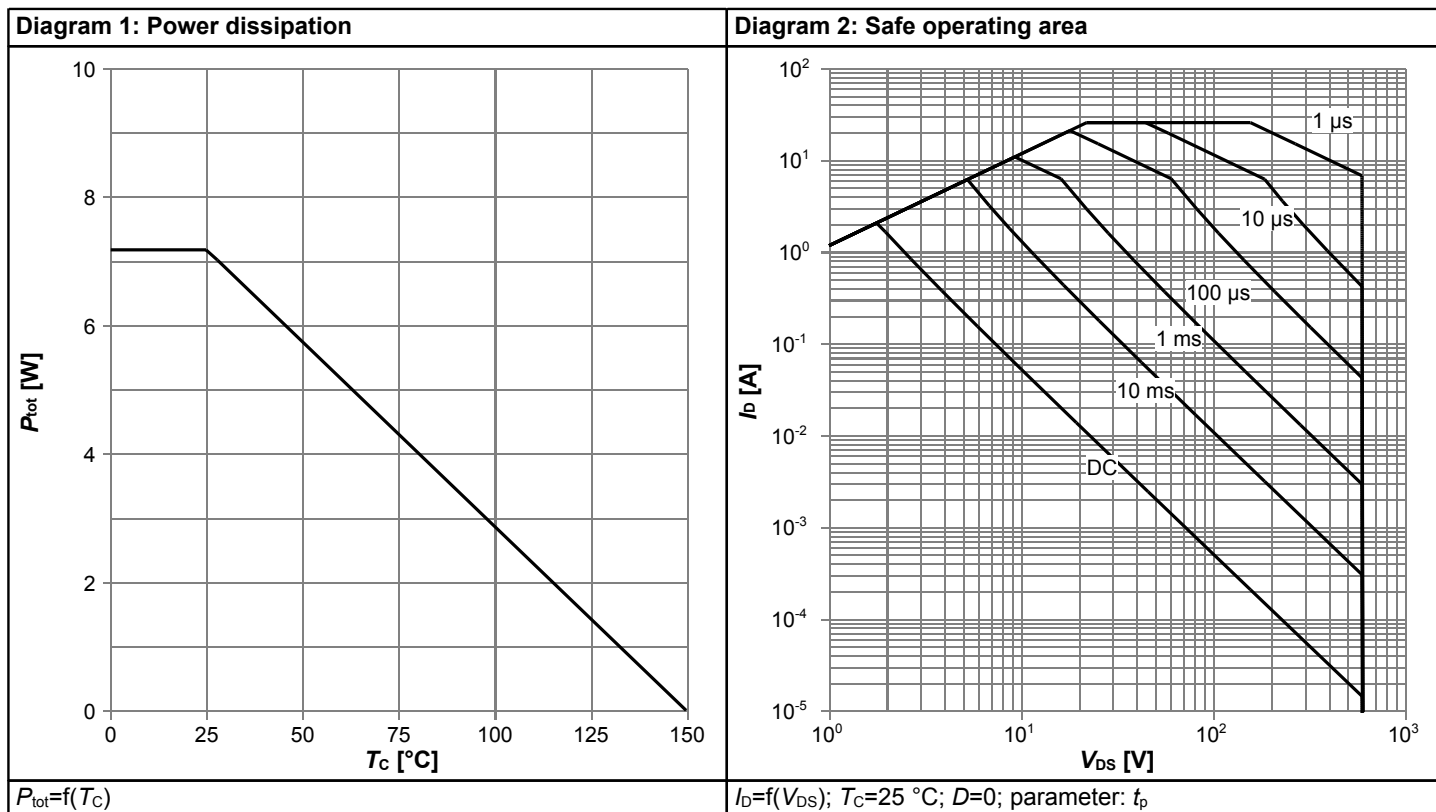
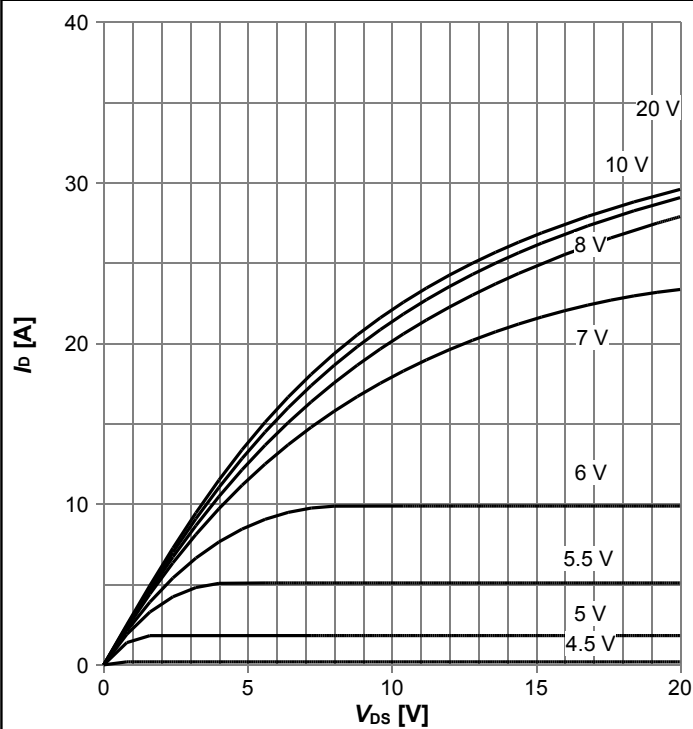
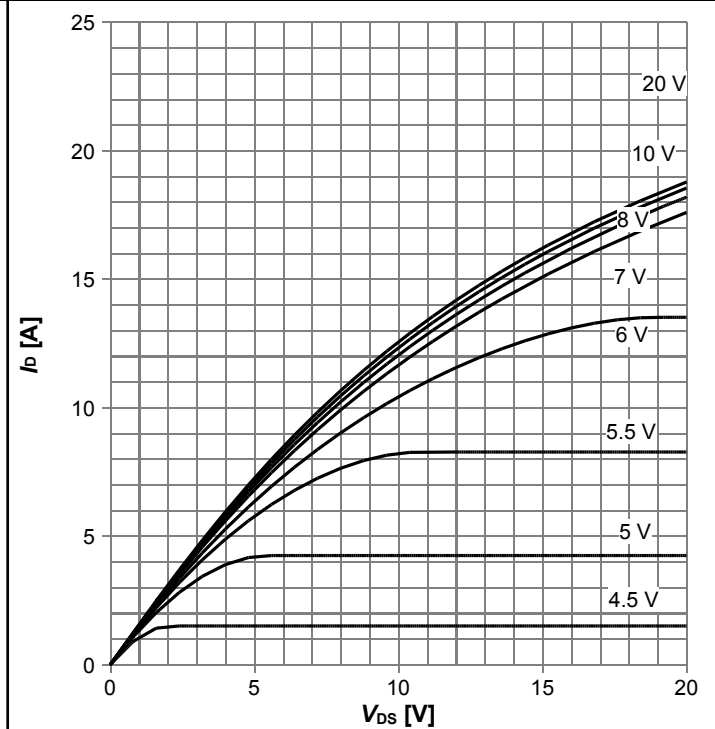


Diagram 5: Typ. output characteristics



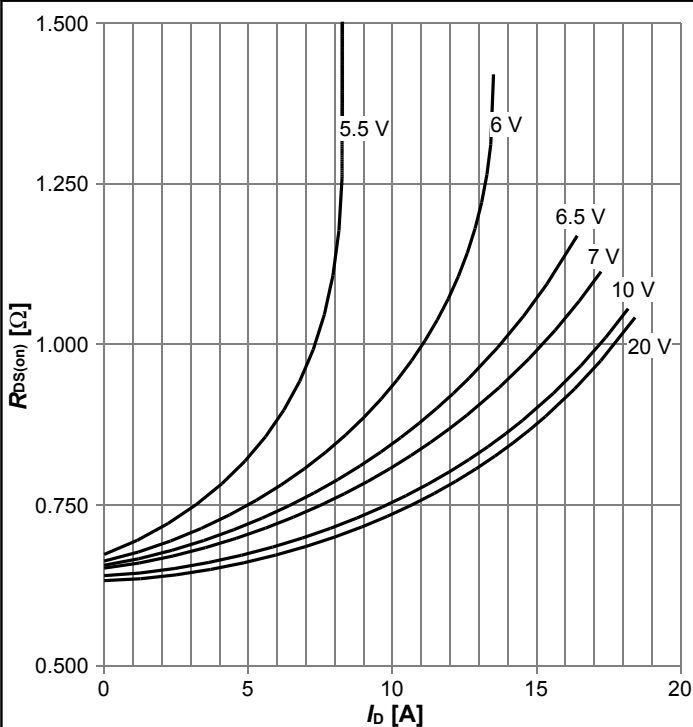
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



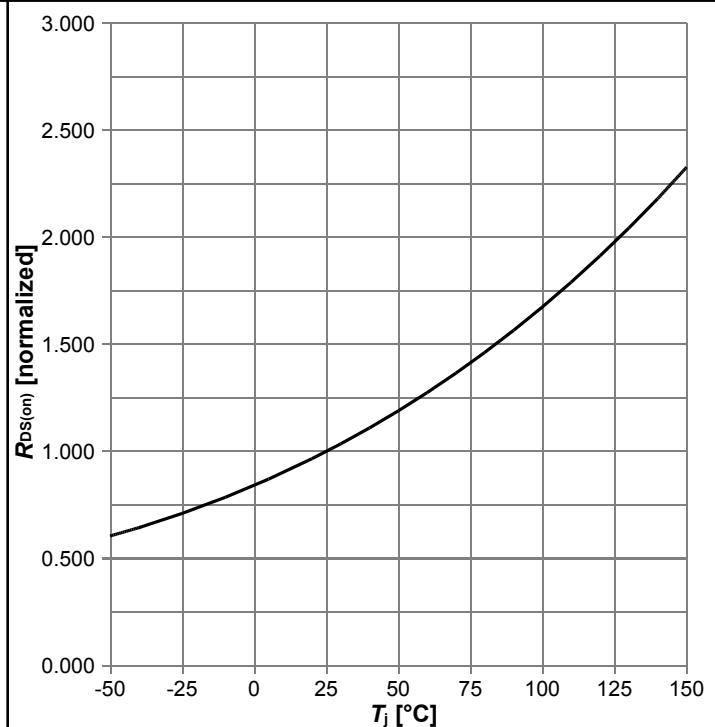
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



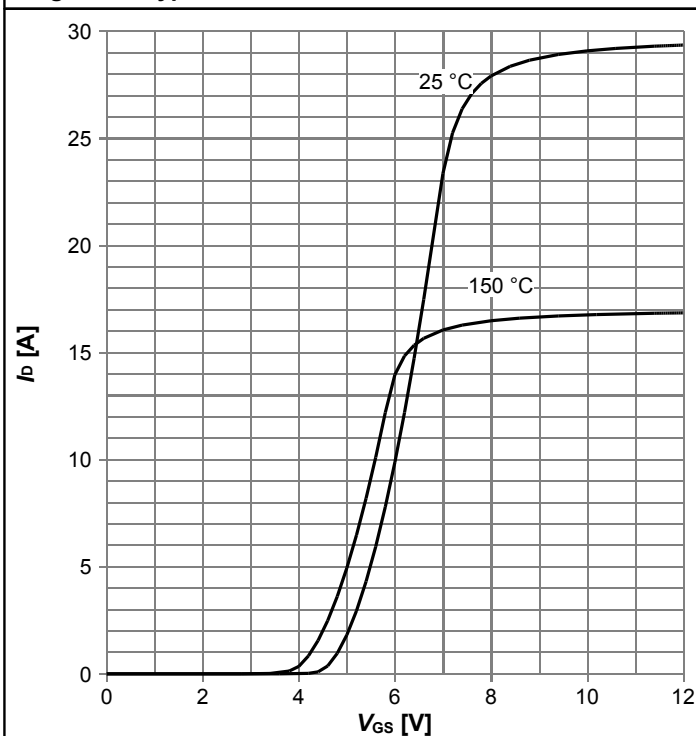
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



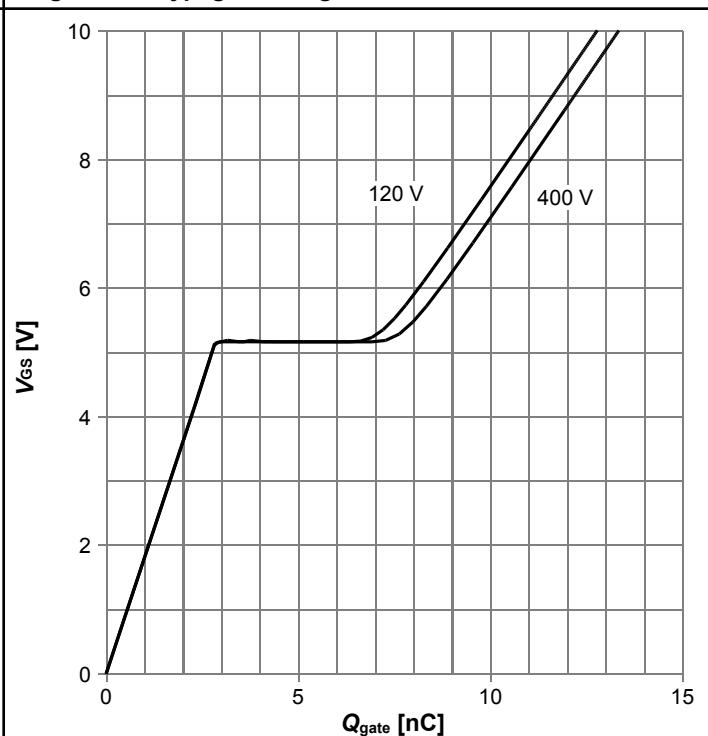
$R_{DS(on)} = f(T_j)$; $I_D = 2.7\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



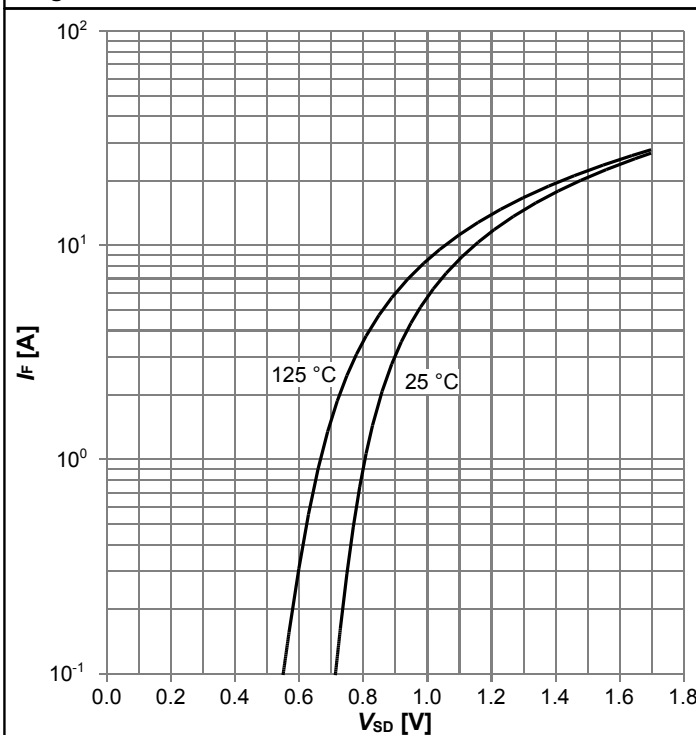
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



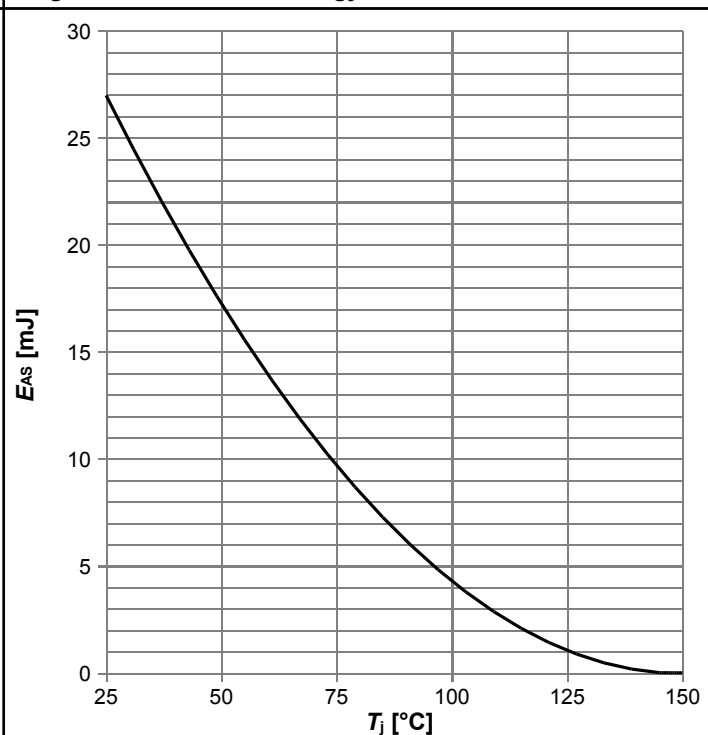
$V_{GS} = f(Q_{gate})$; $I_D = 2.7$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



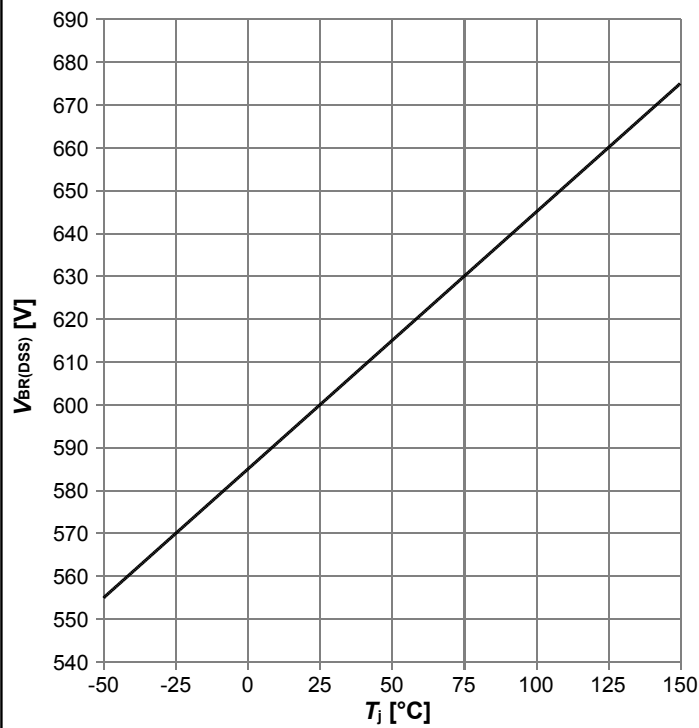
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



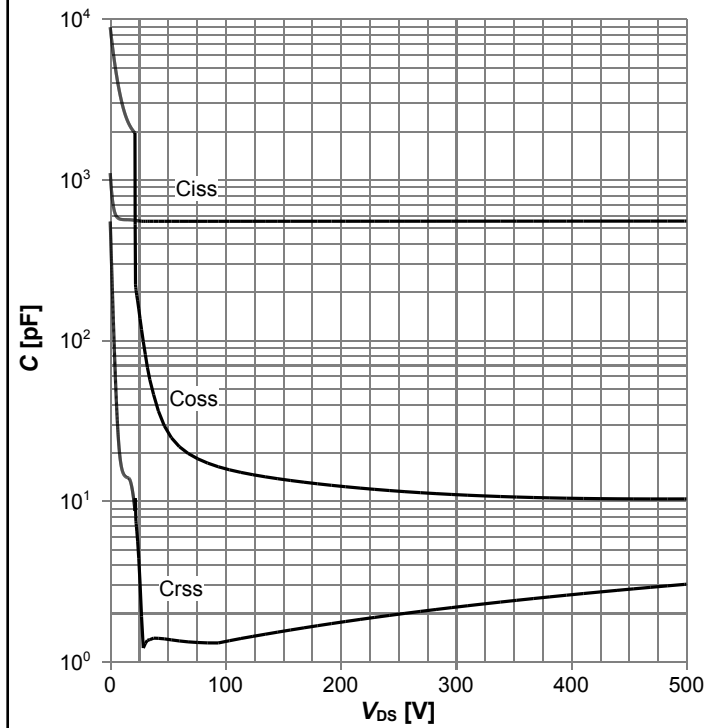
$E_{AS} = f(T_j)$; $I_D = 2.5$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



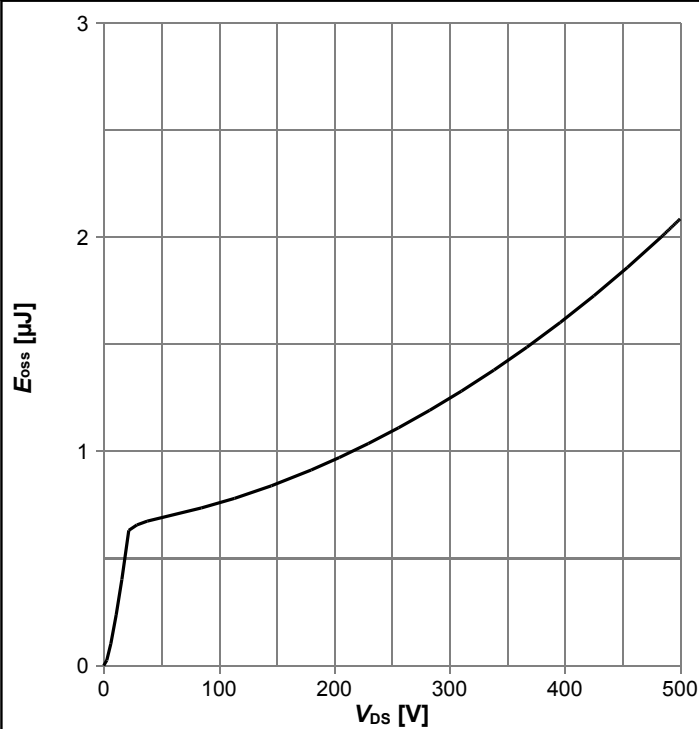
$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

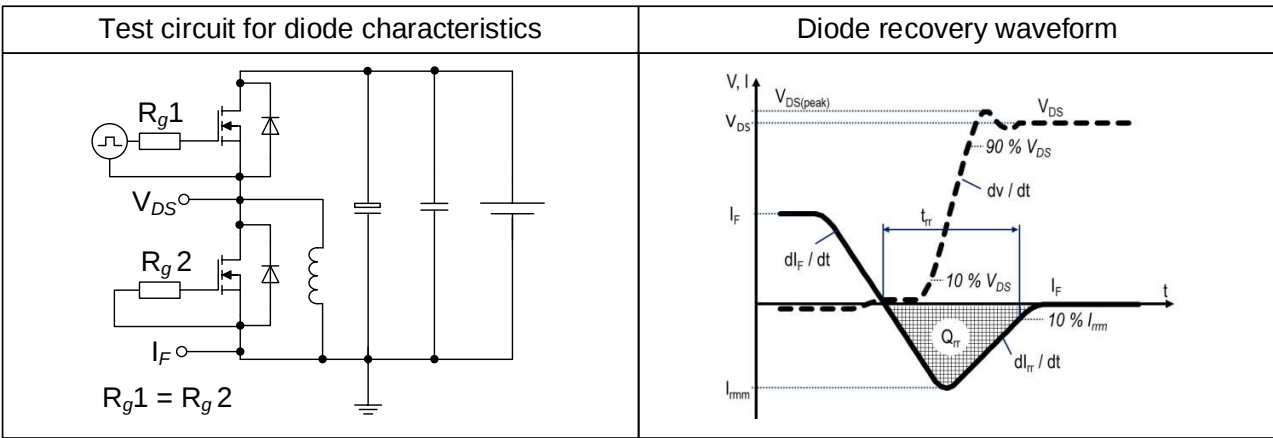


Table 9 Switching times

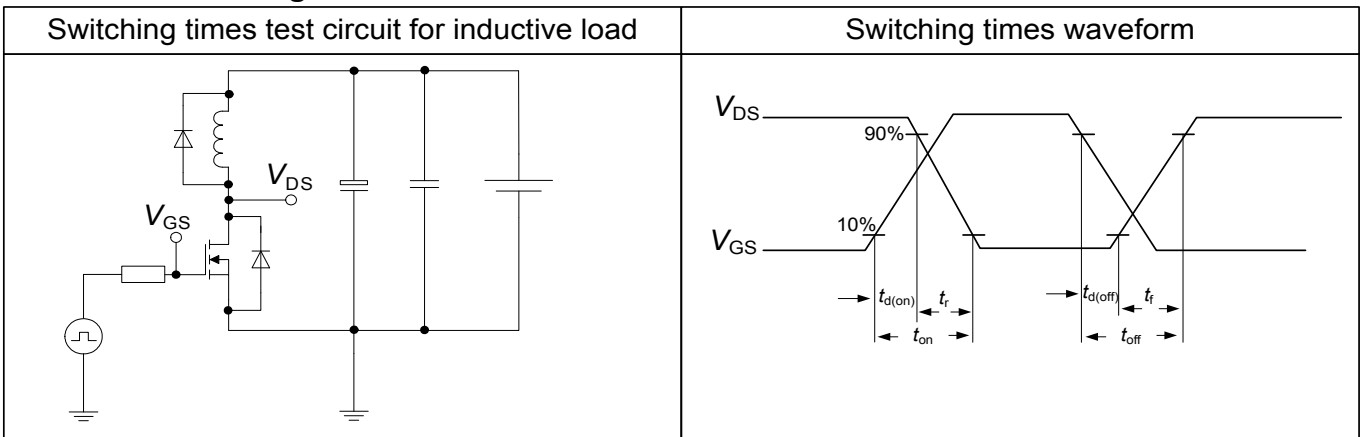
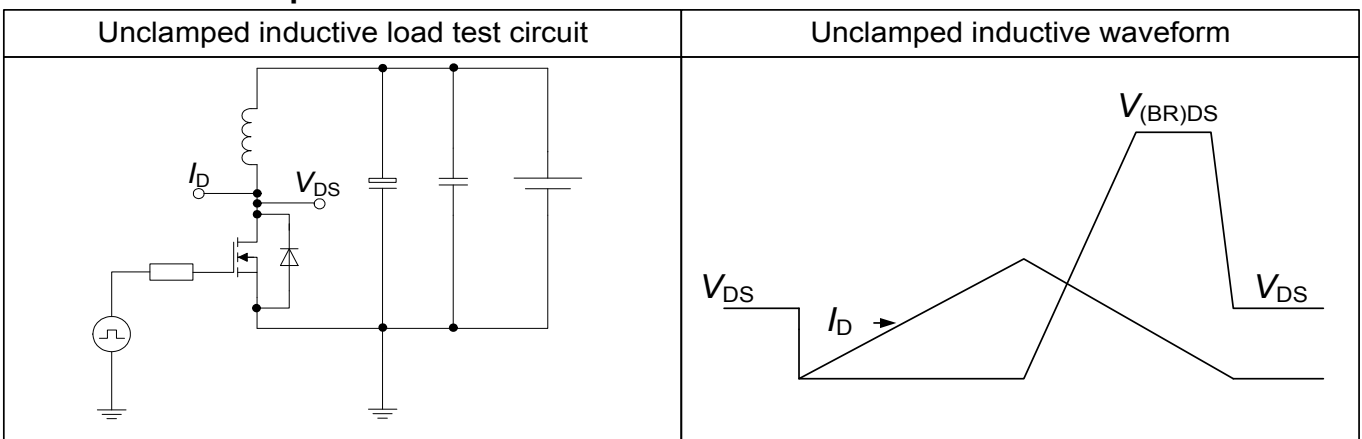
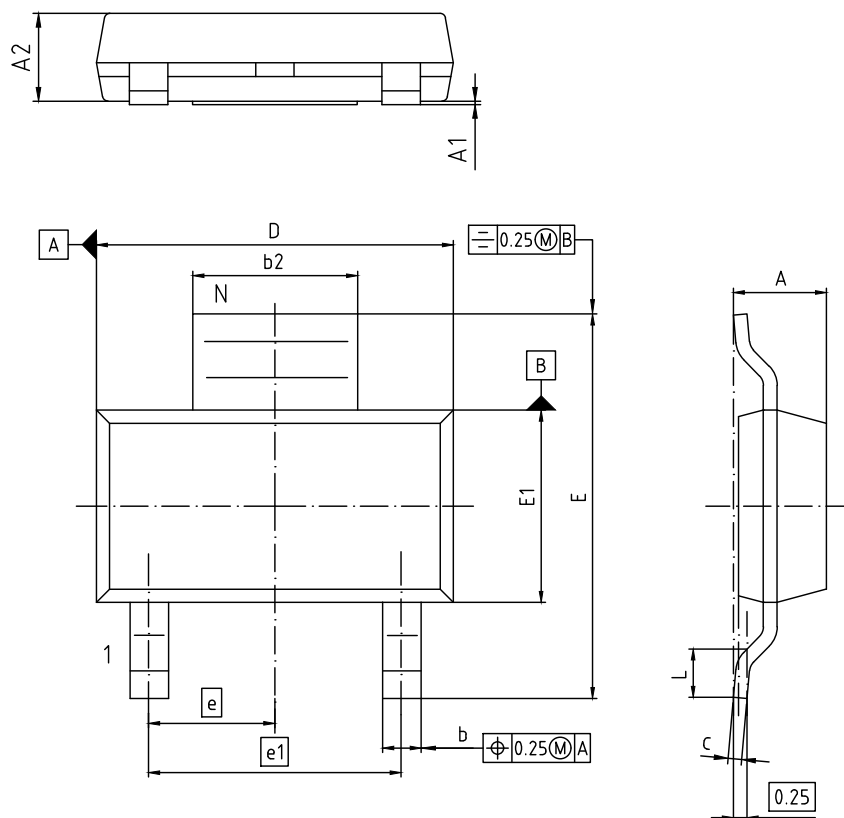


Table 10 Unclamped inductive load



6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

DOCUMENT NO. Z8B00180553
SCALE 0 2.5 5mm
EUROPEAN PROJECTION
ISSUE DATE 24-02-2016
REVISION 01

Figure 1 Outline PG-SOT223, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS P7 Webpage: www.infineon.com
- IFX CoolMOS P7 application note: www.infineon.com
- IFX CoolMOS P7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPN60R360P7S

Revision: 2017-06-23, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-06-23	Release of final version

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Published by

Infineon Technologies AG

81726 München, Germany

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