2N6767, 2N6768

File Number **1898**

Power MOS Field-Effect Transistors

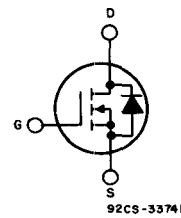
N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

12A and 14A, 350V - 400V
$r_{DS(on)}$ = 0.4Ω and 0.3Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

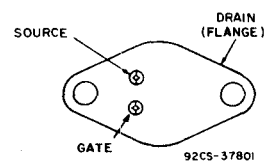


The 2N6767 and 2N6768 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6767 and 2N6768 are supplied in the JEDEC TO-204AA steel package.

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6767		2N6768	
*DRAIN-SOURCE VOLTAGE	V_{DSS}	350		400	V
*DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350		400	V
*GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D				
At T_C = 25°C		12		14	A
At T_C = 100°C		7.75		9	A
Pulsed	I_{DM}	20		25	A
*POWER DISSIPATION	P_T				
At T_C = 25°C			150		W
Above T_C = 25°C, Derate Linearly			1.2		W/°C
INDUCTIVE CURRENT, CLAMPED (L = 100μH)	I_{LM}	20		25	A
*OPERATING AND STORAGE TEMPERATURE	T_i, T_{stg}		-55 to +150		°C
*LEAD TEMPERATURE (0.063 in. or 1.6 mm from case for 10 s)	T_L		300		°C

*JEDEC REGISTERED DATA

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 180V, I_D = 9.0A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	
t_f	Fall Time	ALL	–	–	75*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	*Continuous Source Current* (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6768	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

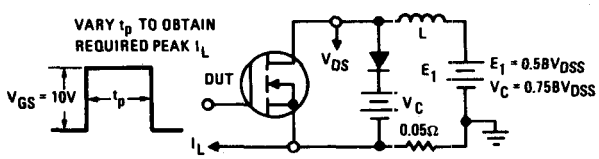


Fig. 1 - Clamped inductive test circuit.

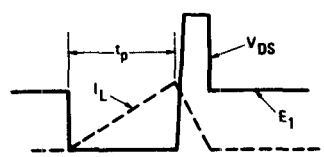


Fig. 2 - Clamped inductive waveforms.

2N6767, 2N6768

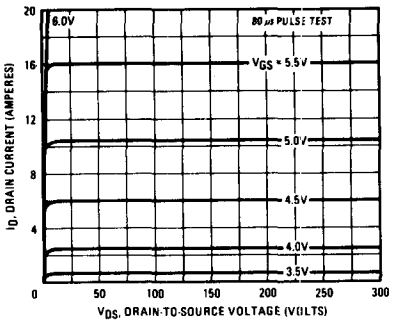


Fig. 3 - Typical output characteristics for both types.

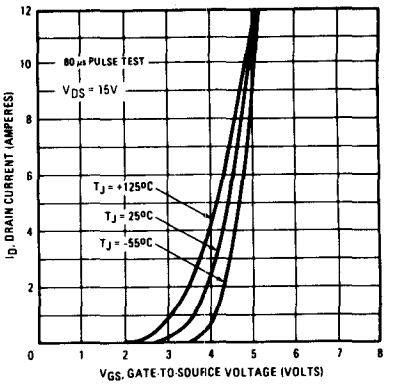


Fig. 4 - Typical transfer characteristics for both types.

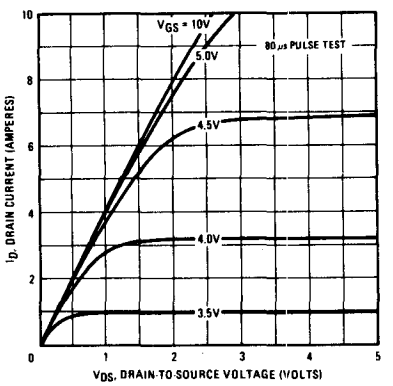


Fig. 5 - Typical saturation characteristics for the 2N6767.

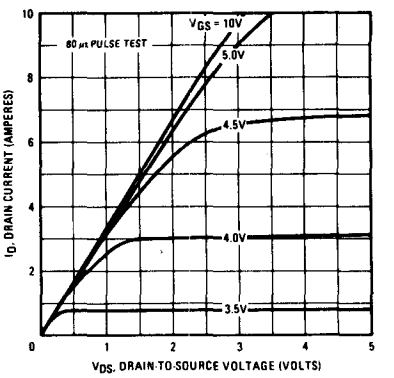


Fig. 6. - Typical saturation characteristics for the 2N6768.

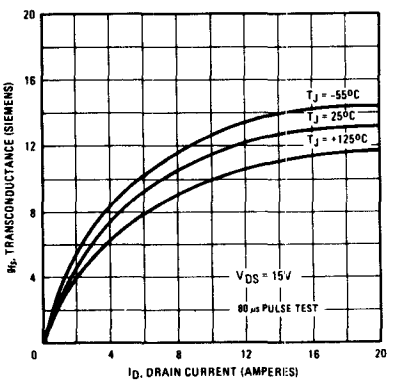


Fig. 7 - Typical transconductance versus drain current for both types.

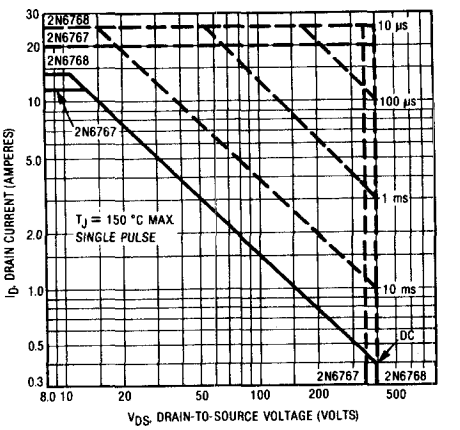


Fig. 8 - Maximum safe operating area for both types.

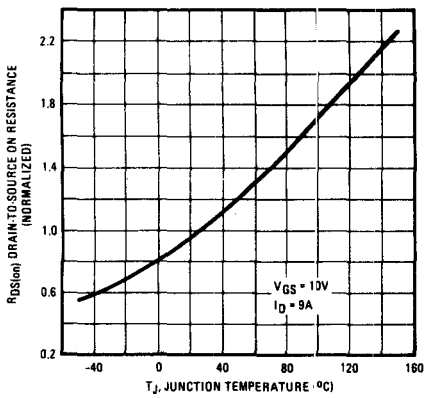


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

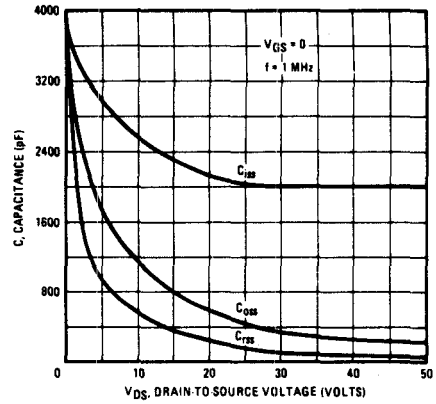


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

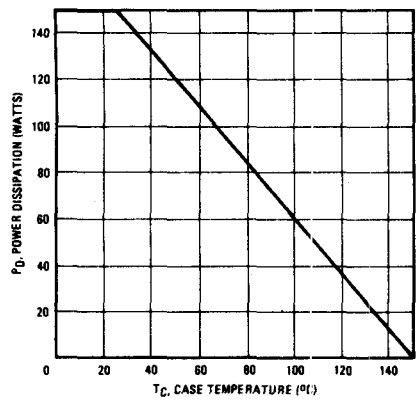


Fig. 11 - Power versus temperature derating curve for both types.

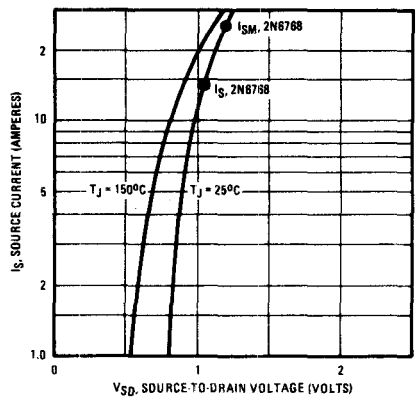


Fig. 12 - Typical body-drain diode forward voltage for both types.

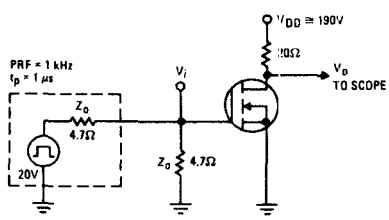


Fig. 13 - Switching time test circuit.

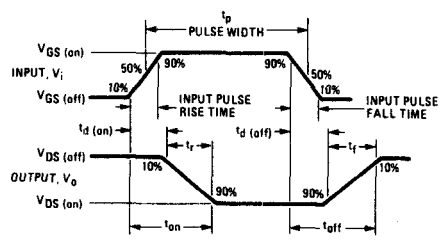


Fig. 14 - Switching time waveforms