DALLAS SEMICONDUCTOR

DS1283
Watchdog Timekeeper Chip

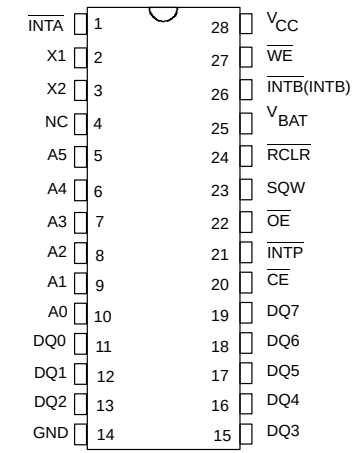
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years; valid leap year compersation up to 2100
- Watchdog timer restarts an out–of–control processor
- Alarm function provides notice of real time related occurrences
- Designed for battery operation
- Programmable interrupts and square wave outputs maintain 28–pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minutes/month at 25°C
- 50 bytes of user nonvolatile RAM
- Optional 28–pin SOIC surface mount package
- Low–power CMOS circuitry is maintained on less than 1 µA in standby mode
- Optional industrial temperature range –40°C to +85°C

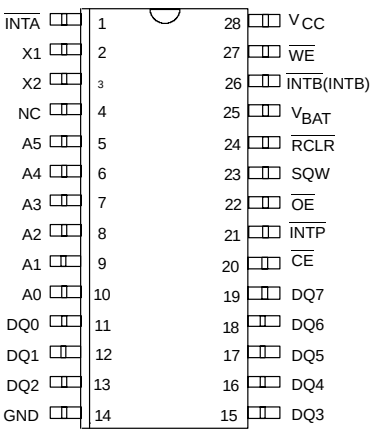
DESCRIPTION

The DS1283 Watchdog Timekeeper Chip is a self–contained real time clock, alarm, watchdog timer, and interval timer in a 28–pin JEDEC DIP or 28–pin SOIC surface mount package. The DS1283 is specifically designed to maintain internal operations from a single low voltage supply. In fact, the only two external components required by the DS1283 are a battery and crystal. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, V_{CC}, $\overline{RCLR}$, $\overline{INTB}$, and $\overline{INTP}$ see the DS1286 Watchdog Timekeeper data sheet.

PIN ASSIGNMENT



DS1283
28–PIN DIP (600 MIL)



DS1283S
28–PIN SOIC (330 MIL)

NOTE: Pin 4 must be left disconnected.

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	$\overline{INTA}$	O	Interrupt Output A (open drain)
2–3	X1,X2	I	32.768 KHz Crystal
4	NC	–	No Connection
5-10	A0-A5	I	Address Inputs: A5=Pin 5; A0=Pin 10
11	DQ0	I/O	Data Input/Output
12	DQ1	I/O	Data Input/Output
13	DQ2	I/O	Data Input/Output
14	GND	–	Ground
15	DQ3	I/O	Data Input/Output
16	DQ4	I/O	Data Input/Output
17	DQ5	I/O	Data Input/Output
18	DQ6	I/O	Data Input/Output
19	DQ7	I/O	Data Input/Output
20	$\overline{CE}$	I	Chip Enable
21	$\overline{INTP}$	O	Interrupt Output P (open drain)
22	$\overline{OE}$	I	Output Enable
23	SQW	O	Square Wave Output
24	$\overline{RCLR}$	I	RAM Clear
25	V_{BAT}	I	Battery Input
26	$\overline{INTB}$ (INTB)	O	Interrupt Output B (open drain)
27	$\overline{WE}$	I	Write Enable
28	V_{CC}	I	V_{CC} Input

PIN DESCRIPTIONS

X1, X2 – Connections for a standard 32.768 KHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a load capacitance (C_L) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks.”

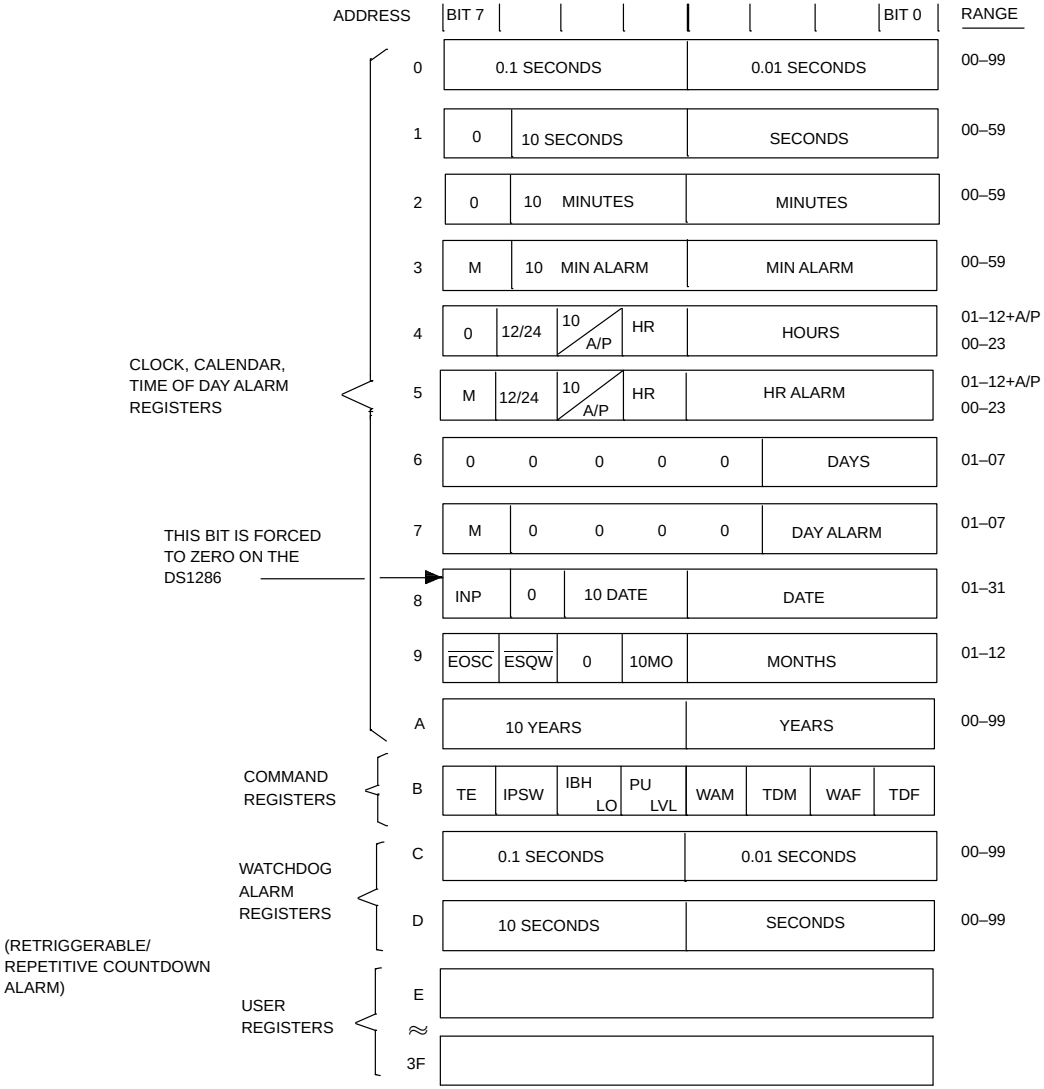
V_{BAT}, V_{CC} – Inputs for batteries or power supplies between 5.5 and 2.5 volts. The V_{CC} supply voltage should never exceed V_{BAT} + 0.3 volts. The V_{BAT} input is used to maintain all internal functions while the V_{CC} input is used to keep all inputs and outputs functional. Therefore, to keep the device fully functional, V_{BAT} and V_{CC} must be at the same voltage potential. As long as the supply voltages are between 4.5 and 5.5 volts, the timing and the input/output levels are guaranteed. In this mode, the active current drain is 2 mA ($CE=V_{IL}$) and the standby current drain is 0.5 mA ($CE=V_{IH}$). Data retention mode occurs when the V_{BAT} supply is between 5.5 and 2.5 volts and the V_{CC} supply is grounded. In the data retention mode the current drain is less than 1 µA maximum at 5.5 volts ($CE=V_{BAT}$–0.2 volts). The current drain specifications are stated with all outputs unloaded.

$\overline{RCLR}$ – The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of user nonvolatile RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (–0.3 to +0.8 volts). The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

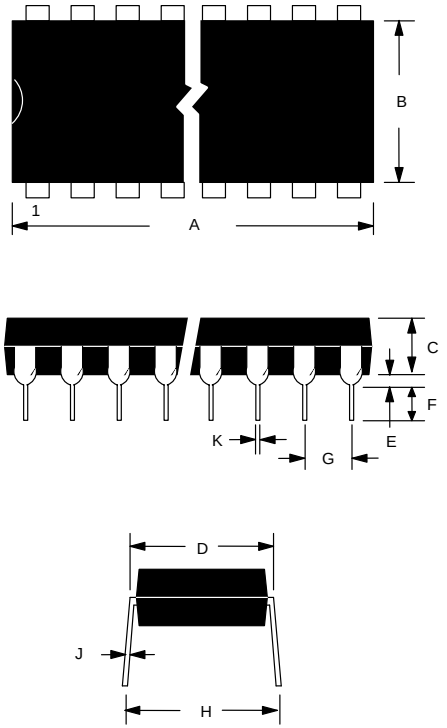
$\overline{INTB}$ – Interrupt B on the DS1283 operates identical to interrupt B on the DS1286 except that the sink and source current is limited to 500 µA. This pin should be pulled up or down if not used.

$\overline{INTP}$ – Interrupt P on the DS1283 was a missing or no connection pin on the DS1286. This interrupt works in the same manner as $\overline{INTA}$ as programmed by the IPSW bit. However, $\overline{INTP}$ is also logically ORed with the MSB of the date register (see Figure 1). This bit is called the INP bit on the DS1283 and is forced to zero on the DS1286. When the INP bit (interrupt P bit) is set to logical one, interrupt P will be held active low. When INP is set to logical zero, $\overline{INTP}$ is always at the same logic state as $\overline{INTA}$. This pin is an open drain capable of sinking 4 mA.

DS1283 WATCHDOG TIMEKEEPER REGISTERS Figure 1

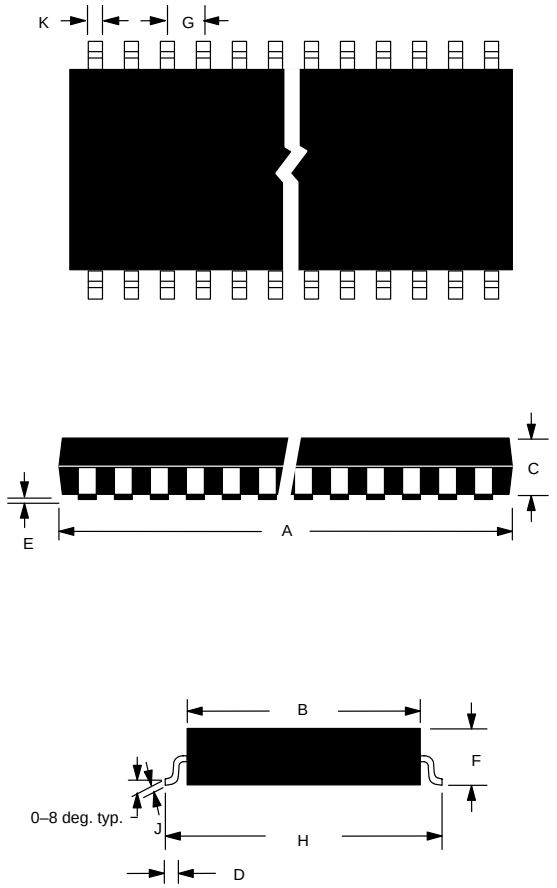


DS1283 28–PIN DIP



PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

DS1283 28–PIN SOIC



PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51