

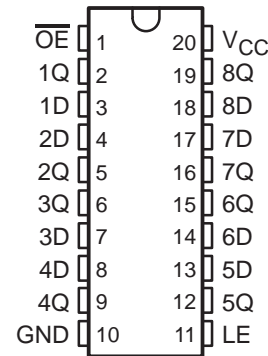
# CD74FCT373

## BiCMOS OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From  $V_{CC}$
- 48-mA Output Sink Current
- Controlled Output Edge Rates
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP

E, M, OR SM PACKAGE  
(TOP VIEW)



### description

The CD74FCT373 is an octal, transparent, D-type latch with 3-state outputs using a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

The outputs are transparent to the inputs when latch enable (LE) is high. When LE is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs. The latch operation is independent of output-enable ( $\overline{OE}$ ) input.

$\overline{OE}$  can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

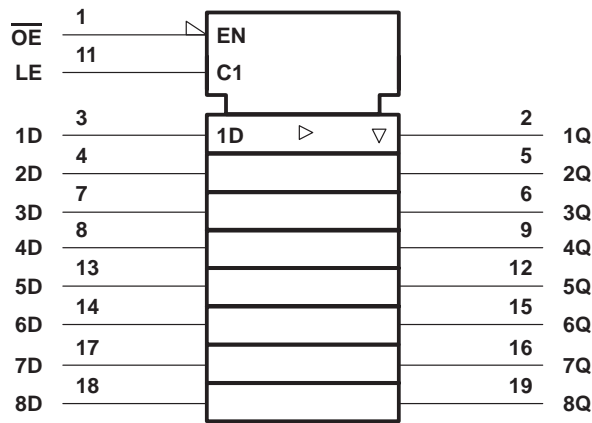
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WITH 3-STATE OUTPUTS

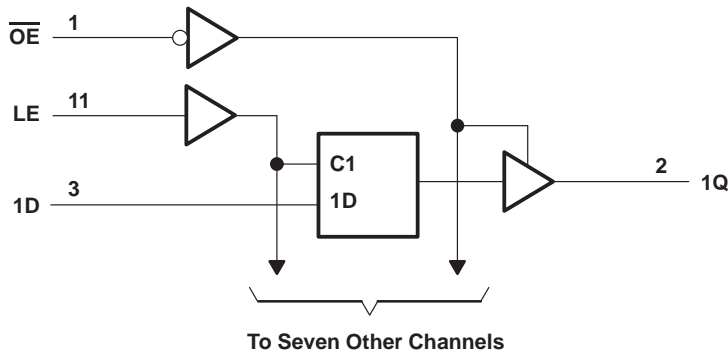
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

DC supply voltage range, $V_{CC}$	–0.5 V to 6 V
DC input diode current, $I_{IK}$ ( $V_I < -0.5$ V)	–20 mA
DC output diode current, $I_{OK}$ ( $V_O < -0.5$ V)	–50 mA
DC output sink current per output pin, $I_{OL}$	70 mA
DC output source current per output pin, $I_{OH}$	–30 mA
Continuous current through $V_{CC}$ , $I_{CC}$	140 mA
Continuous current through GND	400 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package	69°C/W
M package	58°C/W
SM package	70°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.



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**recommended operating conditions (see Note 2)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–15	mA
I <sub>OL</sub>	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V <sub>IK</sub>	I <sub>I</sub> = –18 mA	4.75 V		–1.2		–1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = –15 mA	4.75 V	2.4		2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 48 mA	4.75 V		0.55		0.55	V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.25 V		±0.1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.25 V		±0.5		±10	μA
I <sub>OS</sub> <sup>†</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = 0	5.25 V	–60		–60		mA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.25 V		8		80	μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.25 V		1.6		1.6	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			15		15	pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)**

		MIN	MAX	UNIT
t <sub>w</sub>	Pulse duration LE high	6		ns
t <sub>su</sub>	Setup time Data before LE↓	2		ns
t <sub>h</sub>	Hold time Data after LE↓	1.5		ns

**switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C	MIN	MAX	UNIT
			TYP			
t <sub>pd</sub>	D	Q	5	1.5	8	ns
	LE	Any Q	9	2	13	
t <sub>en</sub>	$\overline{\text{OE}}$	Any Q	7	1.5	12	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Any Q	6	1.5	7.5	ns



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## BiCMOS OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		0.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

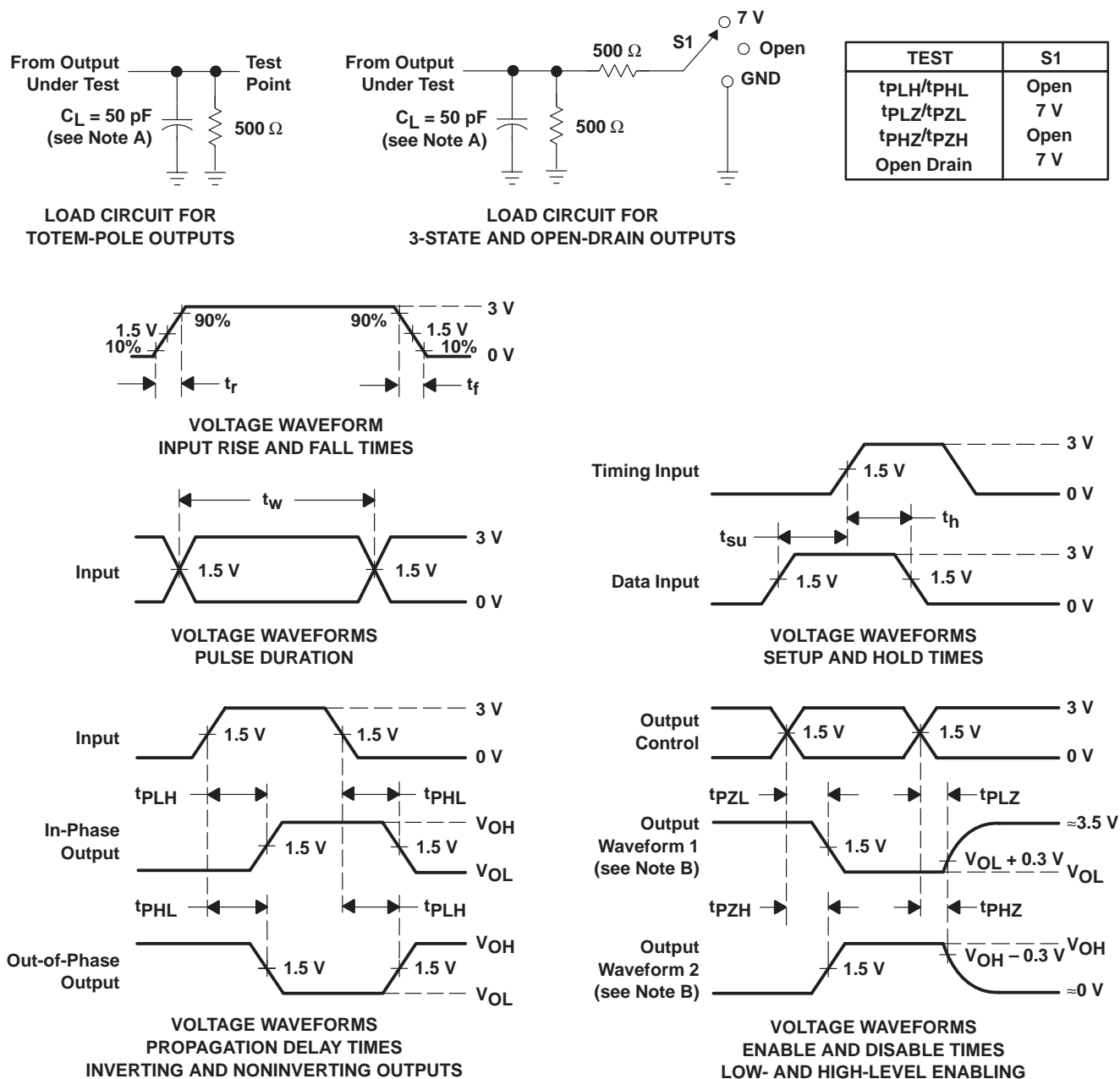
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	33	pF



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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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