DATA SHEET

74AHC1G66; 74AHCT1G66
Bilateral switch

Product specification
Supersedes data of 2002 Feb 15

2002 Jun 06

Philips
Semiconductors

PHILIPS

Bilateral switch 74AHC1G66; 74AHCT1G66

FEATURES

- Very low ON-resistance:
  - 26 Ω (typical) at V_{CC} = 3.0 V
  - 16 Ω (typical) at V_{CC} = 4.5 V
  - 14 Ω (typical) at V_{CC} = 5.5 V.
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353 and SOT753 package
- Output capability: non standard
- Specified from –40 to +125 °C.

DESCRIPTION

The 74AHC1G/AHCT1G66 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G66 provides an analog switch. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC1G	AHCT1G	
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	3	3	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	5	5	ns
C_I	input capacitance		2	2	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 10 MHz; notes 1 and 2	13	15	pF
C_S	switch capacitance		4	4	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT E	SWITCH
L	OFF
H	ON

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G66GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	AL
74AHCT1G66GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	CL
74AHC1G66GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	A66
74AHCT1G66GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	C66

PINNING

PIN	SYMBOL	DESCRIPTION
1	Y	independent input/output
2	Z	independent output/input
3	GND	ground (0 V)
4	E	enable input (active HIGH)
5	V_{CC}	supply voltage

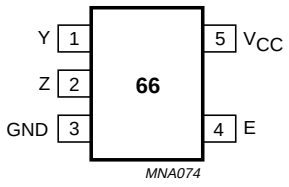


Fig.1 Pin configuration.

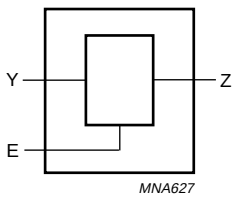


Fig.2 Logic symbol.

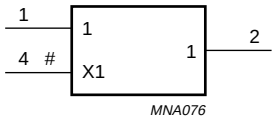


Fig.3 IEC logic symbol.

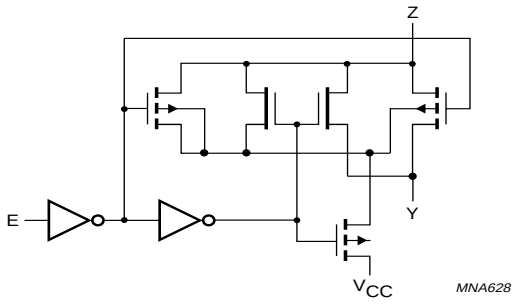


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC1G66			74AHCT1G66			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_S	switch voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5.0 ±0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	–20	mA
I_{SK}	switch diode current	$V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V	–	±20	mA
I_S	switch source or sink current	$-0.5\ V < V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C	–	250	mW

Note

1. To avoid drawing V_{CC} current out of pin Z, when switch current flows into pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no V_{CC} current will flow out of pin Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed V_{CC} or GND.

DC CHARACTERISTICS

Type 74AHC1G66

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	V
			5.5	3.85	–	–	3.85	–	3.85	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	V
			5.5	–	–	1.65	–	1.65	–	1.65	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_S	analog switch current, OFF-state	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - GND$; see Fig.5	5.5	–	–	0.1	–	1.0	–	4.0	µA
	analog switch current, ON-state	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - GND$; see Fig.6	5.5	–	–	0.1	–	1.0	–	4.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND	5.5	–	–	1.0	–	10	–	40	µA
C_I	input capacitance of enable input (E)			–	2	10	–	10	–	10	pF
C_S	maximum switch capacitance	independent I/O		–	4	10	–	10	–	10	pF

Type 74AHCT1G66

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_S	analog switch current, OFF-state	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - GND$; see Fig.5	5.5	–	–	0.1	–	1.0	–	4.0	µA
	analog switch current, ON-state	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - GND$; see Fig.6	5.5	–	–	0.1	–	1.0	–	4.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND	5.5	–	–	1.0	–	10	–	40	µA
ΔI_{CC}	additional quiescent supply current	V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0	5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance of enable input (E)			–	2	10	–	10	–	10	pF
C_S	maximum switch capacitance	independent I/O		–	4	10	–	10	–	10	pF

Type 74AHC1G66 and 74AHCT1G66

For 74AHC1G66: V_{CC} = 2.0, 3.0, 4.5 and 5.5 V; or 74AHCT1G66: V_{CC} = 4.5 and 5.5 V.

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} (°C)							UNIT
			25			−40 to +85		−40 to +125		
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 2.0 V; I_S = 1 mA; V_I = V_{IH} or V_{IL}; see Figs 7 and 8										
R_{ON}	ON-resistance (peak)	V_{is} = V_{CC} to GND	–	148[1]	–	–	–	–	–	Ω
	ON-resistance (rail)	V_{is} = GND	–	30	–	–	–	–	–	Ω
		V_{is} = V_{CC}	–	28	–	–	–	–	–	Ω
V_{CC} = 3.0 to 3.6 V; I_S = 10 mA; V_I = V_{IH} or V_{IL}; see Figs 7 and 8										
R_{ON}	ON-resistance (peak)	V_{is} = V_{CC} to GND	–	28	50	–	70	–	110	Ω
	ON-resistance (rail)	V_{is} = GND	–	20	50	–	65	–	90	Ω
		V_{is} = V_{CC}	–	18	50	–	65	–	90	Ω
V_{CC} = 4.5 to 5.5 V; I_S = 10 mA; V_I = V_{IH} or V_{IL}; see Figs 7 and 8										
R_{ON}	ON-resistance (peak)	V_{is} = V_{CC} to GND	–	15	30	–	40	–	60	Ω
	ON-resistance (rail)	V_{is} = GND	–	15	22	–	26	–	40	Ω
		V_{is} = V_{CC}	–	13	22	–	26	–	40	Ω

Note

1. At supply voltage approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices are used to transmit digital signals only, when using this supply voltage.

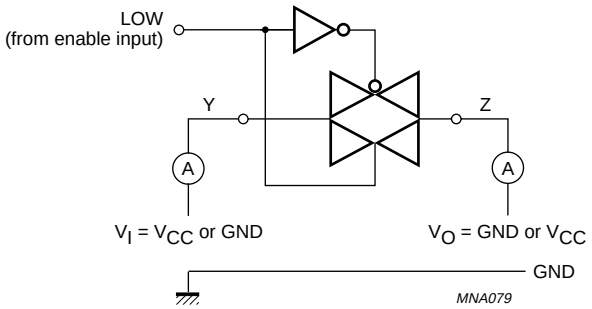


Fig.5 Test circuit for measuring OFF-state current.

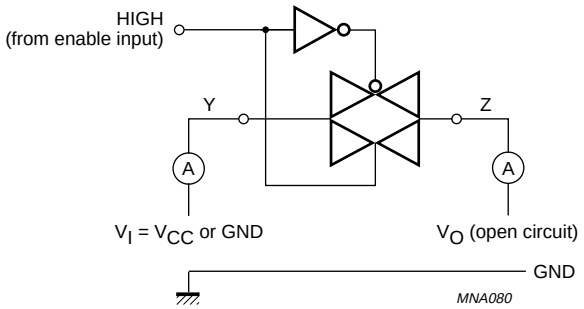


Fig.6 Test circuit for measuring ON-state current.

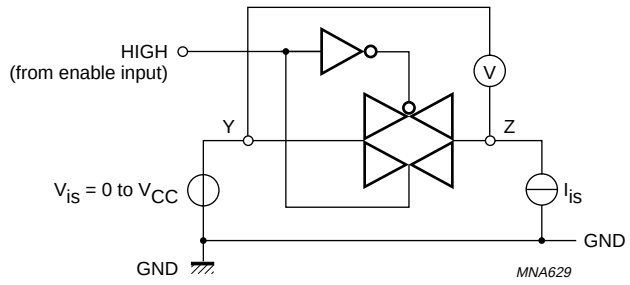


Fig.7 Test circuit for measuring ON-resistance (R_{ON}).

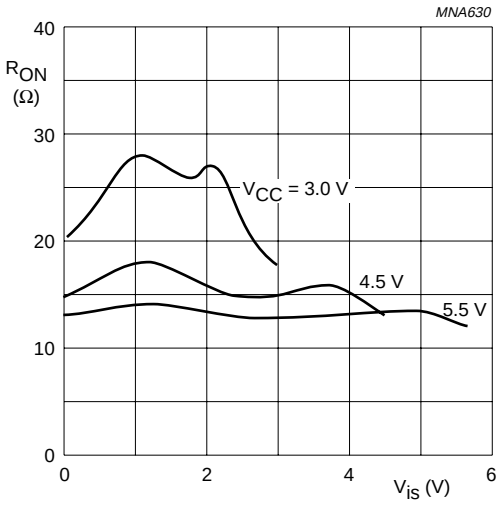


Fig.8 Typical ON-resistance as a function of input voltage.

AC CHARACTERISTICS

Type 74AHC1G66

GND = 0 V; $t_r = t_f \leq 3$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L (pF)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 2.0 V; R_L = 1 kΩ; note 1											
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	see Figs 13 and 16	50	–	2.2	5.0	–	6.0	–	7.0	ns
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	see Figs 14 and 16	15	–	7.0	25.0	–	33.0	–	40.0	ns
			50	–	11.0	35.0	–	46.0	–	57.0	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	see Figs 14 and 16	15	–	9.0	25.0	–	33.0	–	40.0	ns
			50	–	13.0	35.0	–	46.0	–	57.0	ns
V_{CC} = 3.0 to 3.6 V; R_L = 1 kΩ; note 1											
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	see Figs 13 and 16	50	–	1.0	2.0	–	3.0	–	4.0	ns
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	see Figs 14 and 16	15	–	4.0	11.0	–	14.0	–	18.0	ns
			50	–	5.8	15.0	–	20.0	–	25.0	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	see Figs 14 and 16	15	–	6.0	11.0	–	14.0	–	18.0	ns
			50	–	8.4	15.0	–	20.0	–	25.0	ns
V_{CC} = 4.5 to 5.5 V; R_L = 1 kΩ; note 1											
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	see Figs 13 and 16	50	–	0.6	1.0	–	2.0	–	3.0	ns
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	see Figs 14 and 16	15	–	3.0	8.0	–	10.0	–	13.0	ns
			50	–	4.4	11.0	–	13.0	–	17.0	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	see Figs 14 and 16	15	–	5.0	8.0	–	10.0	–	13.0	ns
			50	–	6.1	11.0	–	13.0	–	17.0	ns

Note

1. Typical values are measured at V_{CC} = 2.0 V; V_{CC} = 3.3 V or V_{CC} = 5.0 V and T_{amb} = 25 °C.

74AHCT1G66

GND = 0 V; $t_r = t_f \leq 3$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L (pF)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; R_L = 1 kΩ; note 1											
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	see Figs 13 and 16	50	–	0.7	1.0	–	2.0	–	3.0	ns
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	see Figs 14 and 16	15	–	3.0	7.0	–	10.0	–	13.0	ns
			50	–	4.7	10.0	–	13.0	–	17.0	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	see Figs 14 and 16	15	–	5.0	8.0	–	10.0	–	13.0	ns
			50	–	6.5	11.0	–	13.0	–	17.0	ns

Note

1. All typical values are measured at V_{CC} = 5 V.

TYPE 74AHC1G66 AND 74AHCT1G66

Recommended conditions and typical values. GND = 0 V; $t_r = t_f$ = 3 ns. V_{is} is the input voltage at pins Y or Z, whichever is assigned as an input. V_{os} is the output voltage at pin Y or Z, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{is(p-p)}$ (V)	V_{CC} (V)	TYPICAL	UNIT
	sine-wave distortion at f_{in} = 1 kHz	R_L = 10 kΩ; C_L = 50 pF; see Fig.9	2.5	3.0 to 3.6	0.025	%
			4.0	4.5 to 5.5	0.015	%
	sine-wave distortion at f_{in} = 10 kHz	R_L = 10 kΩ; C_L = 50 pF; see Fig.9	2.5	3.0 to 3.6	0.025	%
			4.0	4.5 to 5.5	0.015	%
	switch OFF signal feed-through	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz; see Fig.10	note 1	3.0 to 3.6	–50	dB
				4.5 to 5.5	–50	dB
f_{max}	minimum frequency response (–3 dB)	R_L = 50 Ω; C_L = 10 pF; see Figs 11 and 12	note 2	3.0 to 3.6	230	MHz
				4.5 to 5.5	280	MHz

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

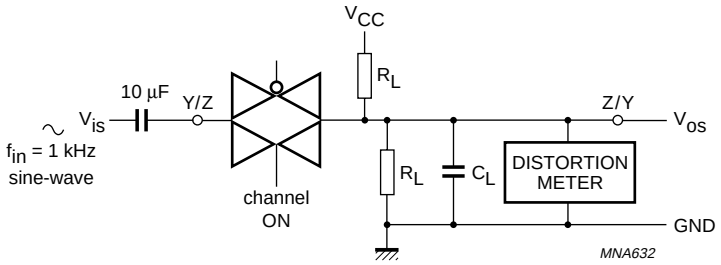


Fig.9 Test circuit for measuring sine-wave distortion.

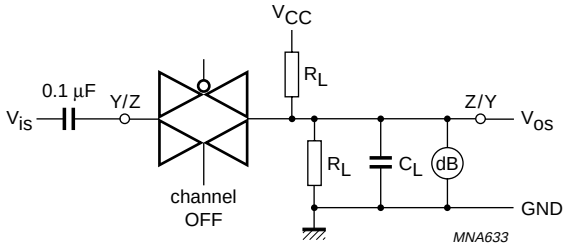
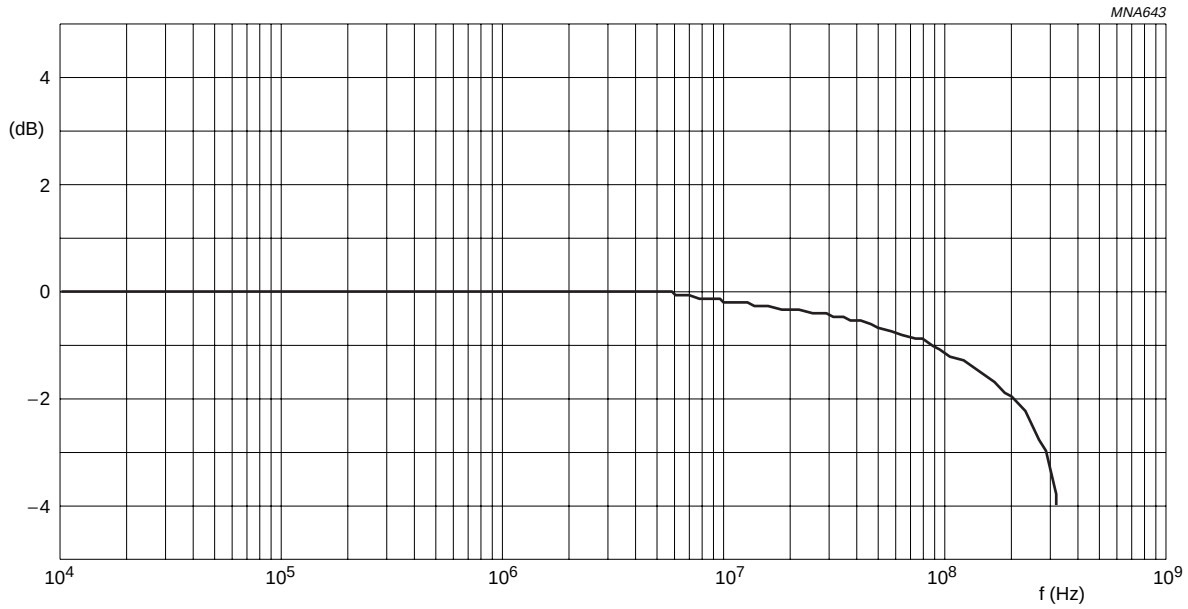
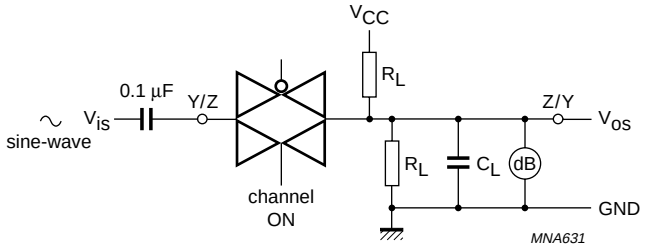


Fig.10 Test circuit for measuring switch OFF signal feed-through.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

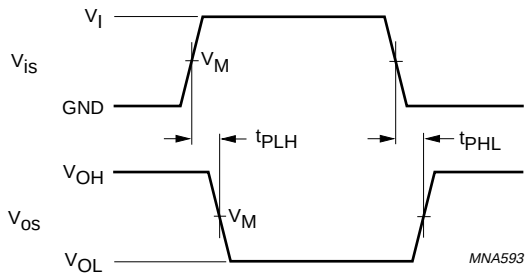
Fig.11 Typical frequency response.



Adjust input voltage to obtain 0 dBm at V_{os} when f = 1 MHz.
After set-up, the frequency is increased to obtain a reading of −3 dB at V_{os}.

Fig.12 Test circuit for measuring minimum frequency response.

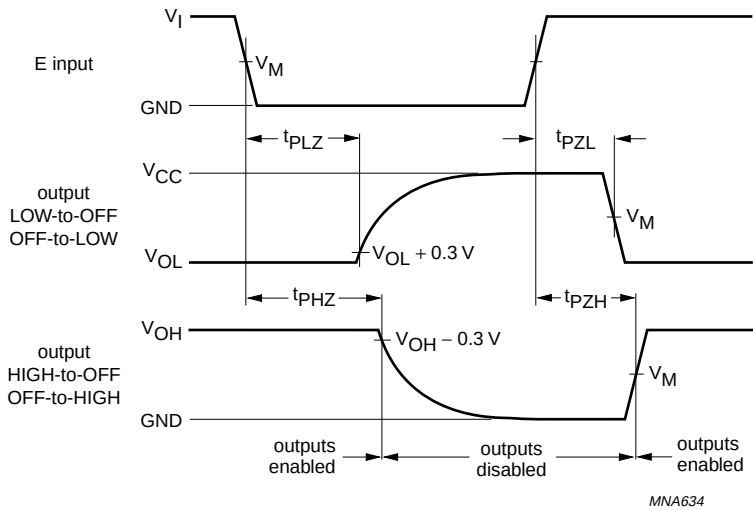
AC WAVEFORMS



V_I INPUT REQUIREMENTS	V_M INPUT
GND to V_{CC}	50% V_{CC}

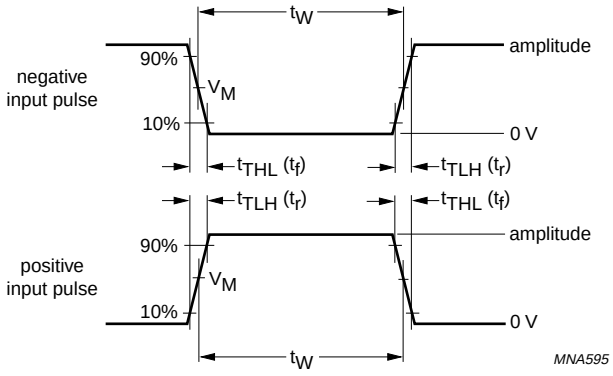
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.13 The input (V_{is}) to output (V_{os}) propagation delays.



TYPE	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC1G	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT1G	GND to 3.0 V	1.5 V	1.5 V

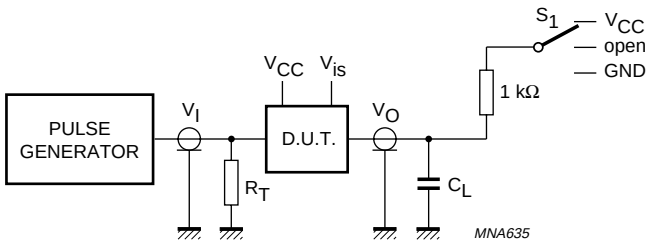
Fig.14 The turn-on and turn-off times.



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT
AHC1G	GND to V_{CC}	50% V_{CC}
AHCT1G	GND to 3.0 V	1.5 V

$t_r = t_f$ = 3 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.15 Input pulse definitions.



TEST	S_1	V_{is}
t_{PLH}/t_{PHL}	open	pulse
t_{PLZ}/t_{PZL}	V_{CC}	GND
t_{PHZ}/t_{PZH}	GND	V_{CC}

Definitions for test circuit:

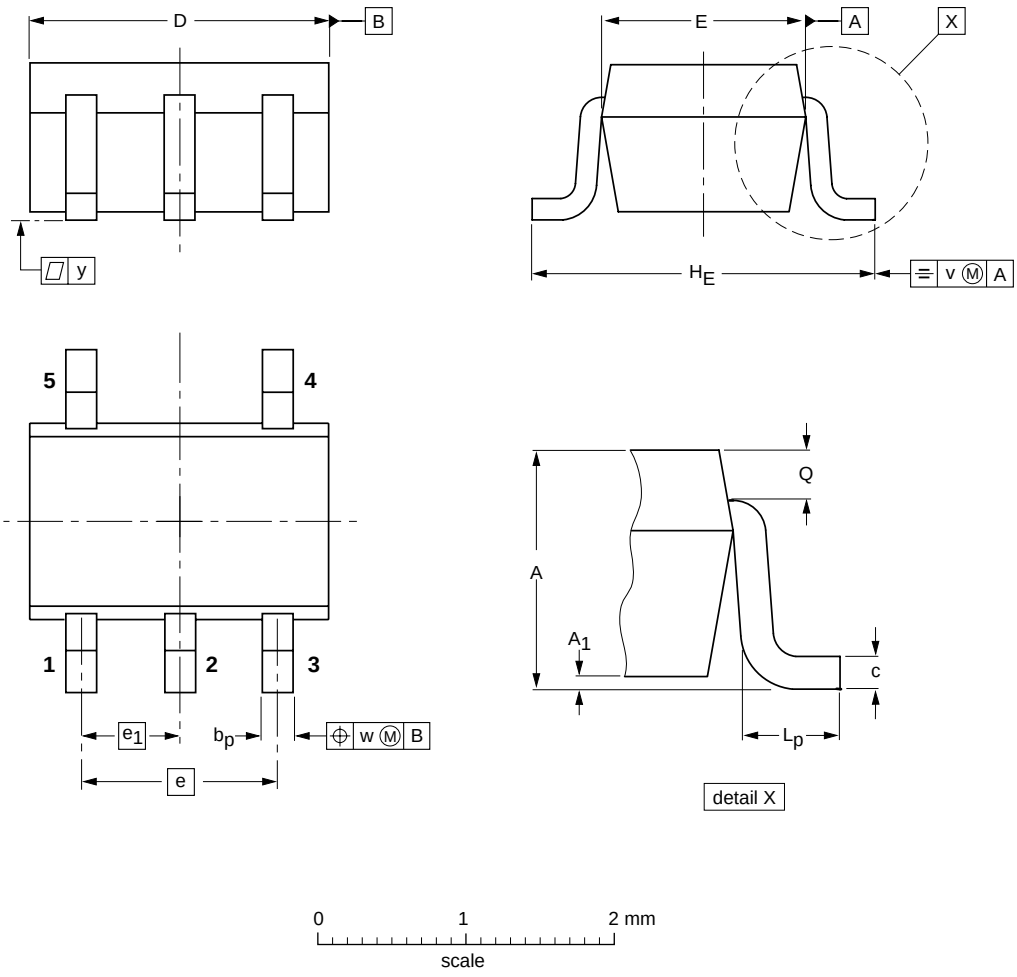
C_L = load capacitance including jig and probe capacitance (see “AC characteristics” for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.16 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads **SOT353**

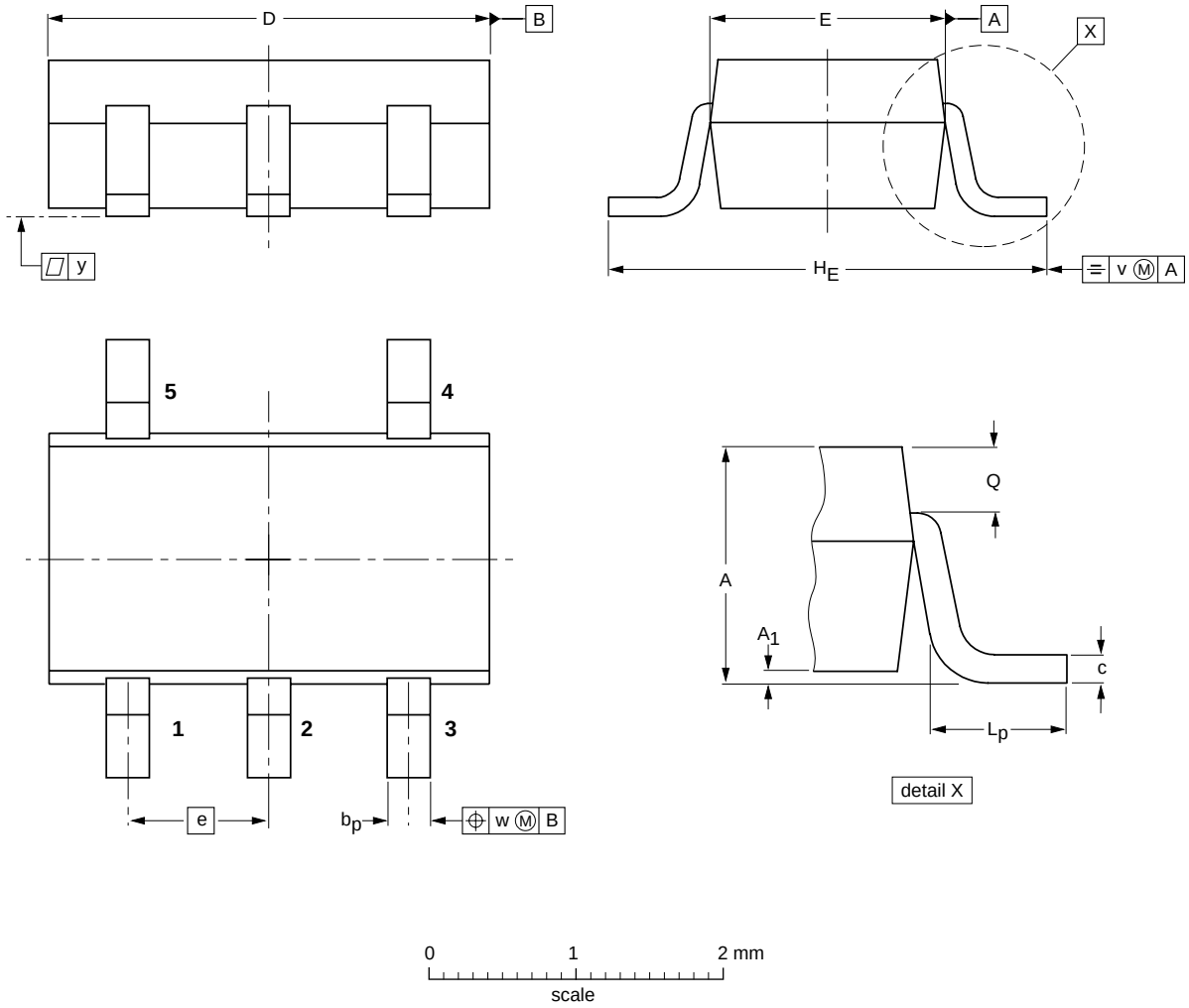


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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Notes

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