CMOS 16-bit MICROCONTROLLERS

TMP96C041BF

1. OUTLINE AND DEVICE CHARACTERISTICS

TMP96C041BF is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C041B has RAMless for TMP96C141BF. Otherwise, the devices function in the same way.

TMP96C041BF is housed in an 80-pin flat package.

Device characteristics are as follows:

(1) Original 16-bit CPU
- TLCS-90 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer/arithmetic instructions
- High-speed micro DMA : 4 channels (1.6 μs/2 bytes @ 20 MHz)

(2) Minimum instruction execution time : 200 ns @ 20 MHz

(3) Internal RAM : None
Internal ROM : None

(4) External memory expansion
- Can be expanded up to16M bytes (for both programs and data).
- Can mix 8- and 16-bit external data buses.

(5) 8-bit timers : 2 channels

(6) 8-bit PWM timers : 2 channels

(7) 16-bit timers : 2 channels

(8) Pattern generators : 4 bits, 2 channels

(9) Serial interface : 2 channels

(10) 10-bit A/D converter : 4 channels

(11) Watchdog timer

(12) Chip select/wait controller : 3 blocks

(13) Interrupt functions
- 3 CPU interrupts····· SWI instruction, priviledged violation, and Illegal instruction
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports
47 pins

(15) Standby function : 3 halt modes (RUN, IDLE, STOP)

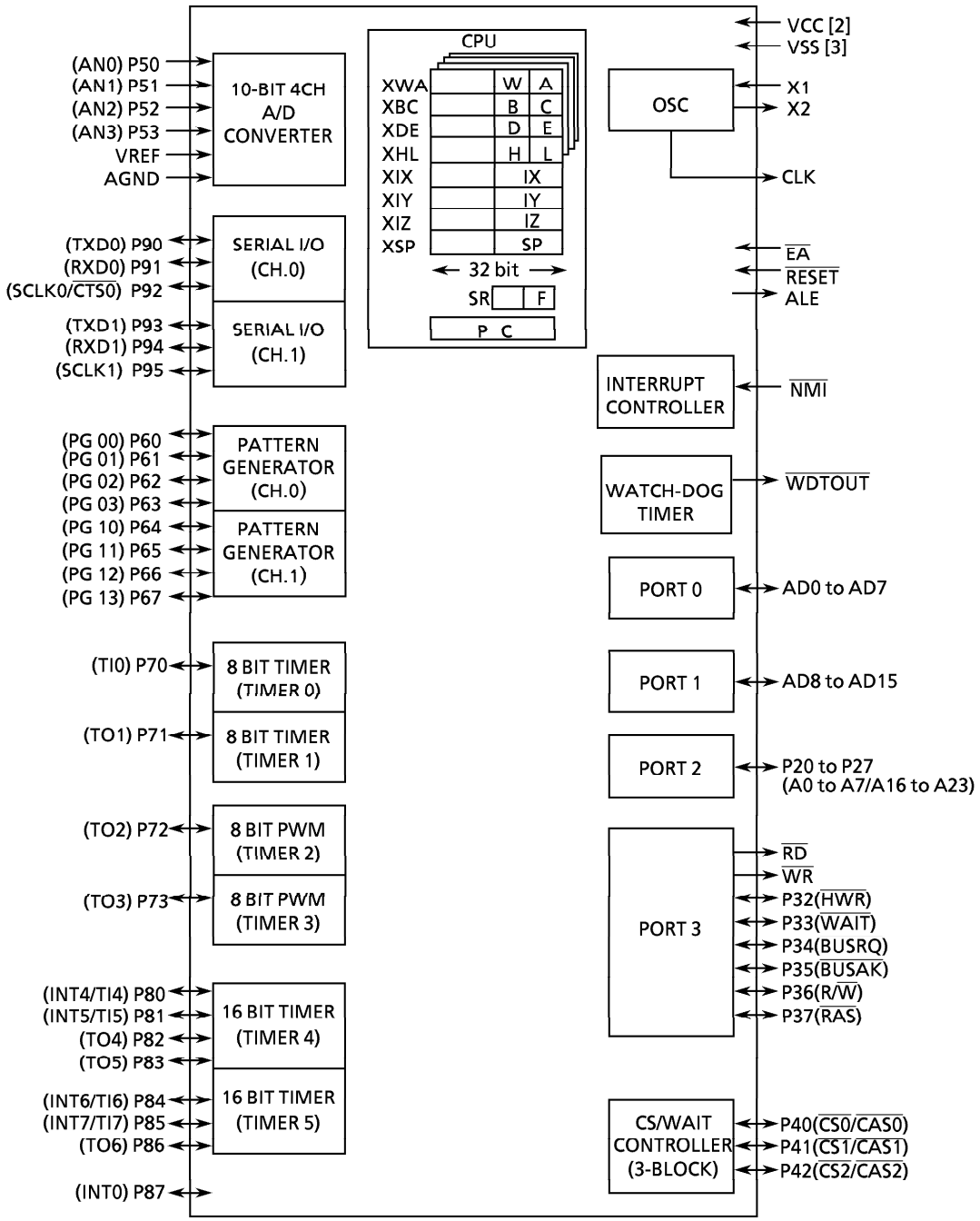


Figure1 TMP96C041B Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for TMP96C041B, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96C041BF.

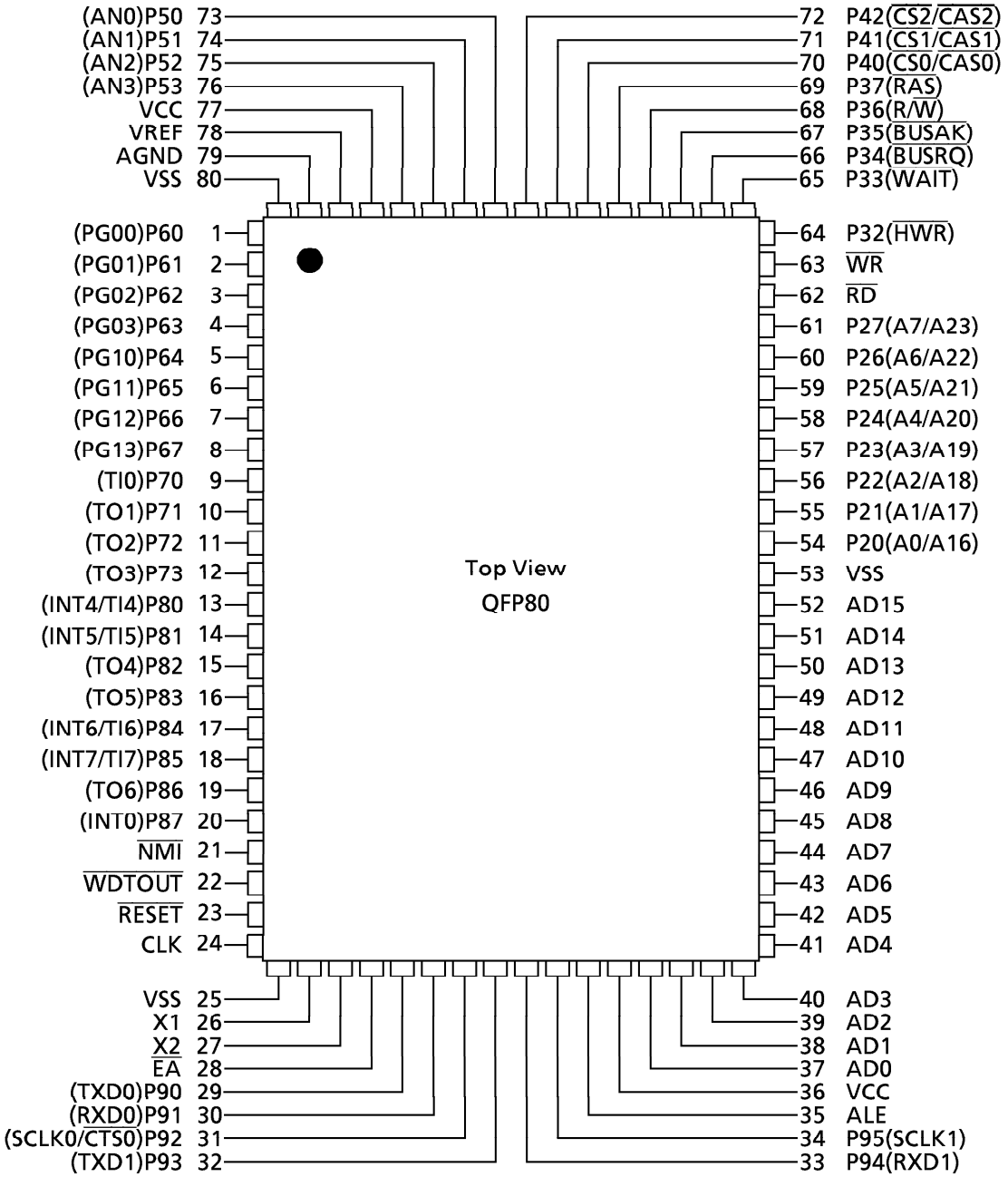


Figure 2.1 Pin Assignment (80-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
AD0 to AD7	8	Tri-state	Address/data (lower): 0 - 7 for address/data bus
AD8 to AD15	8	Tri-state	Address data (upper): 8 - 15 for address/data bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 - 7 for address bus Address: 16 - 23 for address bus
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory
$\overline{WR}$	1	Output	Write: Strobe signal for writing data on pins AD0 - 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 - 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 - 15, A0 - 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0-15, A0-23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) (Note1) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50~P53 AN0~AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60~P63 PG00~PG03	4	I/O Output	Ports 60 - 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 - 03
P64~P67 PG10~PG13	4	I/O Output	Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 - 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Note 1 : Case of the settable $\overline{CS2}$ or $\overline{CAS2}$; when TMP96C041BF is bus release, this pin is not added the internal pull-down resistor but is added the internal pull-up resistor.

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs「X1 ÷ 4」clock. Pulled-up during reset.
$\overline{EA}$	1	Input	External access: 0 should be inputted with TMP96C041B.
ALE	1	Output	Address latch enable
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
VCC	2		Power supply pin (+ 5V)
VSS	3		GND pin (0V)

Note : Pull-up/pull-down resistor can be released from the pin by software (except the $\overline{RESET}$ pin).

3. OPERATION

This section describes the functions and basic operations of TMP96C041B device.

The function of CPU and internal I/O devices are the same function as TMP96C141B. Check the 「7. Care Points and Restriction of TMP96C141B 」because of the Care described.

Regarding the functions of TMP96C041B (not described), see the part of TMP96C141B.

TMP96C141B/TMP96C041B have much the same function but they are different from following points.

Parameter	TMP96C141B	TMP96C041B
Interrnal RAM	1K byte	not exist
Mapping area of CS1 defult setting (B1C1/0: 00)	480H~7FFFH	80H~7FFFH

3.1 CPU

TMP96C041B device has a built-in high-performance 16-bit CPU (900-CPU). (For CPU operation, see TLCS-900 CPU in the previous section.)

3.2 Memory Map

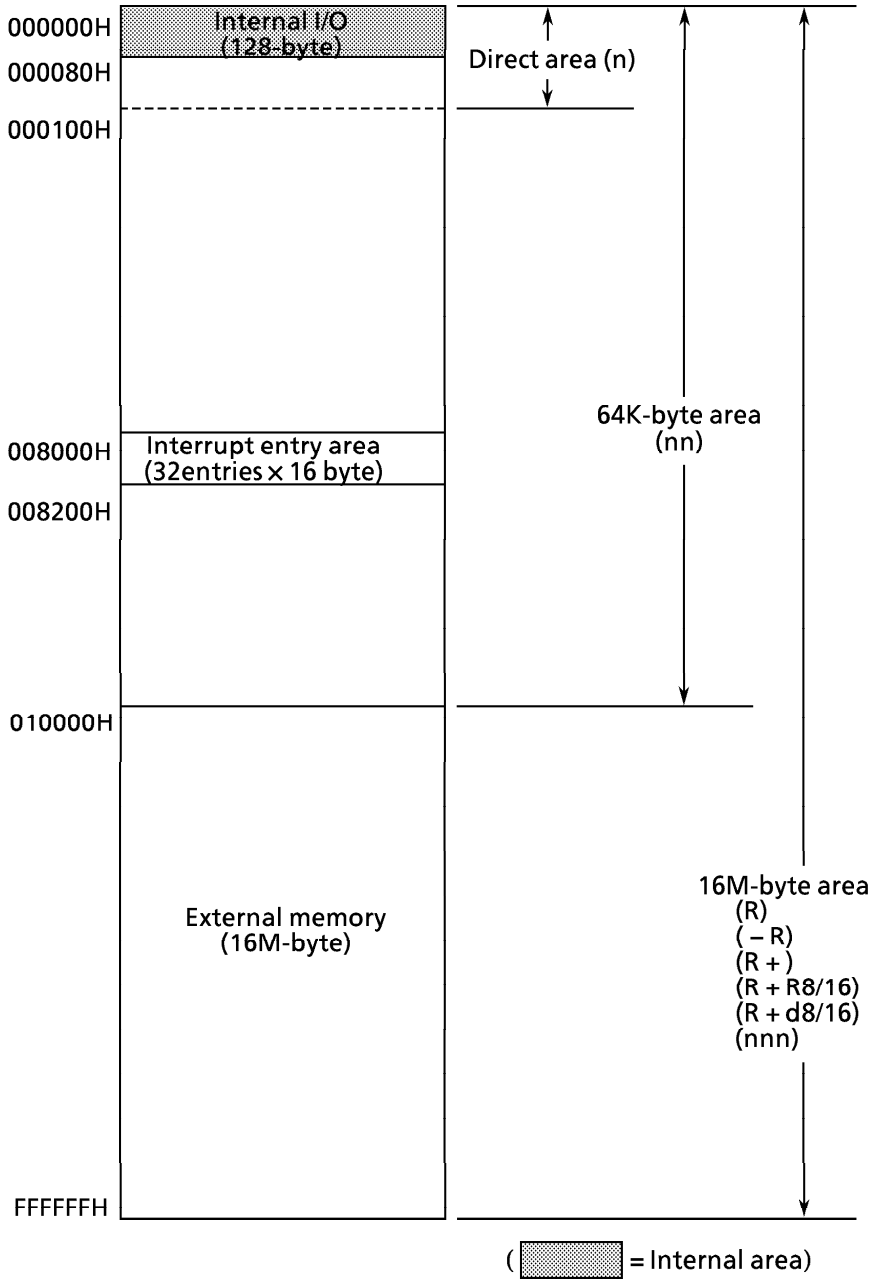
TMP96C041B has two register modes. One is a minimum mode; in this mode, the area of program memory is 64K bytes maximum. The other is a maximum mode; in this mode, the area of program memory is 16M bytes maximum.

Both minimum and maximum modes are the data memory area of 16M bytes maximum.

That is, the program memory can locate 0H~FFFFH in minimum mode and can locate 0H ~ FFFFFFH in maximum mode.

Memory Map

Figure 3.2 (1) is a memory map of the TMP96C041B.



Note : The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.2 (1) Memory map

(2) $\overline{CS1}$ area (Chip select / wait controller)

TMP96C041B is expanded the part of address area for $\overline{CS1}$ (only B1C1.0 = "00"). Show the address area of $\overline{CS1}$ in Fig 3.2 (2).

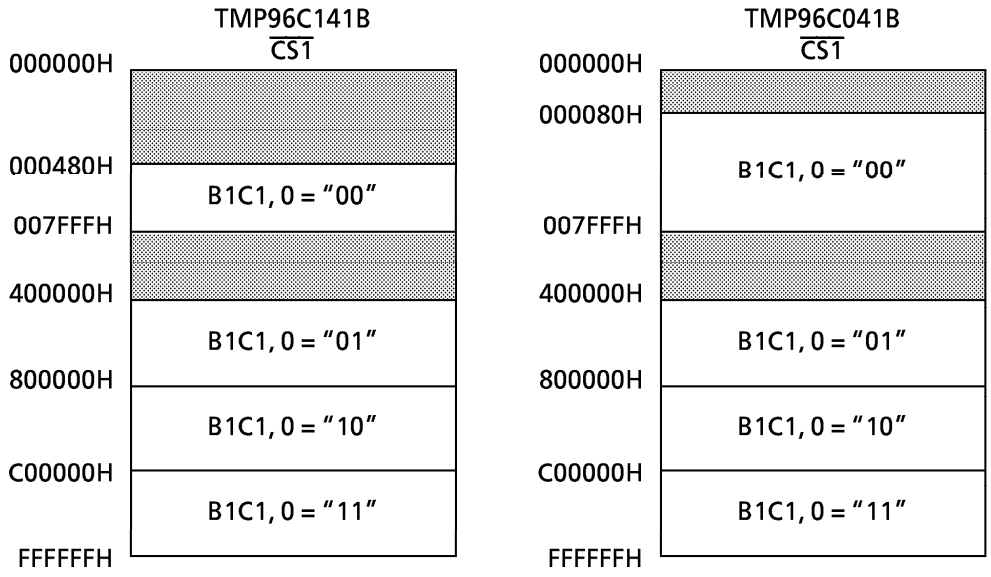


Fig.3.2 (2) $\overline{CS1}$ address area

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum (TMP96C041BF)

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5~6.5	V
V IN	Input Voltage	– 0.5~Vcc + 0.5	V
Σ IOL	Output Current (total)	100	mA
Σ IOH	Output Current (total)	– 100	mA
P D	Power Dissipation (Ta = 85 ℃)	500	mW
T SOLDER	Soldering Temperature (10 s)	260	℃
T STG	Storage Temperature	– 65~150	℃
T OPR	Operating Temperature	– 40~85	℃

4.2 DC Characteristics (TMP96C041BF)

Vcc = 5V ± 10%, TA = – 40~85 ℃ (4~16 MHz) TA = – 20~70 ℃ (4~20 MHz)

(Typical values are for Ta = 25 ℃ and Vcc = 5 V)

Symbol	Parameter	Min	Max	Unit	Test Condition
V IL V IL1 V IL2 V IL3 V IL4	Input Low Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET,NMI,INT0(P87) EA X1	– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V	
V IH V IH1 V IH2 V IH3 V IH4	Input High Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET, NMI, INT0 (P87) EA X1	2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V	
V OL	Output Low Voltage		0.45	V	I OL = 1.6 mA
V OH V OH1 V OH2	Output High Voltage	2.4 0.75 Vcc 0.9 Vcc		V V V	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA
I DAR	Darlington Drive Current (8 Output Pins max.)	– 1.0	– 3.5	mA	V EXT = 1.5 V R EXT = 1.1 kΩ
I LI I LO	Input Leakage Current Output Leakage Current	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2
I cc	Operating Current (RUN) IDLE STOP (Ta = – 40~85 ℃) STOP (Ta = 0~50 ℃)	21 (Typ) 1.7 (Typ) 0.2 (Typ)	50 10 50 10	mA mA μA μA	t osc = 20 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2
V STOP	Power Down Voltage (@ STOP, RAM Back up)	2.0	6.0	V	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc
R RST	RESET Pull Up Resistor	50	150	kΩ	
C IO	Pin Capacitance		10	pF	tosc = 1 MHz
V TH	Schmitt Width RESET, NMI, INT0 (P87)	0.4	1.0 (Typ)	V	
R KL	Programmable Pull Down Resistor	10	80	kΩ	
R KH	Programmable Pull Up Resistor	50	150	kΩ	

Note : I-DAR is guaranteed for a total of up to 8 ports.

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum (TMP96C041BF)

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5~6.5	V
V IN	Input Voltage	– 0.5~Vcc + 0.5	V
Σ IOL	Output Current (total)	100	mA
Σ IOH	Output Current (total)	– 100	mA
P D	Power Dissipation (Ta = 85 ℃)	500	mW
T SOLDER	Soldering Temperature (10 s)	260	℃
T STG	Storage Temperature	– 65~150	℃
T OPR	Operating Temperature	– 40~85	℃

4.2 DC Characteristics (TMP96C041BF)

Vcc = 5V ± 10%, TA = – 40~85 ℃ (4~16 MHz) TA = – 20~70 ℃ (4~20 MHz)

(Typical values are for Ta = 25 ℃ and Vcc = 5 V)

Symbol	Parameter	Min	Max	Unit	Test Condition
V IL V IL1 V IL2 V IL3 V IL4	Input Low Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET,NMI,INT0(P87) EA X1	– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V	
V IH V IH1 V IH2 V IH3 V IH4	Input High Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET, NMI, INT0 (P87) EA X1	2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V	
V OL	Output Low Voltage		0.45	V	I OL = 1.6 mA
V OH V OH1 V OH2	Output High Voltage	2.4 0.75 Vcc 0.9 Vcc		V V V	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA
I DAR	Darlington Drive Current (8 Output Pins max.)	– 1.0	– 3.5	mA	V EXT = 1.5 V R EXT = 1.1 kΩ
I LI I LO	Input Leakage Current Output Leakage Current	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2
I cc	Operating Current (RUN) IDLE STOP (Ta = – 40~85 ℃) STOP (Ta = 0~50 ℃)	21 (Typ) 1.7 (Typ) 0.2 (Typ)	50 10 50 10	mA mA μA μA	t osc = 20 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2
V STOP	Power Down Voltage (@ STOP, RAM Back up)	2.0	6.0	V	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc
R RST	RESET Pull Up Resistor	50	150	kΩ	
C IO	Pin Capacitance		10	pF	tosc = 1 MHz
V TH	Schmitt Width RESET, NMI, INT0 (P87)	0.4	1.0 (Typ)	V	
R KL	Programmable Pull Down Resistor	10	80	kΩ	
R KH	Programmable Pull Up Resistor	50	150	kΩ	

Note : I-DAR is guaranteed for a total of up to 8 ports.

4.3 AC Electrical Characteristics (TMP96C041BF)

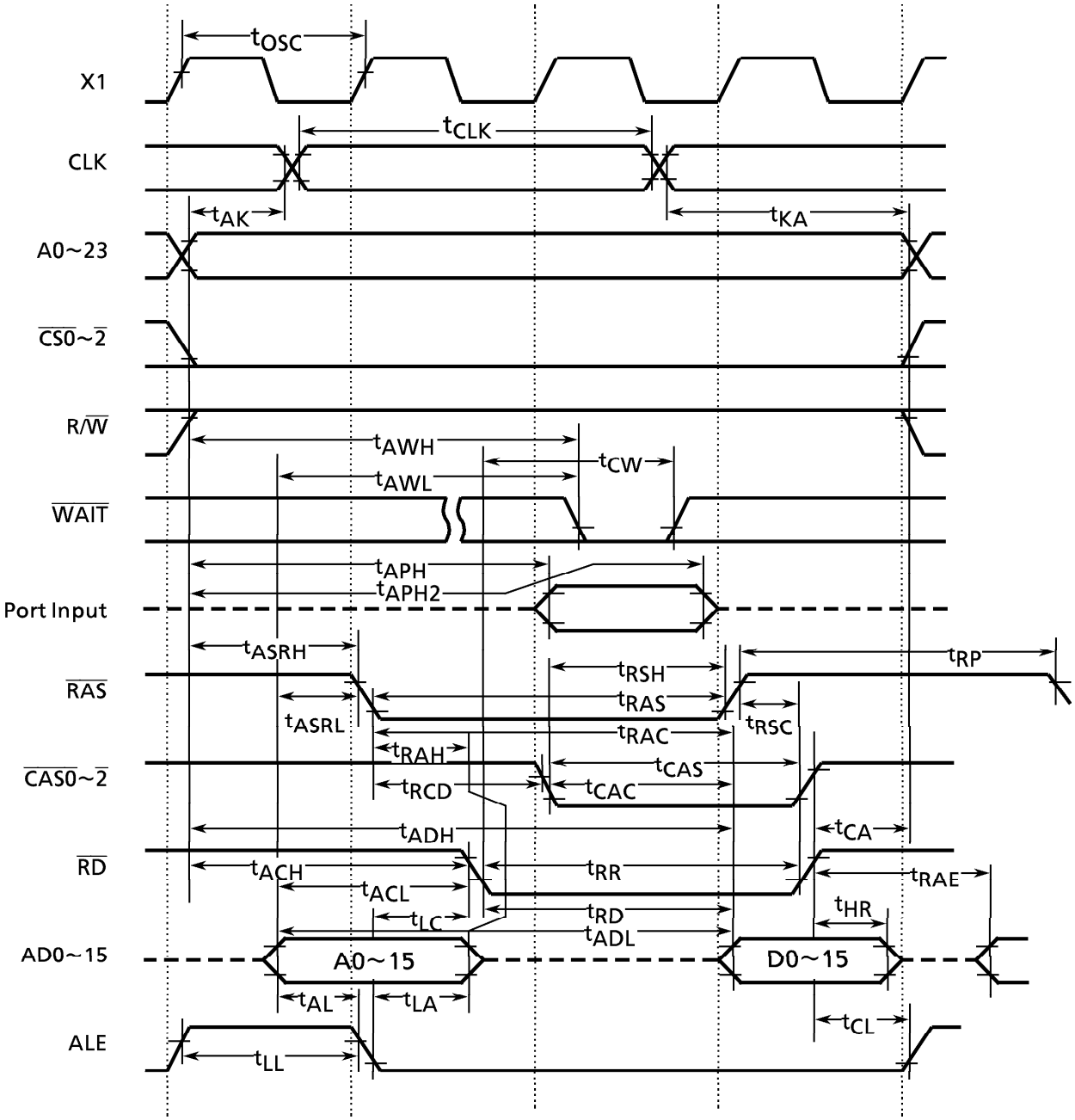
Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

No.	Symbol	Parameter	Variavle		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	250	62.5		50		ns
2	t_{CLK}	CLK width	2x − 40		85		60		ns
3	t_{AK}	A0-23 Valid→ CLK Hold	0.5x − 20		11		5		ns
4	t_{KA}	CLK Valid→ A0-23 Hold	1.5x − 70		24		5		ns
5	t_{AL}	A0-15 Valid→ ALE fall	0.5x − 15		16		10		ns
6	t_{LA}	ALE fall→ A0-15 Hold	0.5x − 15		16		10		ns
7	t_{LL}	ALE High width	x − 40		23		10		ns
8	t_{LC}	ALE fall→ $\overline{RD}/\overline{WR}$ fall	0.5x − 30		1		-5		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ rise→ ALE rise	0.5x − 20		11		5		ns
10	t_{ACL}	A0-15 Valid→ $\overline{RD}/\overline{WR}$ fall	x − 25		38		25		ns
11	t_{ACH}	A0-23 Valid→ $\overline{RD}/\overline{WR}$ fall	1.5x − 50		44		25		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ rise→ A0-23 Hold	0.5x − 20		11		5		ns
13	t_{ADL}	A0-15 Valid→ D0-15 input		3.0x − 45		143		105	ns
14	t_{ADH}	A0-23 Valid→ D0-15 input		3.5x − 65		154		110	ns
15	t_{RD}	$\overline{RD}$fall → D0-15 input		2.0x − 50		75		50	ns
16	t_{RR}	$\overline{RD}$ Low width	2.0x − 40		85		60		ns
17	t_{HR}	$\overline{RD}$rise→ D0-15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$rise→ A0-15output	x − 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low width	2.0x − 40		85		60		ns
20	t_{DW}	D0-15 Valid→ $\overline{WR}$ rise	2.0x − 50		75		50		ns
21	t_{WD}	$\overline{WR}$ rise →D0-15 Hold	0.5x − 10		21		15		ns
22	t_{AEH}	A0-23 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)		3.5x − 90		129		85	ns
23	t_{AWL}	A0-15 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)		3.0x − 80		108		70	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold (1WAIT + n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0-23 Valid→ PORT input		2.5x − 120		36		5	ns
26	t_{APH2}	A0-23 Valid→ PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ rise→ PORT Valid		200		200		200	ns
28	t_{ASRH}	A0-23 Valid→ $\overline{RAS}$ fall	1.0x − 40		23		10		ns
29	t_{ASRL}	A0-15 Valid→ $\overline{RAS}$ fall	0.5x − 15		16		10		ns
30	t_{RAC}	$\overline{RAS}$ fall→ D0-15 input		2.5x − 70		86		55	ns
31	t_{RAH}	$\overline{RAS}$ fall→ A0-15 Hold	0.5x − 15		16		10		ns
32	t_{RAS}	$\overline{RAS}$ Low width	2.0x − 40		85		60		ns
33	t_{RP}	$\overline{RAS}$ High width	2.0x − 40		85		60		ns
34	t_{RSH}	$\overline{CAS}$ fall→ $\overline{RAS}$ rise	1.0x − 35		28		15		ns
35	t_{RSC}	$\overline{RAS}$ rise→ $\overline{CAS}$ rise	0.5x − 25		6		0		ns
36	t_{RCD}	$\overline{RAS}$ fall→ $\overline{CAS}$ fall	1.0x − 40		23		10		ns
37	t_{CAC}	$\overline{CAS}$ fall→ D0-15 input		1.5x − 65		29		10	ns
38	t_{CAS}	$\overline{CAS}$ Low width	1.5x − 30		64		40		ns
39	t_{DS}	D0-15 Valid→ $\overline{CAS}$ fall	0.5x − 15		16		10		ns

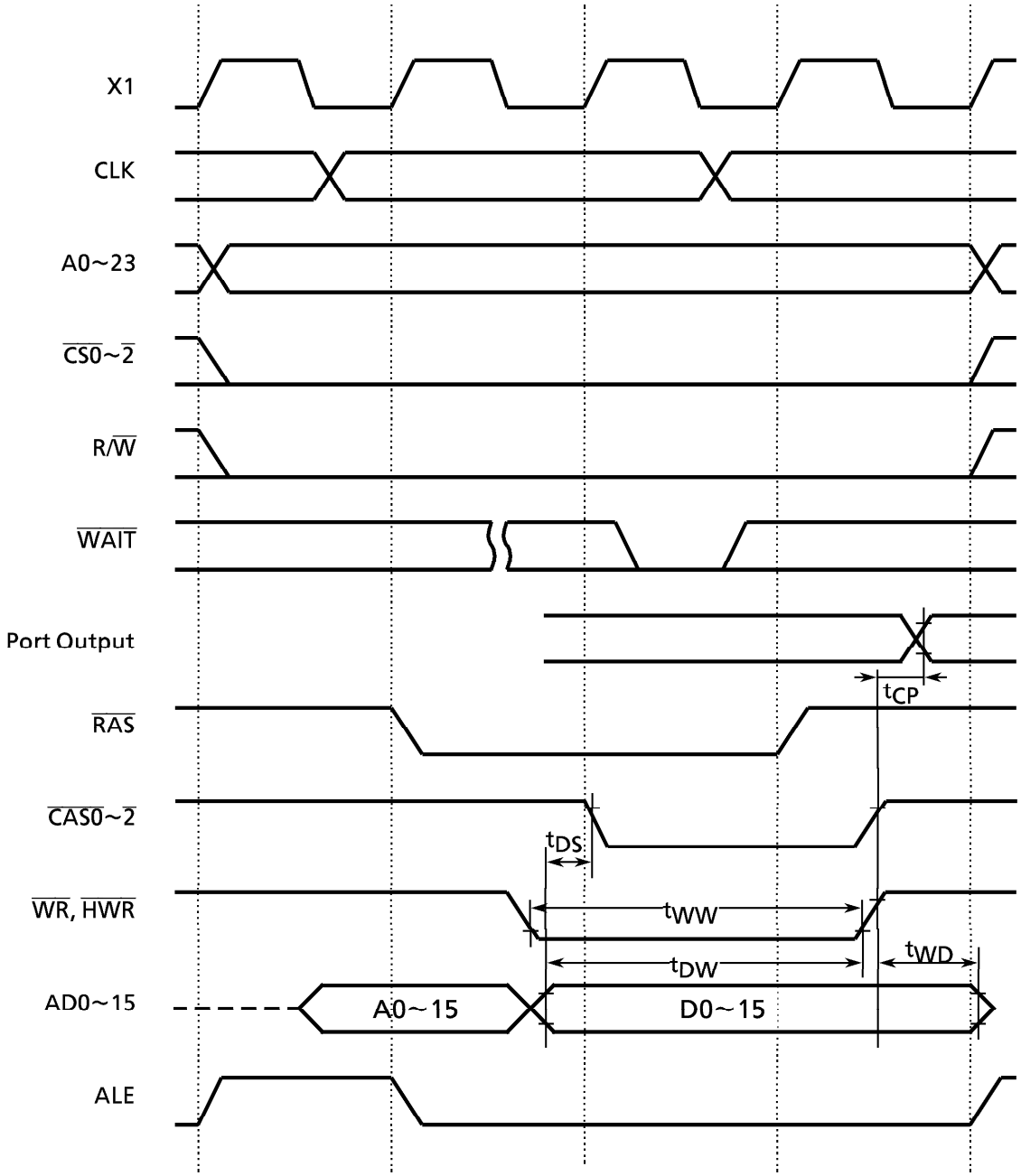
AC Measuring Conditions

- Output Level : High 2.2 V /Low 0.8 V , CL50 pF
  (However CL = 100pF for AD0~AD15, A0~A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$~$\overline{CAS2}$)
- Input Level : High 2.4 V /Low 0.45 V (AD0~AD15)
  High 0.8 Vcc /Low 0.2 Vcc (Except for AD0~AD15)

(1) Read Cycle


X1
CLK
A0~23
CS0~2
R/W
WAIT
Port Input
RAS
CAS0~2
RD
AD0~15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tASRH
tASRL
tRSH
tRAS
tRAC
tRAH
tRCD
tCAS
tCAC
tRSC
tRP
tADH
tCA
tACH
tACL
tLC
tRR
tRD
tADL
tRAE
tHR
A0~15
D0~15
tAL
tLA
tLL
tCL

(2) Write Cycle



4.4 A/D Conversion Characteristics (TMP96C041BF)

Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

Symbol	Parameter		Min	Typ	Max	Unit
V_{REF}	Analog reference voltage		Vcc − 1.5		Vcc	V
A_{GND}	Analog reference voltage		Vss		Vss	
V_{AIN}	Analog input voltage range		Vss		Vcc	
I_{REF}	Anlog current for analog reference voltage			0.5	1.5	mA
Total error (Quantize error of ± 0.5 LSB not included)	4 ≦ fc ≦ 16 MHz	Low change mode		± 1.5	± 4.0	LSB
		High change mode		± 3.0	± 6.0	
	16 < fc ≦ 20 MHz	Low change mode		± 1.5	± 4.0	
		High change mode		± 4.0	± 8.0	

4.5 Serial Channel Timing − I/O Interface Mode

(1) SCLK Input Mode

Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16X		1		0.8		μs
t_{OSS}	Output Data → Rising edge of SCLK	t_{SCY}/2 − 5X − 50		137		100		ns
t_{OHS}	SCLK rising edge→ Output Data hold	5X − 100		212		150		ns
t_{HSR}	SCLK rising edge→ Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge→ effective data input		t_{SCY} − 5X − 100		587		450	ns

(2) SCLK Output Mode

Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16X	8192X	1	512	0.8	409.6	μs
t_{OSS}	Output Data → SCLK rising edge	t_{SCY} − 2X − 150		725		550		ns
t_{OHS}	SCLK rising edge→ Output Data hold	2X − 80		45		20		ns
t_{HSR}	SCLK rising edge→ Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge→ effective data input		t_{SCY} − 2X − 150		725		550	ns

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

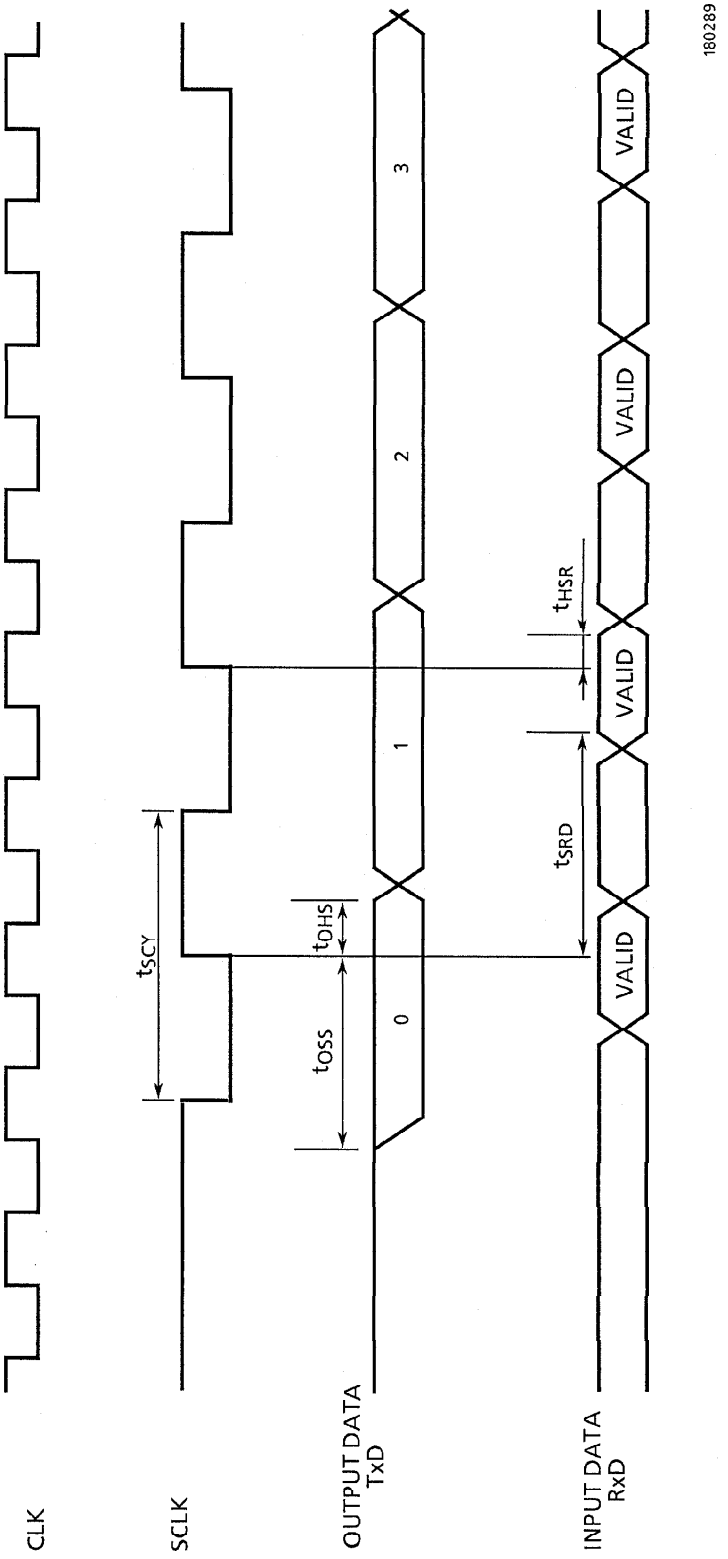
Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	8X + 100		600		500		ns
t_{VCKL}	Low level clock Pulse width	4X + 40		290		240		ns
t_{VCKH}	High level clock Pulse width	4X + 40		290		240		ns

4.7 Interrupt Operation

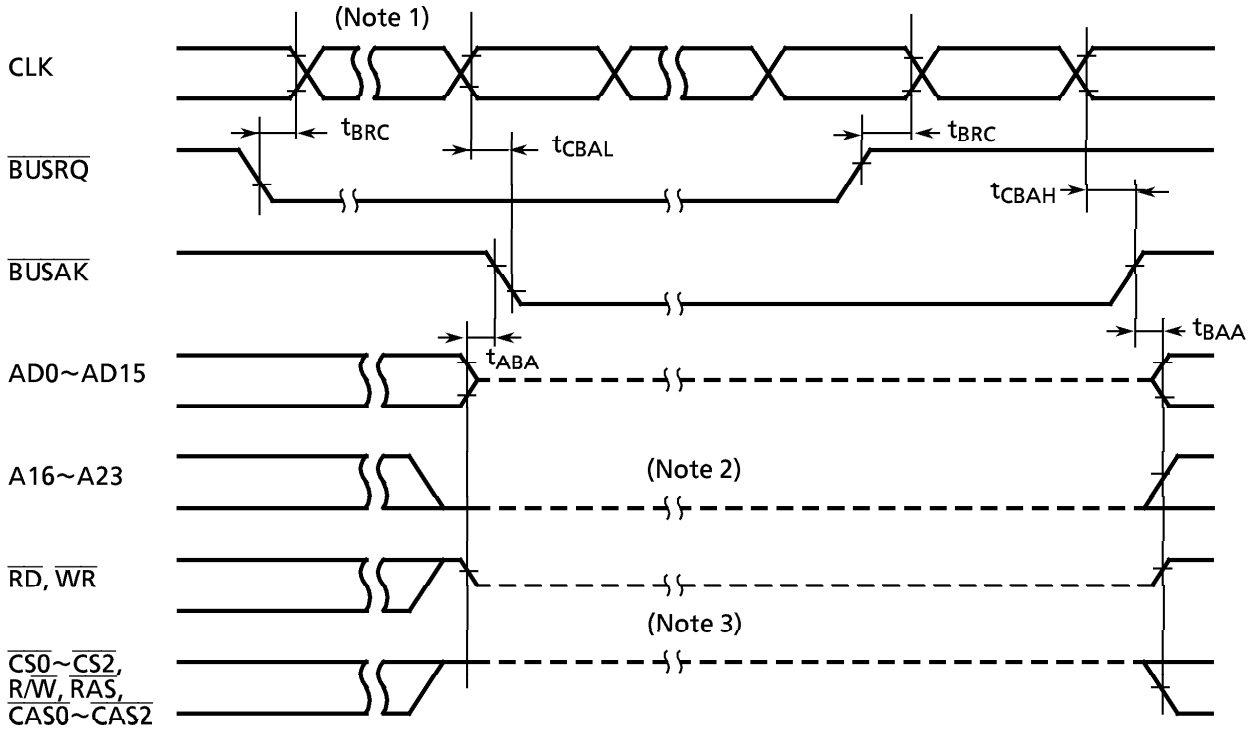
Vcc = 5 V ± 10 %, TA = − 40~85 ℃ (4~16 MHz) TA = − 20~70 ℃ (4~20 MHz)

Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level Pulse width	4X		250		200		ns
t_{INTAH}	$\overline{NMI}$, INT0 High level Pulse width	4X		250		200		ns
t_{INTBL}	INT4~INT7 Low level Pulse width	8X + 100		600		500		ns
t_{INTBH}	INT4~INT7 High level Pulse width	8X + 100		600		500		ns

4.8 Timing Chart for I/O Interface Mode



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{BUSRQ}$ set-up time for CLK	120		120		120		ns
t_{CBAL}	CLK→ $\overline{BUSAK}$ falling edge		2.0x + 120		245		220	ns
t_{CBAH}	CLK→ $\overline{BUSAK}$ rising edge		0.5x + 40		71		65	ns
t_{ABA}	Output Buffer is off to $\overline{BUSAK}$ ↓	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ ↑ to Output Buffer is on.	0	80	0	80	0	80	ns

(Note 1) : The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.
(Note 2) : The internal programmable pull-down resistor is added.
(Note 3) : The internal programmable pull-up resistor is added.
But the $\overline{CS2}$/$\overline{CAS2}$ pin does not have the internal programmable pull-up resistor. And in the condition of bus release, this pin is added the internal pull-up resistor.