IS41C16100C
IS41LV16100C

1Mx16
16Mb DRAM WITH EDO PAGE MODE

FEBRUARY 2012

FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval:
  - — Auto refresh Mode: 1,024 cycles /16 ms
  - — $\overline{\text{RAS}}$-Only, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR), and Hidden
  - — Self refresh Mode: 1,024 cycles /128 ms
- JEDEC standard pinout
- Single power supply:
  5V ± 10% (IS41C16100C)
  3.3V ± 10% (IS41LV16100C)
- Byte Write and Byte Read operation via two $\overline{\text{CAS}}$
- Industrial Temperature Range: -40°C to +85°C

DESCRIPTION

The *ISSI* IS41C16100C and IS41LV16100C are 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. These devices offer a cycle access called Extended Data Out (EDO) Page Mode. EDO Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 30 ns per 16-bit word. It is asynchronous, as it does not require a clock signal input to synchronize commands and I/O.

These features make the IS41C/41LV16100C ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications that run without a clock to synchronize with the DRAM.

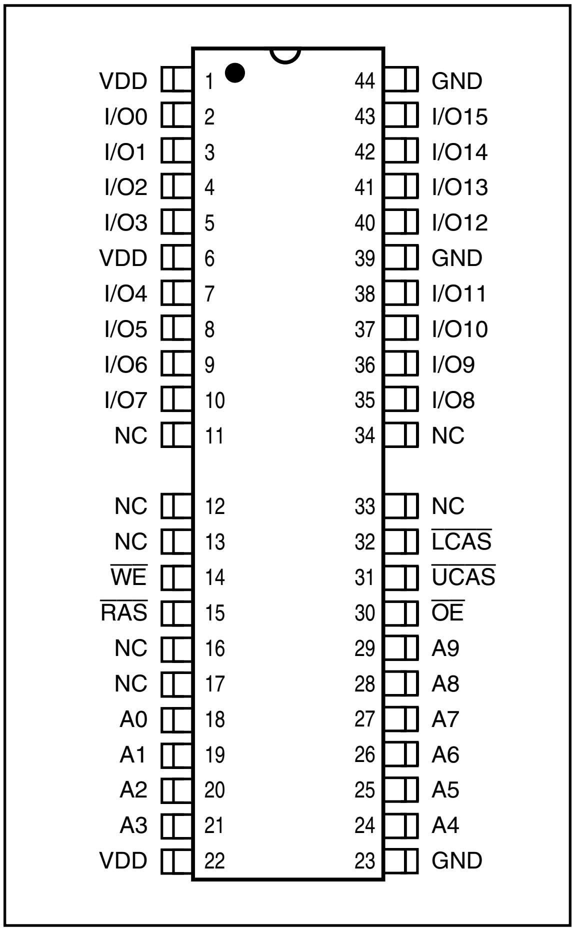
The IS41C/41LV16100C is packaged in a 42-pin 400-mil SOJ and 400-mil 50/44 pin TSOP (Type II).

KEY TIMING PARAMETERS

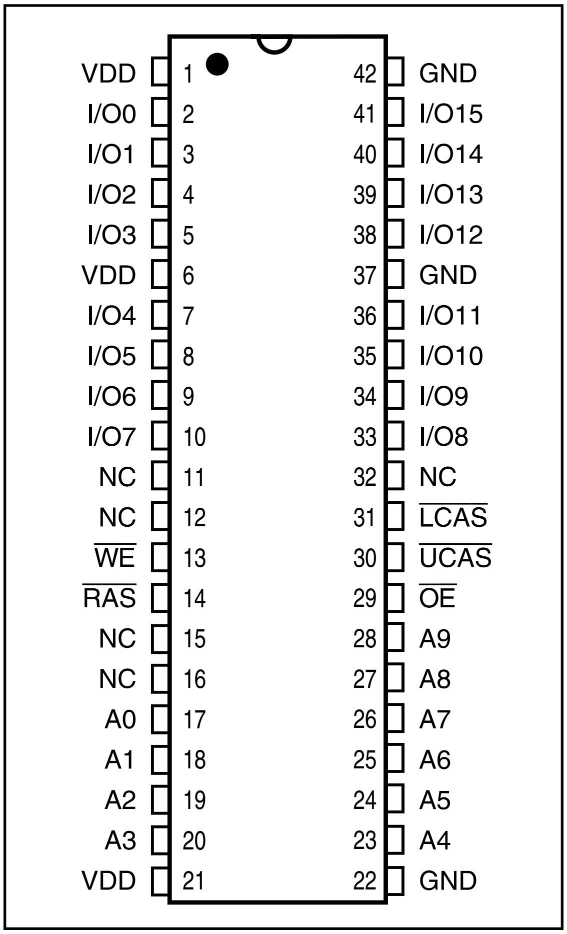
Parameter	-50	Unit
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	50	ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	14	ns
Max. Column Address Access Time (t_{AA})	25	ns
Min. EDO Page Mode Cycle Time (t_{PC})	30	ns
Min. Read/Write Cycle Time (t_{RC})	85	ns

PIN CONFIGURATIONS

50(44)-Pin TSOP (Type II)



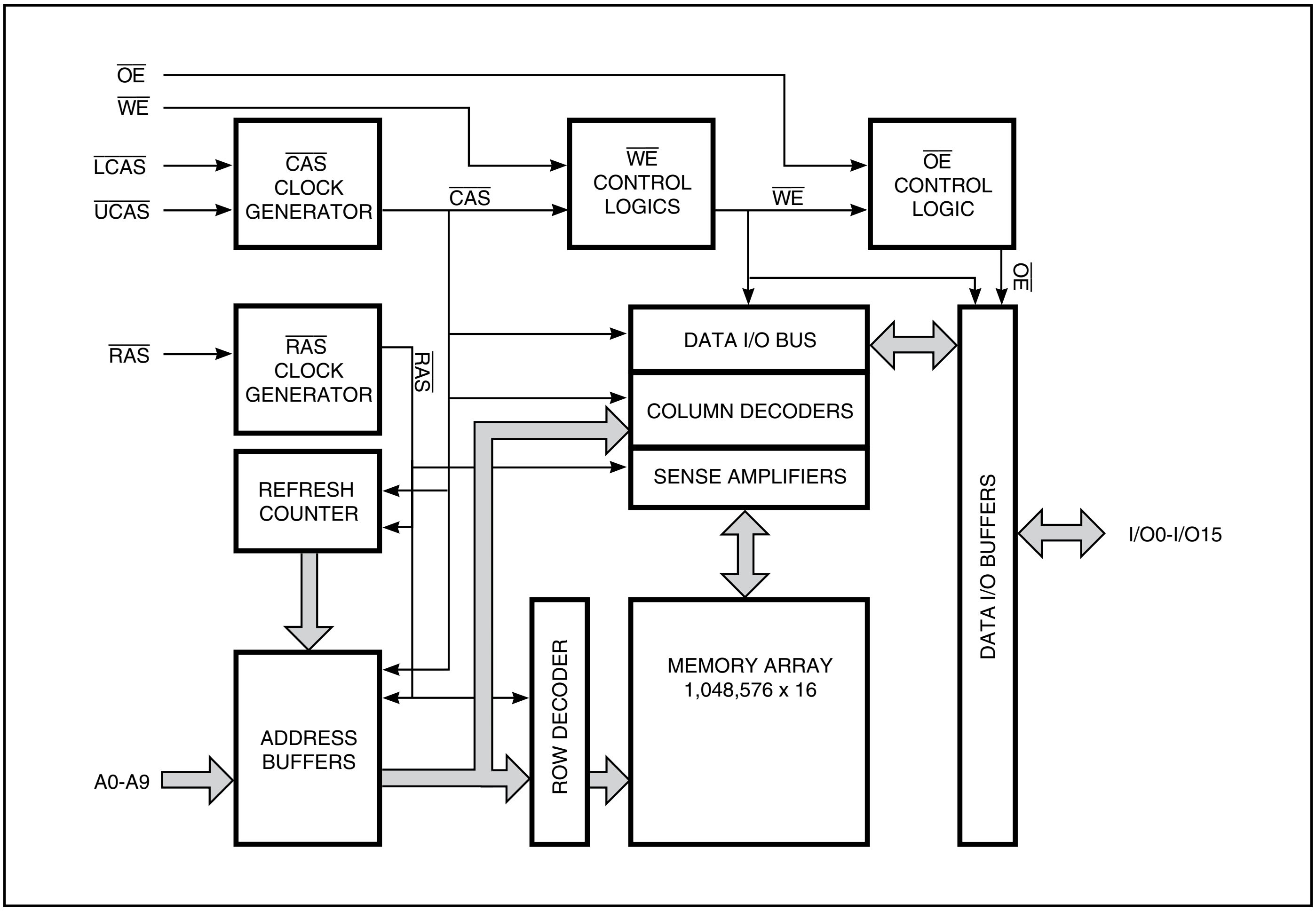
42-Pin SOJ



PIN DESCRIPTIONS

A0-A9	Address Inputs
I/O0-15	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
V_{DD}	Power
GND	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE(5)

Function	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Address t_R/t_C	I/O
Standby	H	X	X	X	X	X	High-Z
Read: Word	L	L	L	H	L	ROW/COL	D_{OUT}
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, D_{OUT} Upper Byte, High-Z
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, D_{OUT}
Write: Word (Early Write)	L	L	L	L	X	ROW/COL	D_{IN}
Write: Lower Byte (Early Write)	L	L	H	L	X	ROW/COL	Lower Byte, D_{IN} Upper Byte, High-Z
Write: Upper Byte (Early Write)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, D_{IN}
Read-Write(1,2)	L	L	L	H→L	L→H	ROW/COL	D_{OUT}, D_{IN}
EDO Page-Mode Read(2) 1st Cycle:	L	H→L	H→L	H	L	ROW/COL	D_{OUT}
2nd Cycle:	L	H→L	H→L	H	L	NA/COL	D_{OUT}
Any Cycle:	L	L→H	L→H	H	L	NA/NA	D_{OUT}
EDO Page-Mode Write(1) 1st Cycle:	L	H→L	H→L	L	X	ROW/COL	D_{IN}
2nd Cycle:	L	H→L	H→L	L	X	NA/COL	D_{IN}
EDO Page-Mode(1,2) 1st Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	D_{OUT}, D_{IN}
Read-Write 2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/COL	D_{OUT}, D_{IN}
Hidden Refresh Read(2)	L→H→L	L	L	H	L	ROW/COL	D_{OUT}
Write(1,3)	L→H→L	L	L	L	X	ROW/COL	D_{OUT}
$\overline{RAS}$-Only Refresh	L	H	H	X	X	ROW/NA	High-Z
CBR Refresh(4)	H→L	L	L	H	X	X	High-Z

Notes:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).
5. Commands valid only after proper initialization.

Functional Description

The IS41C/41LV16100C is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits. These are entered ten bits (A0-A9) at time. The row address is latched by the Row Address Strobe ($\overline{\text{RAS}}$). The column address is latched by the Column Address Strobe ($\overline{\text{CAS}}$). $\overline{\text{RAS}}$ is used to latch the first nine bits and $\overline{\text{CAS}}$ is used to latch the latter nine bits.

The IS41C/41LV16100C has two $\overline{\text{CAS}}$ controls, $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$. The $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ inputs internally generates a $\overline{\text{CAS}}$ signal functioning in an identical manner to the single $\overline{\text{CAS}}$ input on the other 1M x 16 DRAMs. The key difference is that each $\overline{\text{CAS}}$ controls its corresponding I/O tristate logic (in conjunction with $\overline{\text{OE}}$ and $\overline{\text{WE}}$ and $\overline{\text{RAS}}$). $\overline{\text{LCAS}}$ controls I/O0 through I/O7 and $\overline{\text{UCAS}}$ controls I/O8 through I/O15.

The IS41C/41LV16100C $\overline{\text{CAS}}$ function is determined by the first $\overline{\text{CAS}}$ ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$) transitioning LOW and the last transitioning back HIGH. The two $\overline{\text{CAS}}$ controls give the IS41C16100C and IS41LV16100C both BYTE READ and BYTE WRITE cycle capabilities.

Memory Cycle

A memory cycle is initiated by bring $\overline{\text{RAS}}$ LOW and it is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP}, t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{OE}}$, whichever occurs last, while holding $\overline{\text{WE}}$ HIGH. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{AA}, t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs first.

Auto Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1,024 row addresses (A0 through A9) with $\overline{\text{RAS}}$ at least once every t_{REF} max. Any read, write, read-modify-write or $\overline{\text{RAS}}$-only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is activated by the falling edge of $\overline{\text{RAS}}$, while holding $\overline{\text{CAS}}$ LOW. In $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Self Refresh Cycle

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 128 ms. i.e., 125 µs per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding $\overline{\text{RAS}}$ LOW for the specified tRAS.

The Self Refresh mode is terminated by driving $\overline{\text{RAS}}$ HIGH for a minimum time of tRP. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{\text{RAS}}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a $\overline{\text{RAS}}$-only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

Extended Data Out Page Mode

EDO page mode operation permits all 1,024 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

In EDO page mode, due to the extended data function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one $\overline{\text{RAS}}$ cycle, but the performance is equivalent to that of the fast page mode in that case.

Power-On

During Power-On, $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, and $\overline{\text{WE}}$ must all track with V_{DD} (HIGH) to avoid current surges, and allow initialization to continue. An initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ signal).

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
V_T	Voltage on Any Pin Relative to GND	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
V_{DD}	Supply Voltage	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
I_{OUT}	Output Current		50	mA
P_D	Power Dissipation		1	W
T_A	Industrial Operation Temperature		-40 to +85	°C
T_{STG}	Storage Temperature		–55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(At T_A = -40°C to +85°C for Industrial grade. Voltages are referenced to GND.)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		5V	4.5	5.0	5.5	V
			3.3V	3.0	3.3	3.6	
V_{IH}	Input High Voltage		5V	2.4	—	V_{DD} + 1.0	V
			3.3V	2.0	—	V_{DD} + 0.3	
V_{IL}	Input Low Voltage		5V	–1.0	—	0.8	V
			3.3V	–0.3	—	0.8	
I_{IL}	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{DD}$ Other inputs not under test = 0V		–5		5	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{DD}$		–5		5	µA
V_{OH}	Output High Voltage Level	I_{OH} = –5.0 mA	5V	2.4		—	V
		I_{OH} = –2.0 mA	3.3V	2.4		—	
V_{OL}	Output Low Voltage Level	I_{OL} = 4.2 mA	5V	—		0.4	V
		I_{OL} = 2.0 mA	3.3V	—		0.4	

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance: A0-A9	5	pF
C_{IN2}	Input Capacitance: $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O15	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS(1)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	V_{DD}	Min.	Max.	Unit
I_{DD1}	Standby Current: TTL	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS} \geq V_{IH}$	5V 3.3V	— —	2 2	mA mA
I_{DD2}	Standby Current: CMOS	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS} \geq V_{DD} - 0.2V$	5V 3.3V	— —	1 1	mA mA
I_{DD3}	Operating Current: Random Read/Write$^{(2,3,4)}$ Average Power Supply Current	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, Address Cycling, $t_{RC} = t_{RC}$ (min.)	5V 3.3V	— —	90 90	mA
I_{DD4}	Operating Current: EDO Page Mode$^{(2,3,4)}$ Average Power Supply Current	$\overline{RAS} = V_{IL}$, $\overline{LCAS}$, $\overline{UCAS}$, Cycling $t_{PC} = t_{PC}$ (min.)	5V 3.3V	— —	30 30	mA
I_{DD5}	Refresh Current: $\overline{RAS}$-Only$^{(2,3)}$ Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}$, $\overline{UCAS} \geq V_{IH}$ $t_{RC} = t_{RC}$ (min.)	5V 3.3V	— —	60 60	mA
I_{DD6}	Refresh Current: CBR$^{(2,3,5)}$ Average Power Supply Current	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ Cycling $t_{RC} = t_{RC}$ (min.)	5V 3.3V	— —	60 60	mA

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

		-50		-60		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Random READ or WRITE Cycle Time	85	—	110	—	ns
t_{RAC}	Access Time from $\overline{\text{RAS}}$(6, 7)	—	50	—	60	ns
t_{CAC}	Access Time from $\overline{\text{CAS}}$(6, 8, 15)	—	14	—	15	ns
t_{AA}	Access Time from Column-Address(6)	—	25	—	30	ns
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	ns
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width(26)	8	10K	10	10K	ns
t_{CP}	$\overline{\text{CAS}}$ Precharge Time(9, 25)	9	—	10	—	ns
t_{CSH}	$\overline{\text{CAS}}$ Hold Time (21)	50	—	60	—	ns
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time(10, 20)	12	37	20	45	ns
t_{ASR}	Row-Address Setup Time	0	—	0	—	ns
t_{RAH}	Row-Address Hold Time	8	—	10	—	ns
t_{ASC}	Column-Address Setup Time(20)	0	—	0	—	ns
t_{CAH}	Column-Address Hold Time(20)	8	—	10	—	ns
t_{AR}	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$)	30	—	40	—	ns
t_{RAD}	$\overline{\text{RAS}}$ to Column-Address Delay Time(11)	14	25	15	30	ns
t_{RAL}	Column-Address to $\overline{\text{RAS}}$ Lead Time	25	—	30	—	ns
t_{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	—	5	—	ns
t_{RSH}	$\overline{\text{RAS}}$ Hold Time(27)	14	—	15	—	ns
t_{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	37	—	37	—	ns
t_{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z(15, 29)	0	—	0	—	ns
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time(21)	5	—	5	—	ns
t_{OD}	Output Disable Time(19, 28, 29)	3	12	3	12	ns
t_{OE}/t_{OEA}	Output Enable Time(15, 16)	—	14	—	15	ns
t_{OEHC}	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	15	—	15	—	ns
t_{OEP}	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	ns
t_{OES}	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	ns
t_{RCS}	Read Command Setup Time(17, 20)	0	—	0	—	ns
t_{RRH}	Read Command Hold Time (referenced to $\overline{\text{RAS}}$)(12)	0	—	0	—	ns
t_{RCH}	Read Command Hold Time (referenced to $\overline{\text{CAS}}$)(12, 17, 21)	0	—	0	—	ns
t_{WCH}	Write Command Hold Time(17, 27)	8	—	10	—	ns
t_{WCR}	Write Command Hold Time (referenced to $\overline{\text{RAS}}$)(17)	40	—	50	—	ns

AC CHARACTERISTICS (Continued)(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

		-50		-60		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{WP}	Write Command Pulse Width(17)	8	—	10	—	ns
t_{WPZ}	$\overline{WE}$ Pulse Widths to Disable Outputs	10	—	10	—	ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time(17)	13	—	15	—	ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time(17, 21)	8	—	15	—	ns
t_{WCS}	Write Command Setup Time(14, 17, 20)	0	—	0	—	ns
t_{DHR}	Data-in Hold Time (referenced to $\overline{RAS}$)	39	—	40	—	ns
t_{ACH}	Column-Address Setup Time to $\overline{CAS}$ precharge during WRITE cycle	15	—	15	—	ns
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle(18)	14	—	15	—	ns
t_{DS}	Data-In Setup Time(15, 22)	0	—	0	—	ns
t_{DH}	Data-In Hold Time(15, 22)	8	—	15	—	ns
t_{RWC}	READ-MODIFY-WRITE Cycle Time	110	—	155	—	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle(14)	65	—	85	—	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time(14, 20)	26	—	40	—	ns
t_{AWD}	Column-Address to $\overline{WE}$ Delay Time(14)	40	—	55	—	ns
t_{PC}	EDO Page Mode READ or WRITE Cycle Time(24)	30	—	40	—	ns
t_{RASP}	$\overline{RAS}$ Pulse Width in EDO Page Mode	50	100K	60	100K	ns
t_{CPA}	Access Time from $\overline{CAS}$ Precharge(15)	—	30	—	35	ns
t_{PRWC}	EDO Page Mode READ-WRITE Cycle Time(24)	56	—	56	—	ns
t_{COH}	Data Output Hold after $\overline{CAS}$ LOW	5	—	5	—	ns
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$(13,15,19, 29)	3	12	3	15	ns
t_{WHZ}	Output Disable Delay from $\overline{WE}$	3	10	3	15	ns
t_{CLCH}	Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH(23)	10	—	10	—	ns
t_{CSR}	$\overline{CAS}$ Setup Time (CBR REFRESH)(30, 20)	5	—	5	—	ns
t_{CHR}	$\overline{CAS}$ Hold Time (CBR REFRESH)(30, 21)	8	—	10	—	ns
t_{ORD}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	ns
t_{WRP}	$\overline{WE}$ Setup Time (CBR Refresh)	5	—	5	—	ns
t_{WRH}	$\overline{WE}$ Hold Time (CBR Refresh)	8	—	10	—	ns
t_{REF}	Auto Refresh Period (1,024 Cycles)	—	16	—	16	ms
t_{REF}	Self Refresh Period (1,024 Cycles)	—	128	—	128	ms
t_{T}	Transition Time (Rise or Fall)(2, 3)	1	50	1	50	ns

Note:
The -60 timing parameters are shown for reference only. The -50 speed option supports 50ns and 60ns timing specifications.

AC TEST CONDITIONS

Output load: Two TTL Loads and 100 pF (V_{DD} = 5.0V ±10%)
One TTL Load and 50 pF (V_{DD} = 3.3V ±10%)

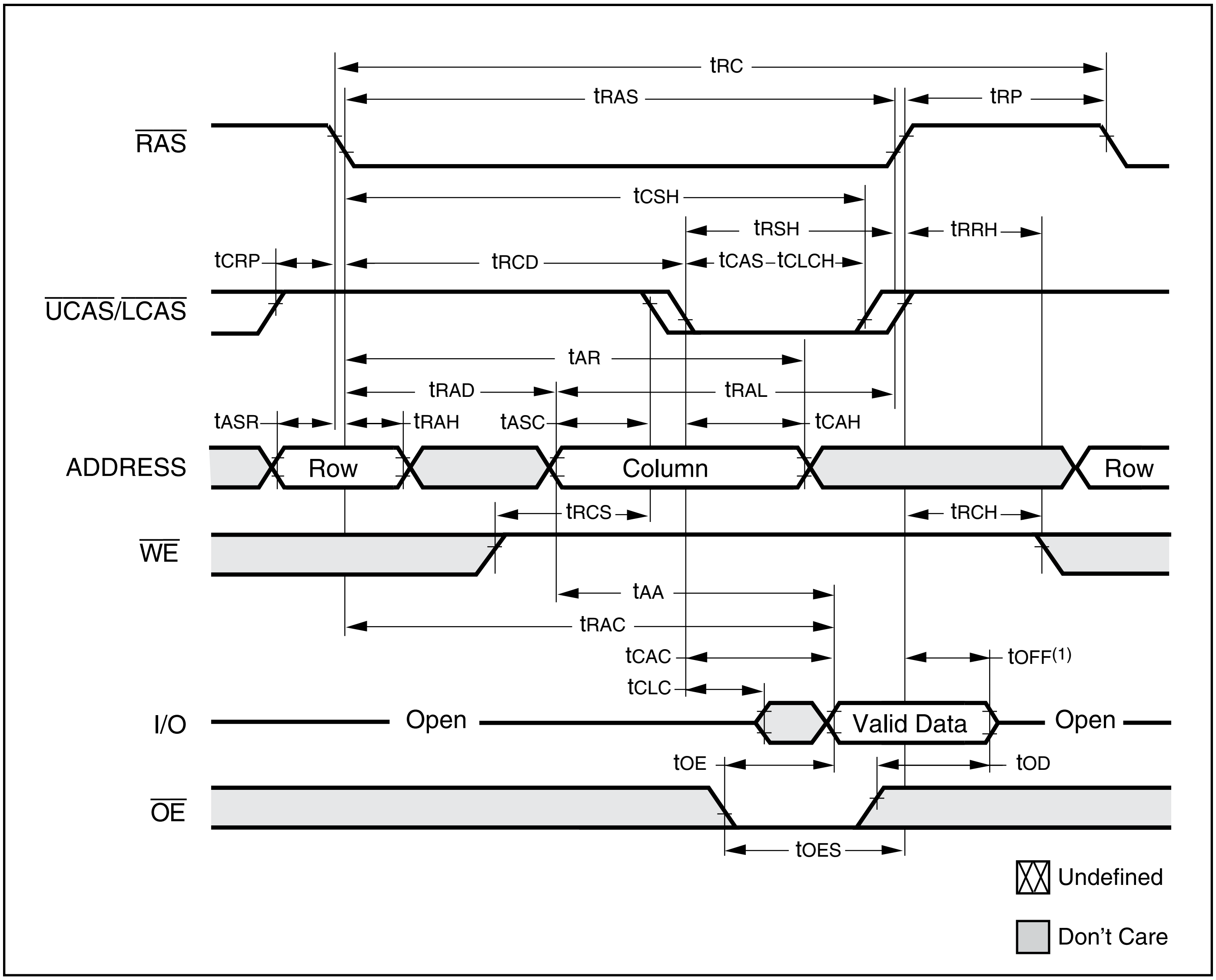
Input timing reference levels: V_{IH} = 2.4V, V_{IL} = 0.8V (V_{DD} = 5.0V ±10%);
V_{IH} = 2.0V, V_{IL} = 0.8V (V_{DD} = 3.3V ±10%)

Output timing reference levels: V_{OH} = 2.4V, V_{OL} = 0.4V (V_{DD} = 5V ±10%, 3.3V ±10%)

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
5. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for t_{CP}.
10. Operation with the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, access time is controlled exclusively by t_{CAC}.
11. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, access time is controlled exclusively by t_{AA}.
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
14. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \leq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} \leq t_{RWD}$ (MIN), $t_{AWD} \leq t_{AWD}$ (MIN) and $t_{CWD} \leq t_{CWD}$ (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, I/O0-I/O7 by $\overline{LCAS}$ and I/O8-I/O15 by $\overline{UCAS}$.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first $\chi\overline{CAS}$ edge to transition LOW.
21. The last $\chi\overline{CAS}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{CAS}$ edge to first rising $\chi\overline{CAS}$ edge.
24. Last rising $\chi\overline{CAS}$ edge to next cycle's last rising $\chi\overline{CAS}$ edge.
25. Last rising $\chi\overline{CAS}$ edge to first falling $\chi\overline{CAS}$ edge.
26. Each $\chi\overline{CAS}$ must meet minimum pulse width.
27. Last $\chi\overline{CAS}$ to go LOW.
28. I/Os controlled, regardless $\overline{UCAS}$ and $\overline{LCAS}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

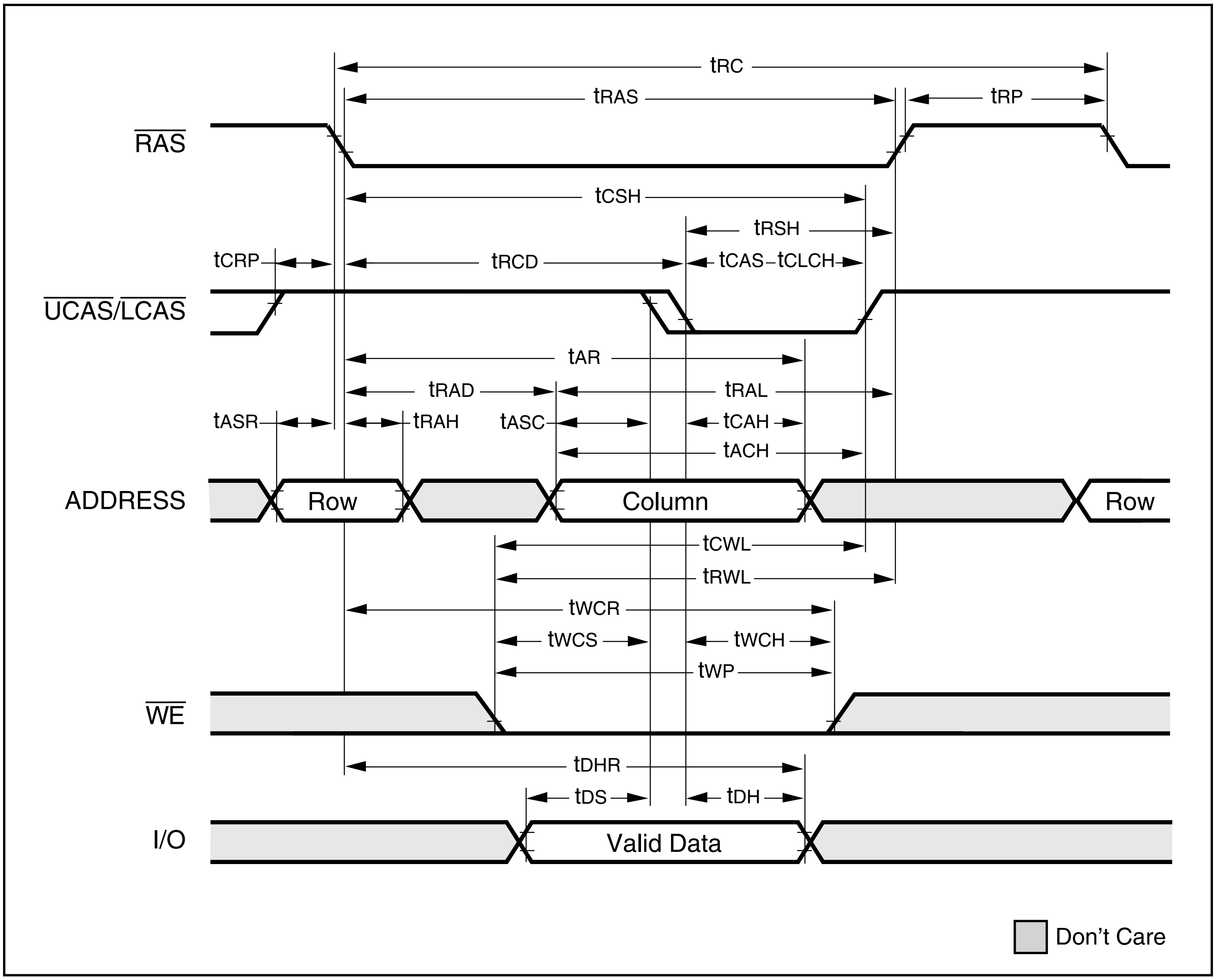
READ CYCLE



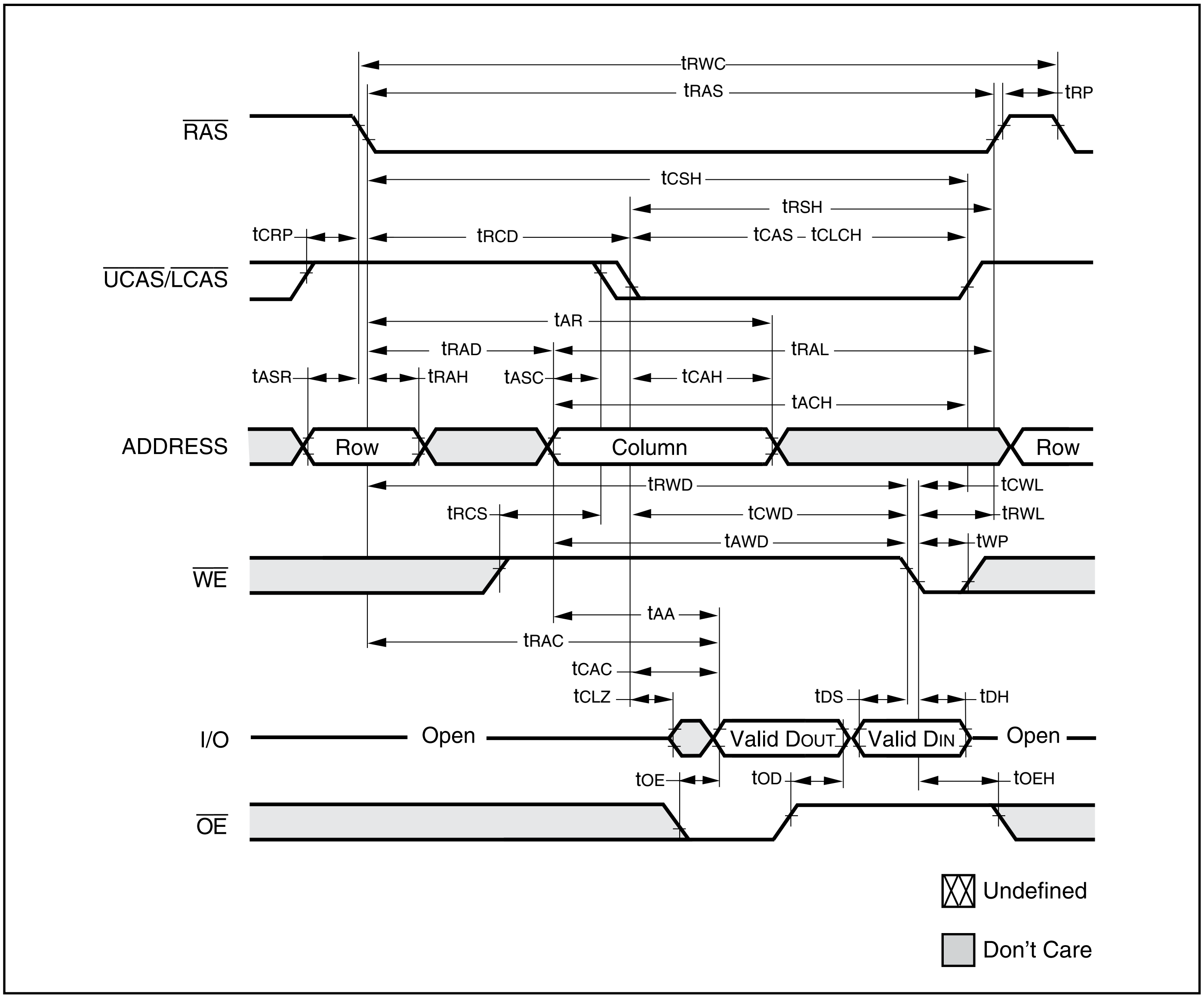
Note:

1. tOFF is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

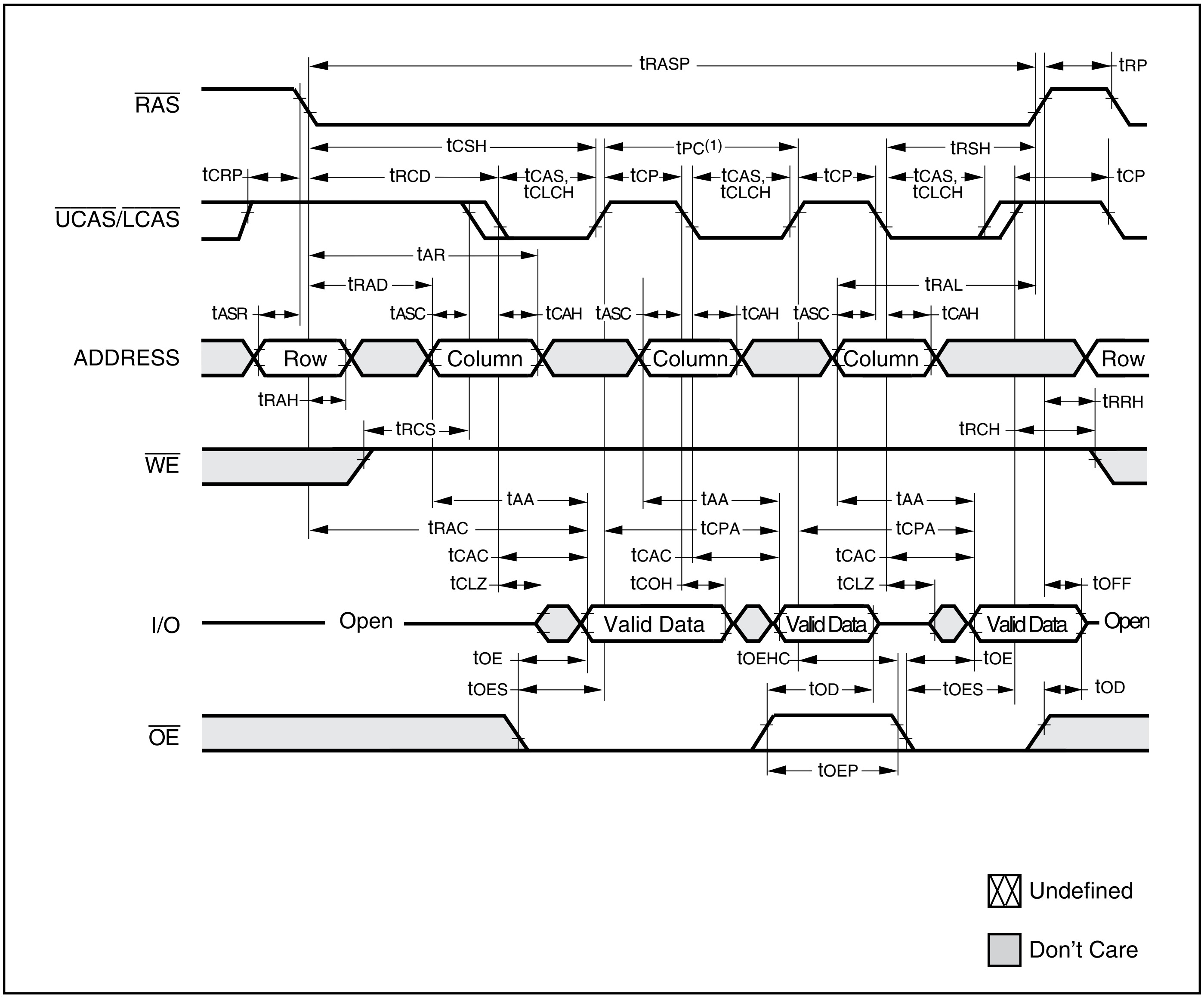
EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



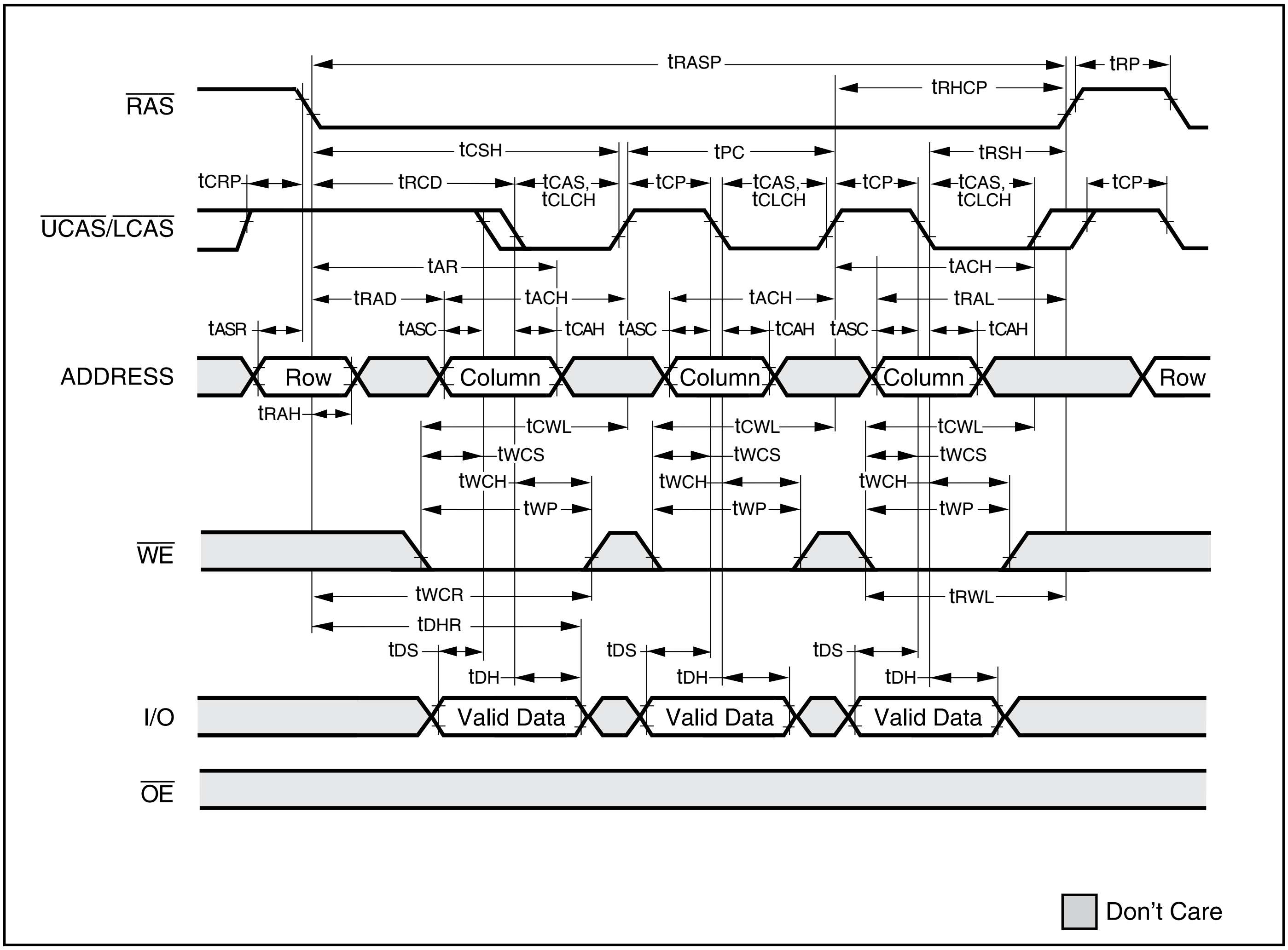
EDO-PAGE-MODE READ CYCLE



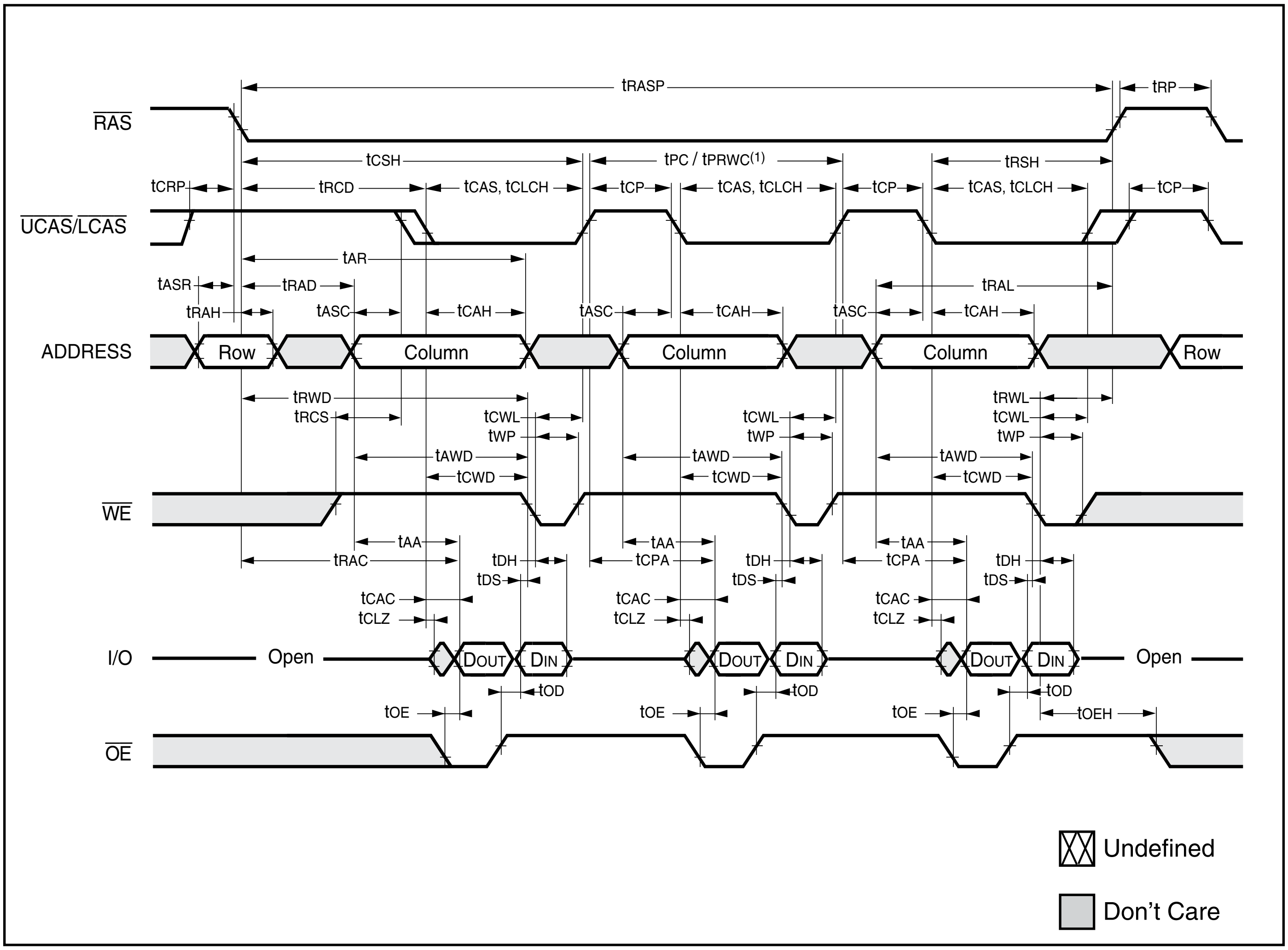
Note:

1. tPC can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



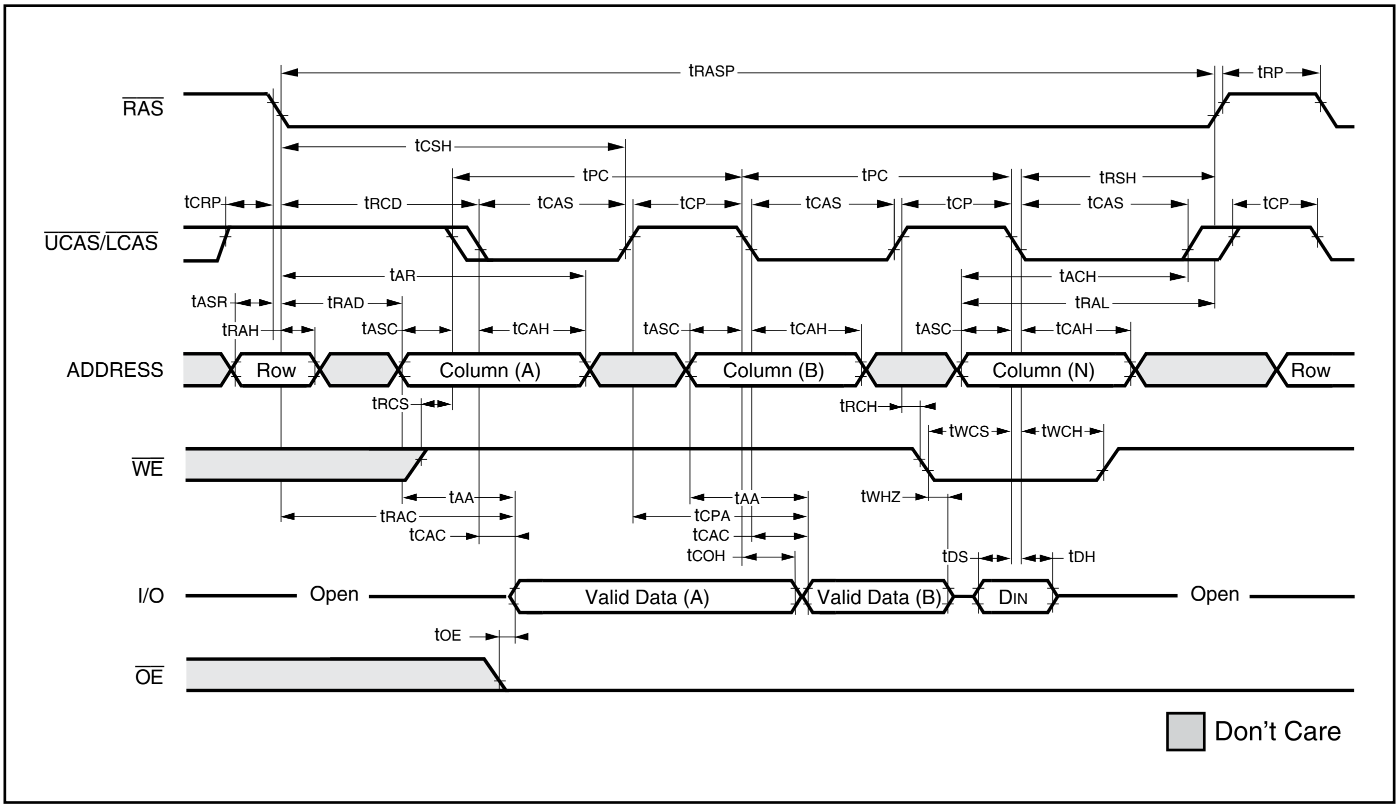
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



Note:

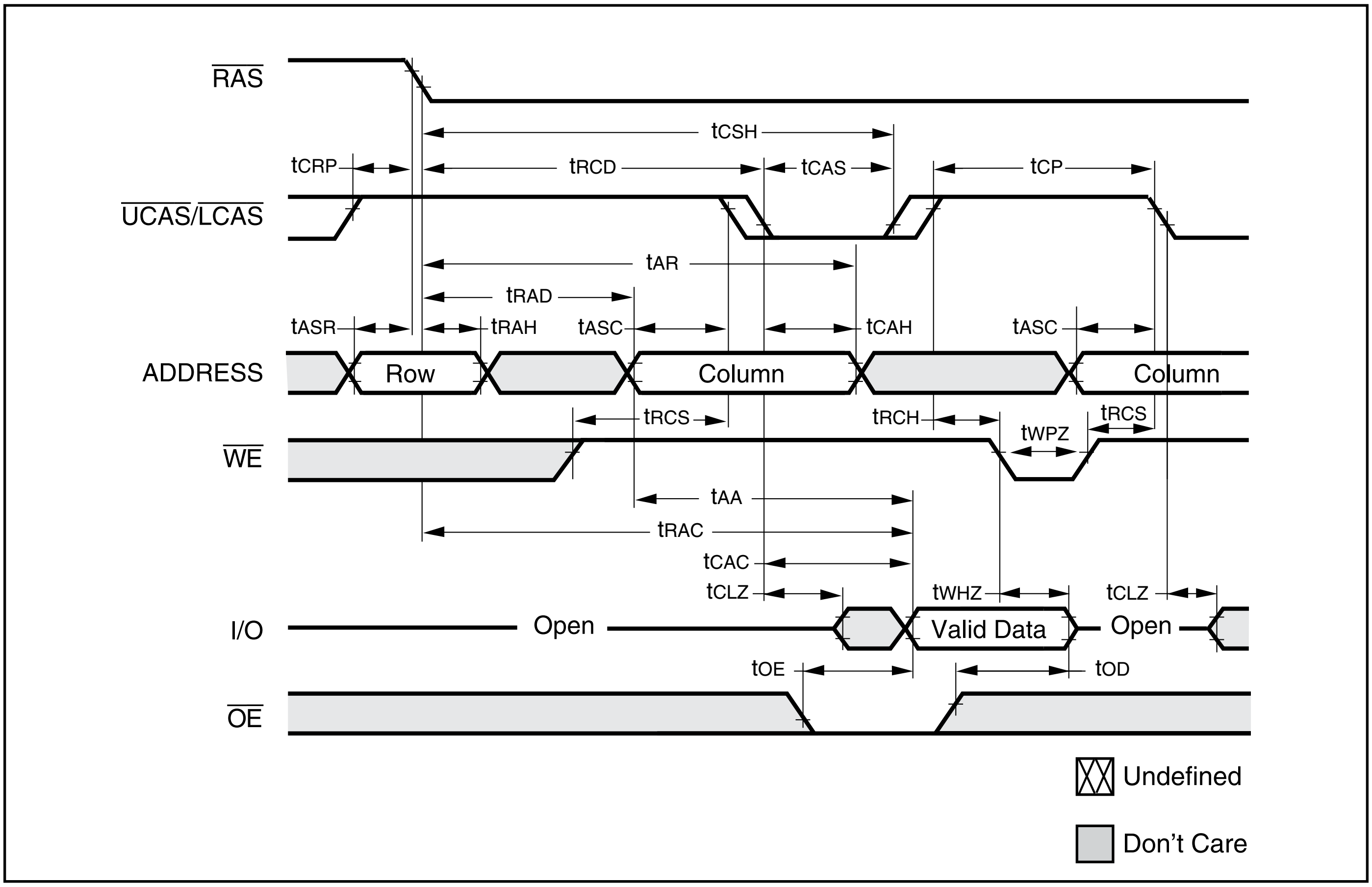
1. t_{PC} can be measured from falling edge of $\overline{\text{CAS}}$ to falling edge of $\overline{\text{CAS}}$, or from rising edge of $\overline{\text{CAS}}$ to rising edge of $\overline{\text{CAS}}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY WRITE)

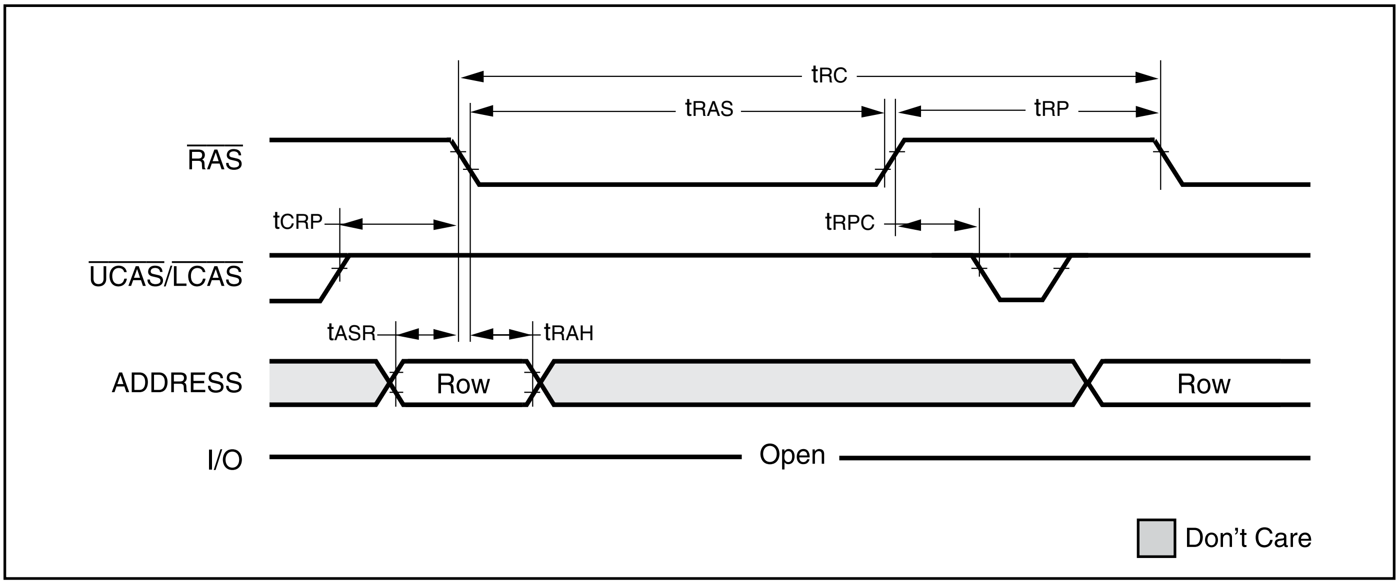


AC WAVEFORMS

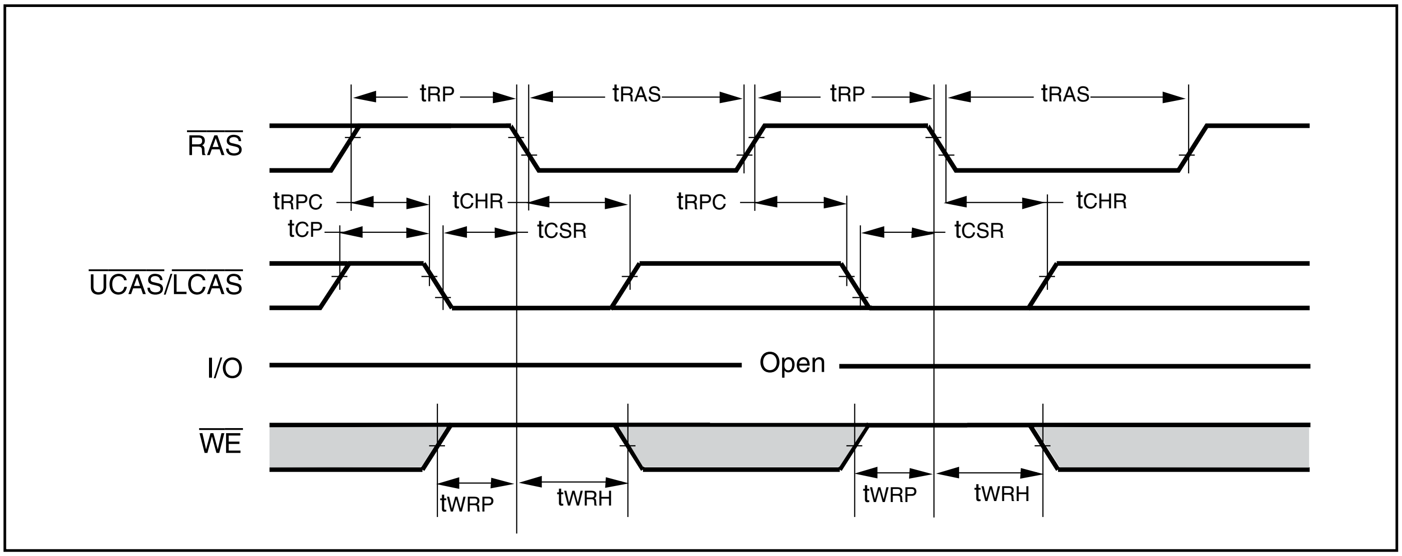
READ CYCLE (With $\overline{\text{WE}}$-Controlled Disable)



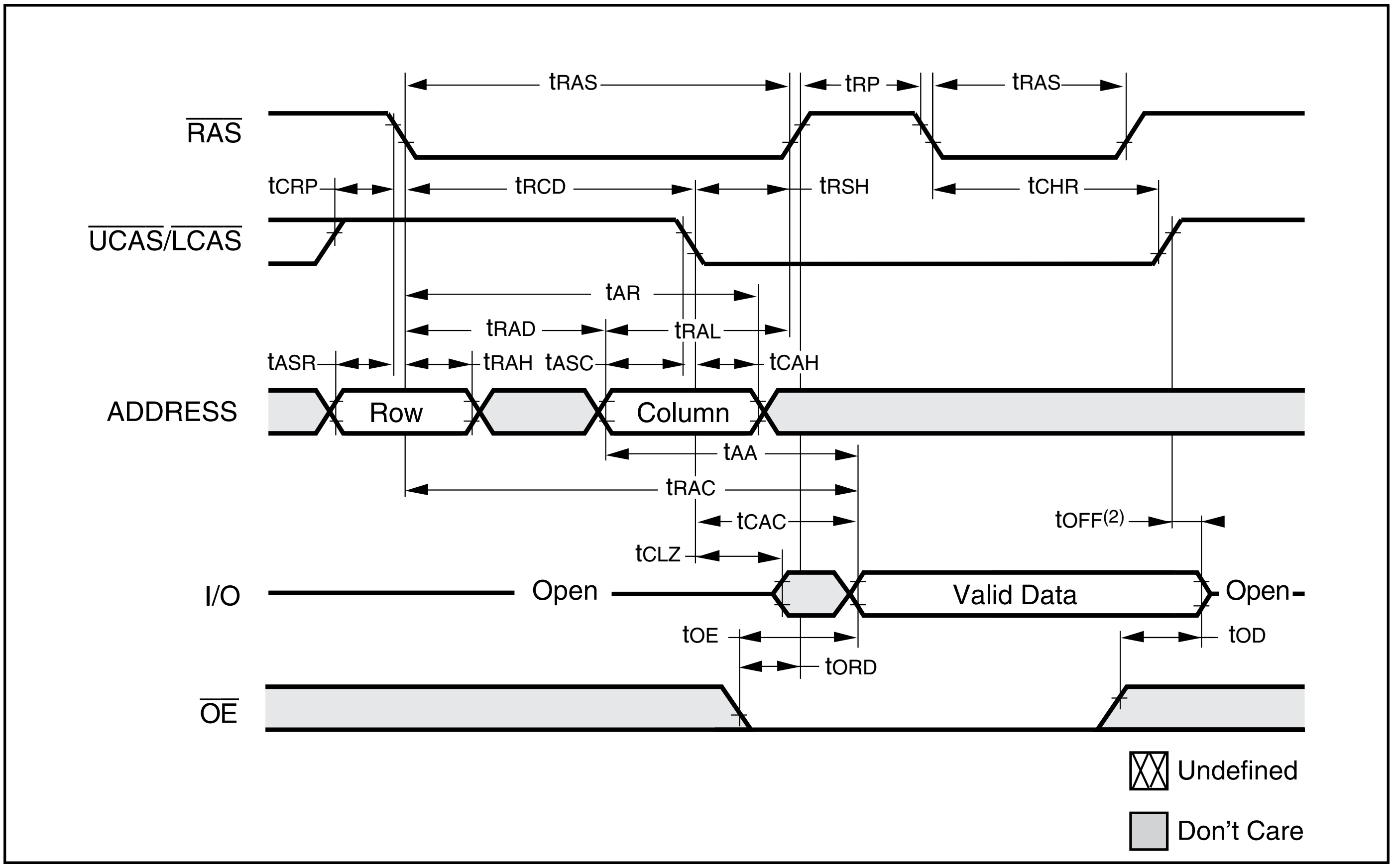
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE ($\overline{\text{OE}}$, $\overline{\text{WE}}$ = DON'T CARE)



CBR REFRESH CYCLE (Addresses; OE = DON'T CARE)



HIDDEN REFRESH CYCLE[(1)] (WE = HIGH; OE = LOW)



Notes:
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, WE = LOW and OE = HIGH.
2. tOFF is referenced from rising edge of RAS or CAS, whichever occurs last.

ORDERING INFORMATION : 5V

Industrial Range: -40°C to +85°C

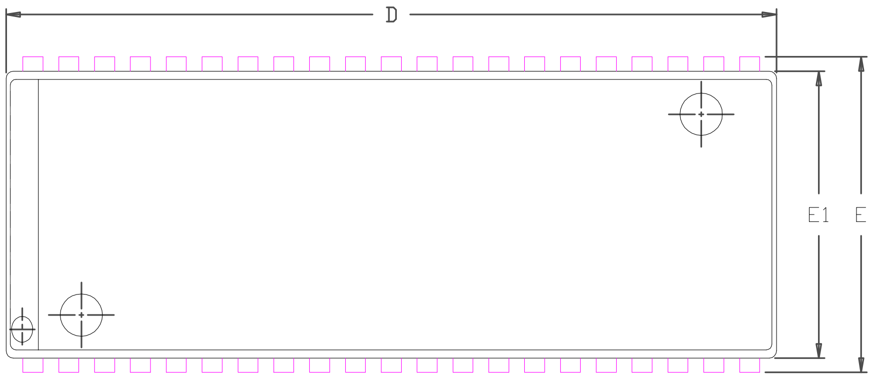
Speed (ns)	Order Part No.	Package
50	IS41C16100C-50KI	400-mil SOJ
	IS41C16100C-50KLI	400-mil SOJ, Lead-free
	IS41C16100C-50TI	400-mil TSOP (Type II)
	IS41C16100C-50TLI	400-mil TSOP (Type II), Lead-free

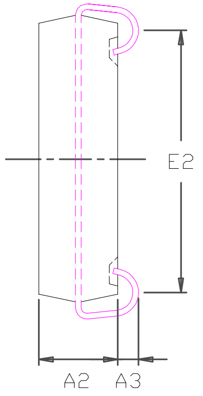
ORDERING INFORMATION : 3.3V

Industrial Range: -40°C to +85°C

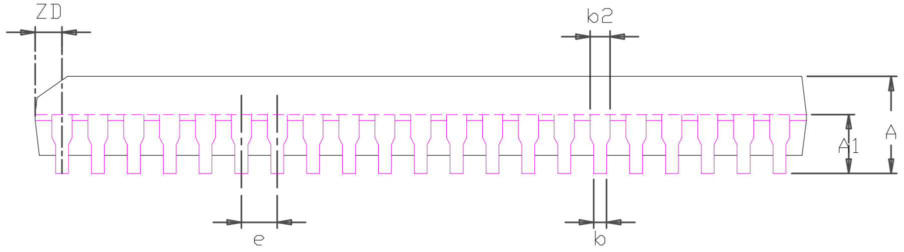
Speed (ns)	Order Part No.	Package
50	IS41LV16100C-50KI	400-mil SOJ
	IS41LV16100C-50KLI	400-mil SOJ, Lead-free
	IS41LV16100C-50TI	400-mil TSOP (Type II)
	IS41LV16100C-50TLI	400-mil TSOP (Type II), Lead-free

Note:
The -50 speed option supports 50ns and 60ns timing specifications.





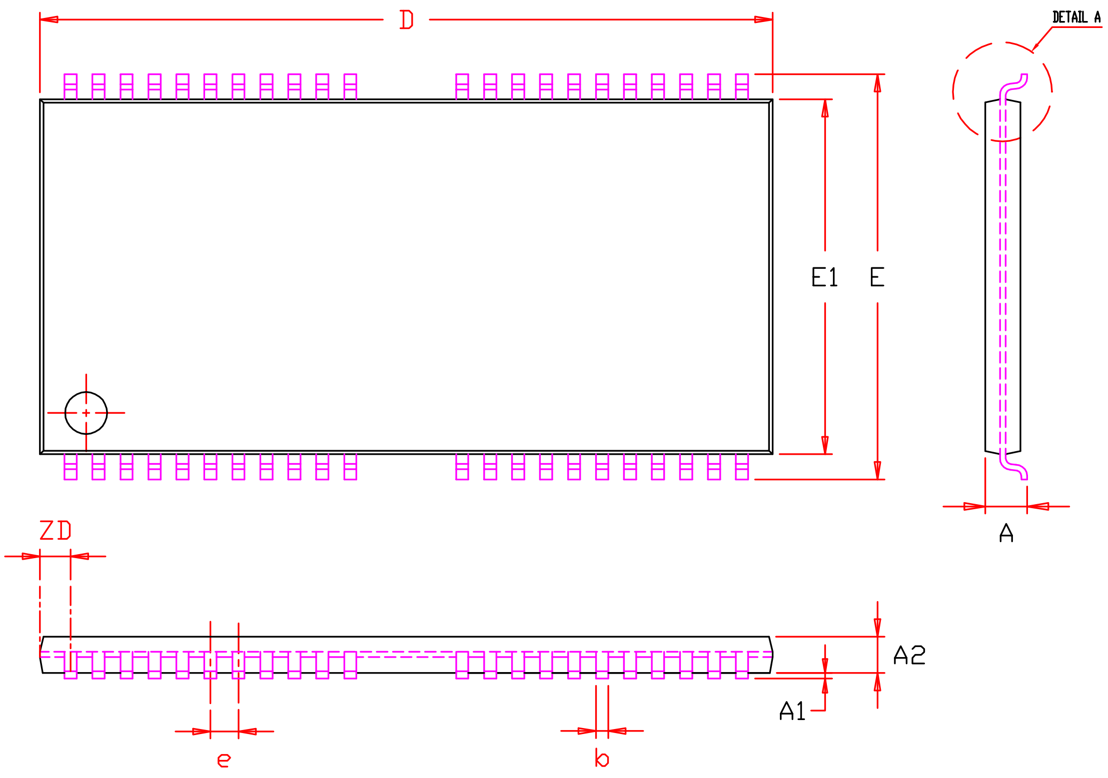
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	2.70	0.082	—	0.106
A2	2.61	—	2.92	0.103	—	0.115
A3	0.64	—	0.84	0.025	—	0.033
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	—	0.81	0.026	—	0.032
D	27.18	—	27.43	1.070	—	1.080
E	11.03	11.18	11.33	0.434	0.440	0.446
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.14	—	9.65	0.360	—	0.380
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		



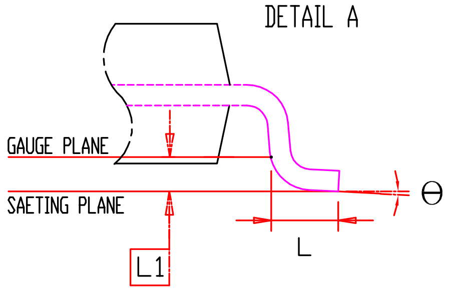
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	42L 400mil SOJ Package Outline	REV.	C	DATE	03/19/2009



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.875 REF.			0.034 REF.		
Θ	0	—	8°	0	—	8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	44/50L 400mil TSOP-2 Package Outline	REV.	E	DATE	03/19/2009