

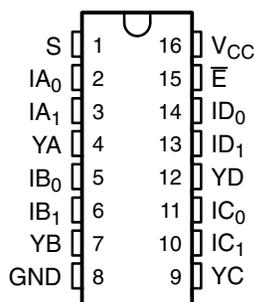
TS3L110

QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH DIFFERENTIAL 8-CHANNEL TO 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER

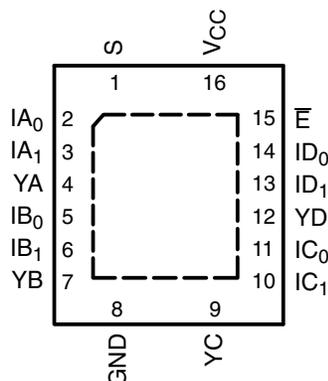
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- Wide Bandwidth (BW = 500 MHz Typ)
- Low Crosstalk ($X_{TALK} = -30$ dB Typ)
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low and Flat ON-State Resistance ($r_{on} = 4 \Omega$ Typ, $r_{on(Flat)} = 1 \Omega$)
- Switching on Data I/O Ports (0 to 5 V)
- V_{CC} Operating Range From 3 V to 3.6 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Data and Control Inputs Have Undershoot Clamp Diodes
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Suitable for Both 10 Base-T/100 Base-T Signaling

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (\bar{E}) input. When \bar{E} is low, the switch is enabled, and the I port is connected to the Y port. When \bar{E} is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RGY | Tape and reel | TS3L110RGYR | TK110 |
| | SOIC – D | Tube | TS3L110D | TS3L110 |
| | | Tape and reel | TS3L110DR | |
| | SSOP (QSOP) – DBQ | Tape and reel | TS3L110DBQR | TK110 |
| | TSSOP – PW | Tube | TS3L110PW | TK110 |
| | | Tape and reel | TS3L110PWR | |
| TVSOP – DGV | Tape and reel | TS3L110DGVR | TK110 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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TS3L110
QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH
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description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low and flat r_{on} , wide bandwidth, and low crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications. The device can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations. The device is designed for low channel-to-channel skew and low crosstalk.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \bar{E} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

| INPUTS | | INPUT/OUTPUT YX | FUNCTION |
|-----------|---|--------------------|-------------|
| \bar{E} | S | | |
| L | L | IX_0 | $YX = IX_0$ |
| L | H | IX_1 | $YX = IX_1$ |
| H | X | Z | Disconnect |

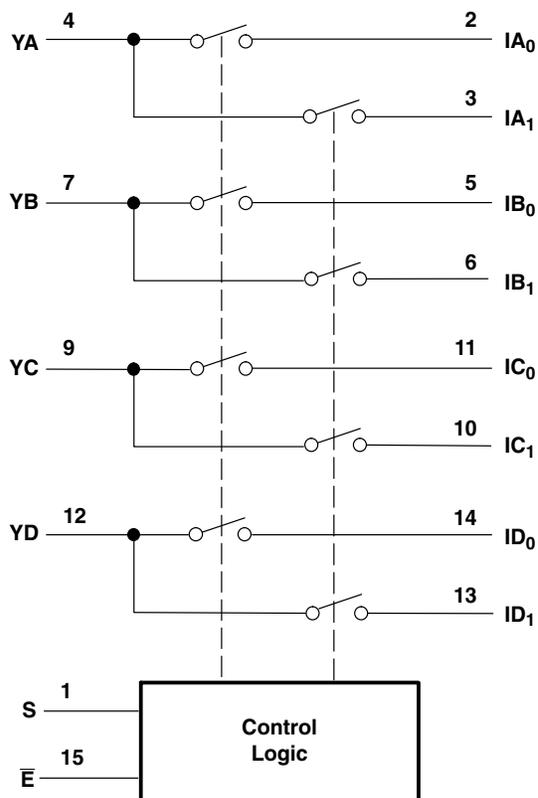
PIN DESCRIPTIONS

| PIN NAME | DESCRIPTION |
|-----------|--------------|
| $IAn-IDn$ | Data I/Os |
| S | Select input |
| \bar{E} | Enable input |
| $YA-YD$ | Data I/Os |



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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Control input voltage range, V_{IN} (see Notes 1 and 2) | -0.5 V to 7 V |
| Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) | -0.5 V to 7 V |
| Control input clamp current, I_{IK} ($V_{IN} < 0$) | -50 mA |
| I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) | -50 mA |
| ON-state switch current, $I_{I/O}$ (see Note 4) | ± 128 mA |
| Continuous current through V_{CC} or GND terminals | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 5): D package | 73°C/W |
| (see Note 5): DBQ package | 90°C/W |
| (see Note 5): DGV package | 120°C/W |
| (see Note 5): PW package | 108°C/W |
| (see Note 6): RGY package | 39°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.
 6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

| | | MIN | MAX | UNIT |
|-----------|---|-----|-----|------|
| V_{CC} | Supply voltage | 3 | 3.6 | V |
| V_{IH} | High-level control input voltage (\bar{E} , S) | 2 | 5.5 | V |
| V_{IL} | Low-level control input voltage (\bar{E} , S) | 0 | 0.8 | V |
| $V_{I/O}$ | Input/output voltage | 0 | 5.5 | V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------------|--------------|--------------------------|---------------------------------------|-----|------|---------|---------------|
| V_{IK} | \bar{E}, S | $V_{CC} = 3.6\text{ V},$ | $I_{IN} = -18\text{ mA}$ | | | -1.8 | V |
| I_{IH} | \bar{E}, S | $V_{CC} = 3.6\text{ V},$ | $V_{IN} = 5.5\text{ V}$ | | | ± 1 | μA |
| I_{IL} | \bar{E}, S | $V_{CC} = 3.6\text{ V},$ | $V_{IN} = \text{GND}$ | | | ± 1 | μA |
| I_{off} | | $V_{CC} = 0,$ | $V_O = 0\text{ to }5.5\text{ V},$ | | | 1 | μA |
| I_{CC} | | $V_{CC} = 3.6\text{ V},$ | $I_{I/O} = 0,$ | | | 0.7 1.5 | mA |
| C_{in} | \bar{E}, S | $f = 1\text{ MHz},$ | $V_{IN} = 0$ | | | 2.5 3.5 | pF |
| $C_{io(OFF)}$ | I port | $V_I = 0,$ | $f = 1\text{ MHz},$ Outputs open, | | | 3.5 5 | pF |
| | Y port | $V_I = 0,$ | $f = 1\text{ MHz},$ Outputs open, | | | 5.5 7 | |
| $C_{io(ON)}$ | I or Y port | $V_I = 0,$ | $f = 1\text{ MHz},$ Outputs open, | | | 10.5 13 | pF |
| r_{on} | | $V_{CC} = 3\text{ V}$ | $1.25\text{ V} \leq V_I \leq V_{CC},$ | | | 4 8 | Ω |
| $r_{on(flat)}^\ddagger$ | | $V_{CC} = 3\text{ V}$ | $V_I = 1.25\text{ V}$ and $V_{CC},$ | | | 1 | Ω |
| Δr_{on}^\S | | $V_{CC} = 3\text{ V},$ | $1.25\text{ V} \leq V_I \leq V_{CC},$ | | | 0.9 2 | Ω |

$V_I, V_O, I_I,$ and I_O refer to I/O pins. V_{IN} refers to the control inputs.

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.

§ Δr_{on} is the difference of r_{on} in a given device.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}, R_L = 200\ \Omega, C_L = 10\text{ pF}$ (unless otherwise noted) (see Figures 5 and 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|--------------------|----------------|-------------|-----|---------|-----|------|
| t_{pd}^\parallel | I or Y | Y or I | | 0.25 | | ns |
| t_{PZH}, t_{PZL} | \bar{E} or S | I or Y | | 0.5 | 7 | ns |
| t_{PHZ}, t_{PLZ} | \bar{E} or S | I or Y | | 0.5 | 5 | ns |
| $t_{sk(p)}^\#$ | I or Y | Y or I | | 0.1 0.2 | | ns |

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$. This parameter is not production tested.

dynamic characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------|---|-----|------|-----|------|
| X_{TALK} | $R_L = 100\ \Omega,$ $f = 250\text{ MHz},$ see Figure 7 | | -26 | | dB |
| O_{IRR} | $R_L = 100\ \Omega,$ $f = 250\text{ MHz},$ see Figure 8 | | -28 | | dB |
| BW | $R_L = 100\ \Omega,$ see Figure 6 | | 500 | | MHz |

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.



OPERATING CHARACTERISTICS

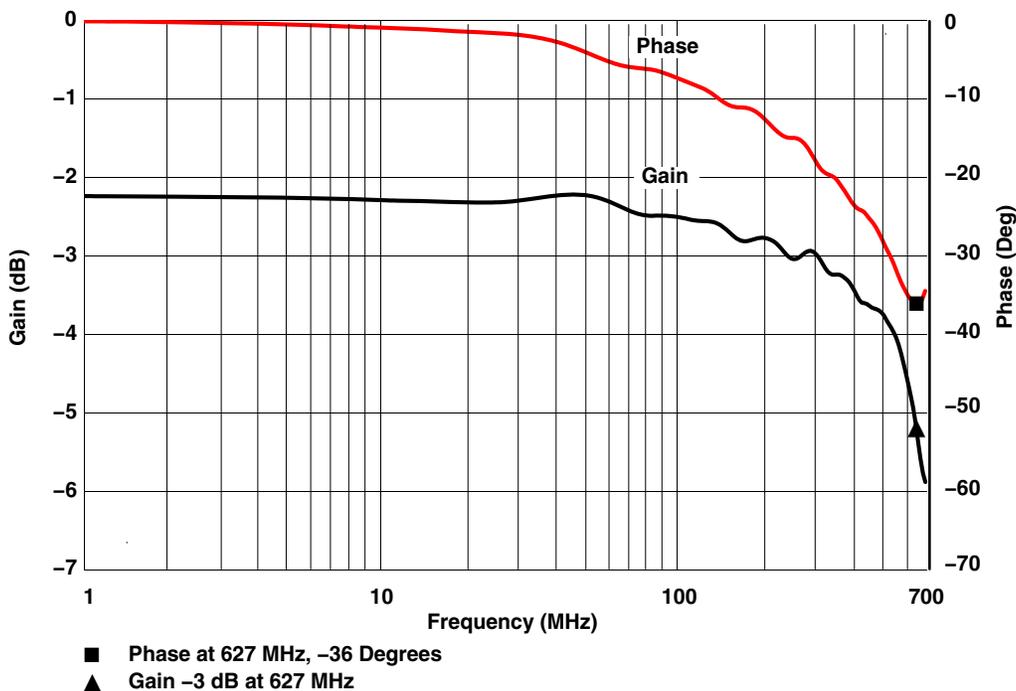


Figure 1. Gain/Phase vs Frequency

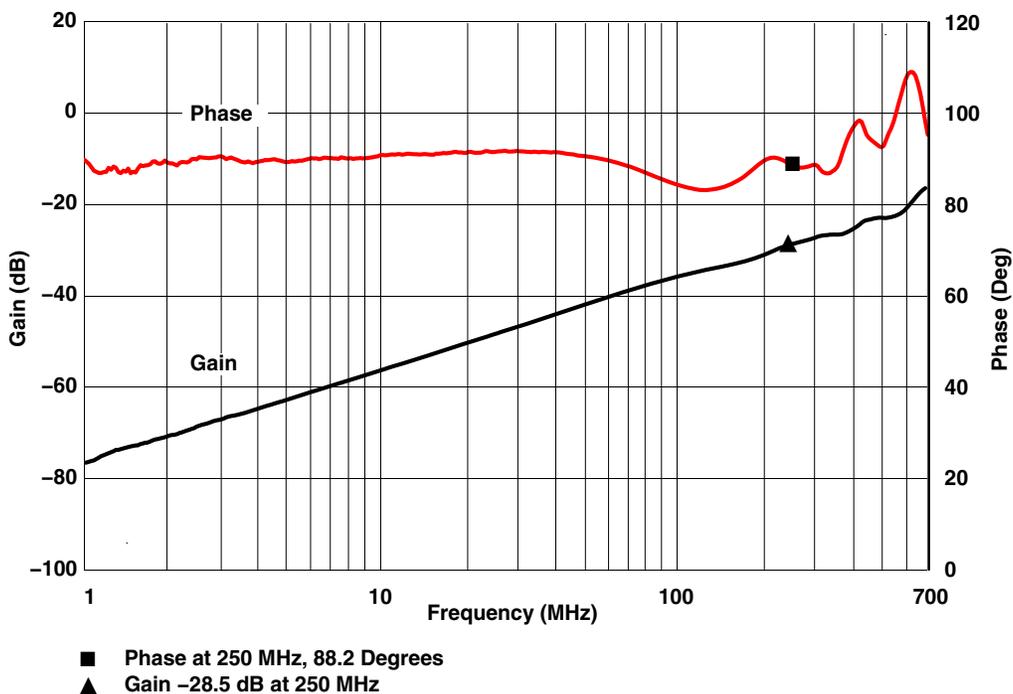


Figure 2. OFF Isolation vs Frequency

OPERATING CHARACTERISTICS

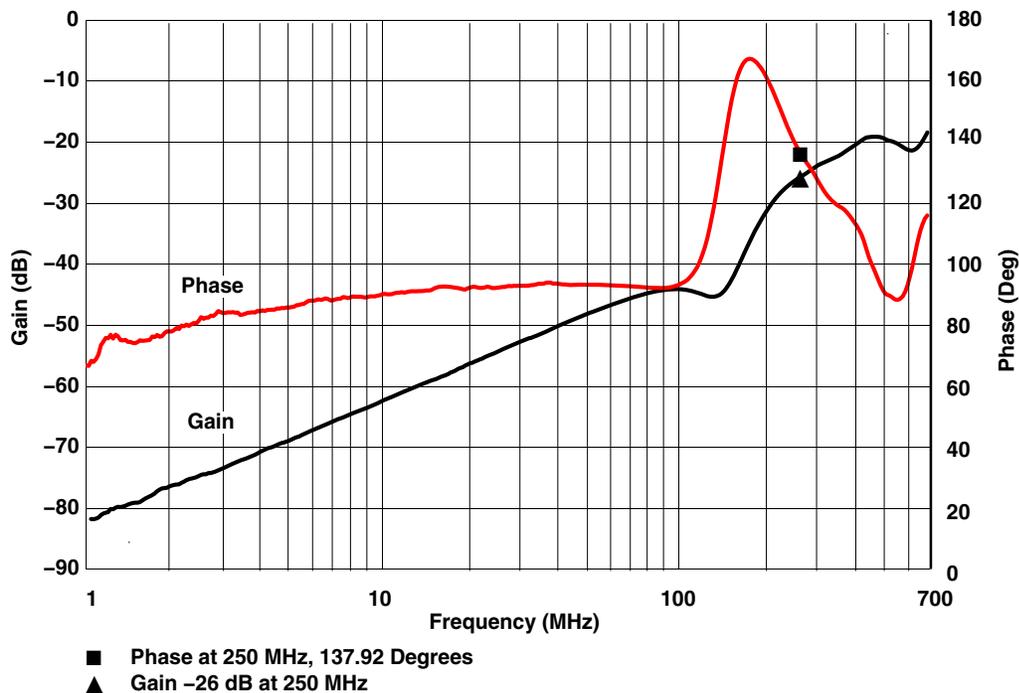


Figure 3. Crosstalk vs Frequency

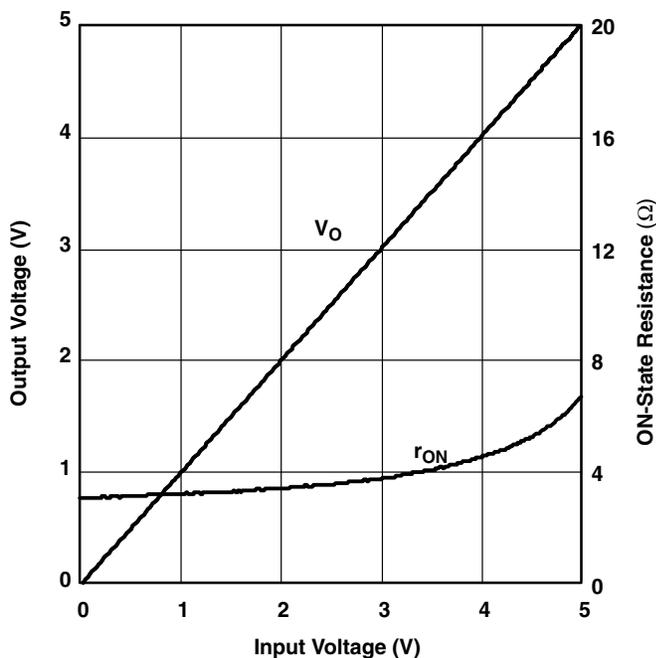
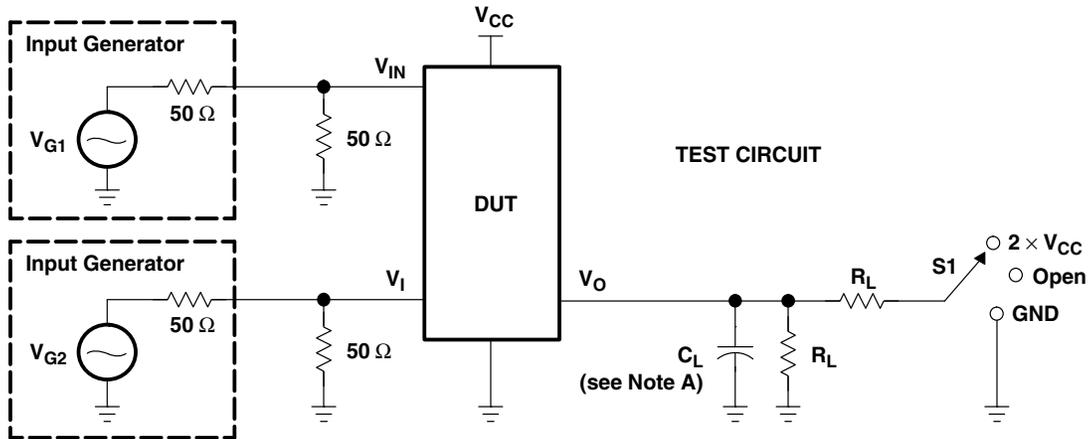


Figure 4. Output Voltage/ON-State Resistance vs Input Voltage

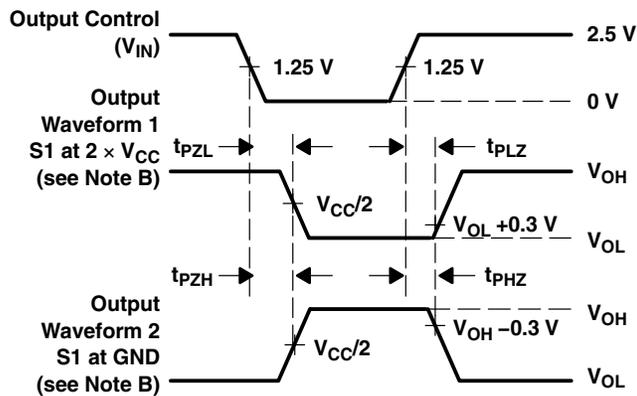
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PARAMETER MEASUREMENT INFORMATION
FOR ENABLE AND DISABLE TIMES



| TEST | V _{CC} | S1 | R _L | V _I | C _L | V _Δ |
|------------------------------------|-----------------|---------------------|----------------|-----------------|----------------|----------------|
| t _{PLZ} /t _{PZL} | 3.3 V ± 0.3 V | 2 × V _{CC} | 200 Ω | GND | 10 pF | 0.3 V |
| t _{PHZ} /t _{PZH} | 3.3 V ± 0.3 V | GND | 200 Ω | V _{CC} | 10 pF | 0.3 V |

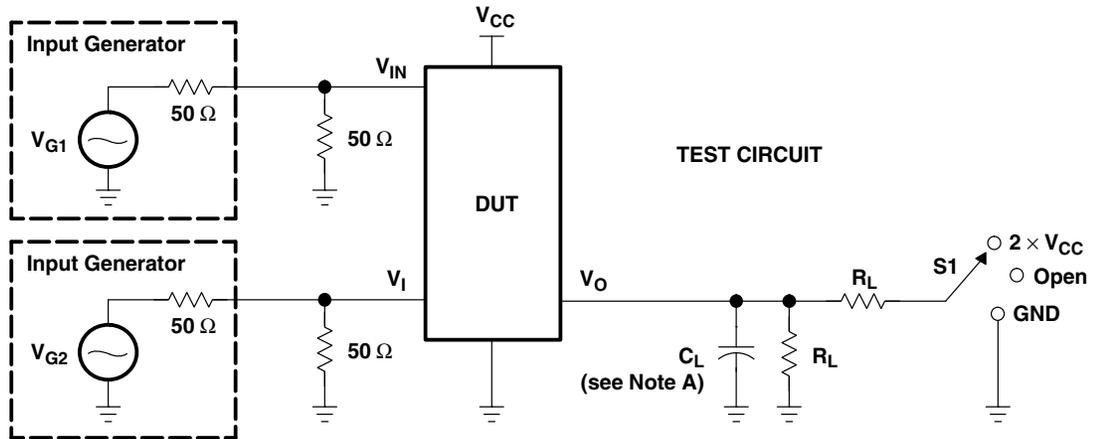


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

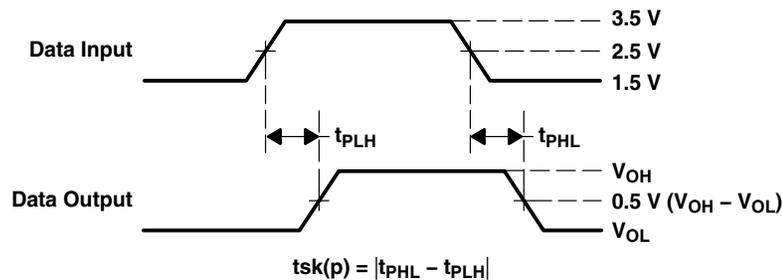
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION
 FOR SKEW**



| TEST | V _{CC} | S1 | R _L | V _{IN} (see Note B) | C _L |
|--------------------|-----------------|-----|----------------|---------------------------------|----------------|
| t _{sk(p)} | 3.3 V ± 0.3 V | GND | 200 Ω | V _{CC} or GND | 10 pF |

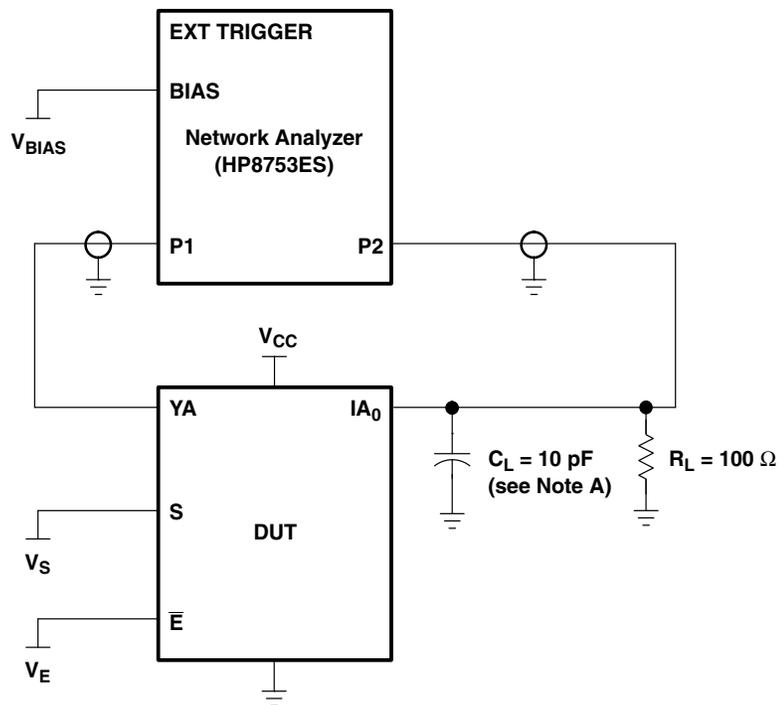


**VOLTAGE WAVEFORMS
 PULSE SKEW (t_{sk(p)})**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Switch is ON during the measurement of t_{sk(p)}, i.e., voltage at $\bar{E} = 0$ and S = V_{CC} or GND

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

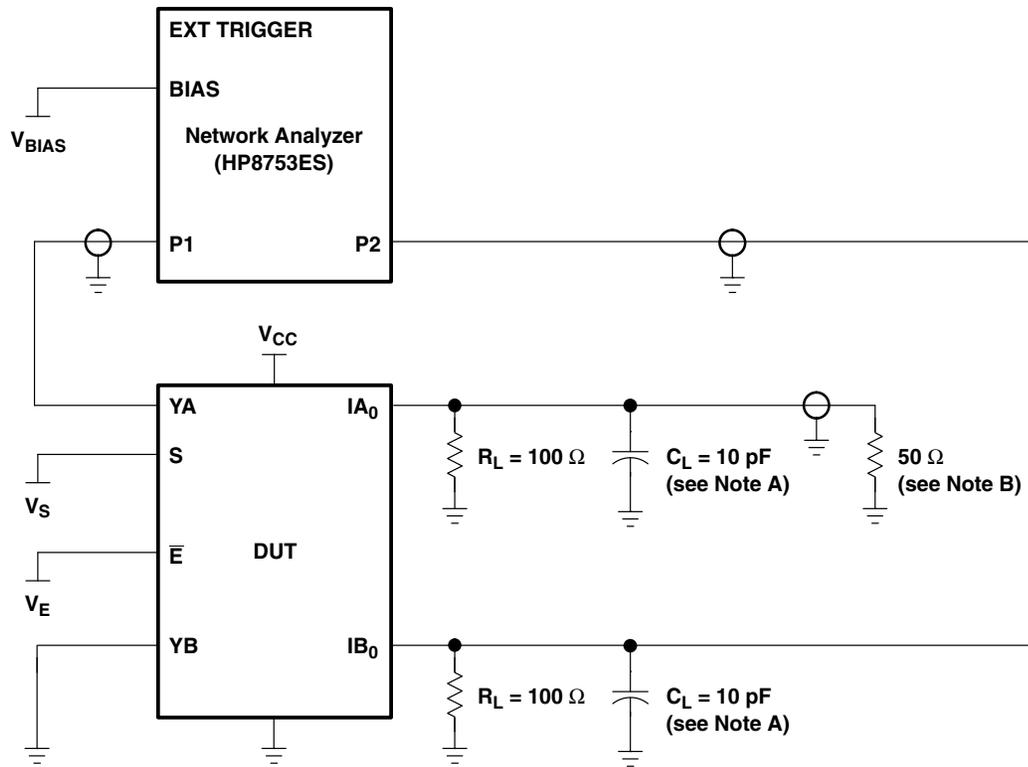
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IA₀. All unused analog I/O ports are left open.

HP8753ES setup

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35 \text{ V}$
- ST = 2 s
- P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

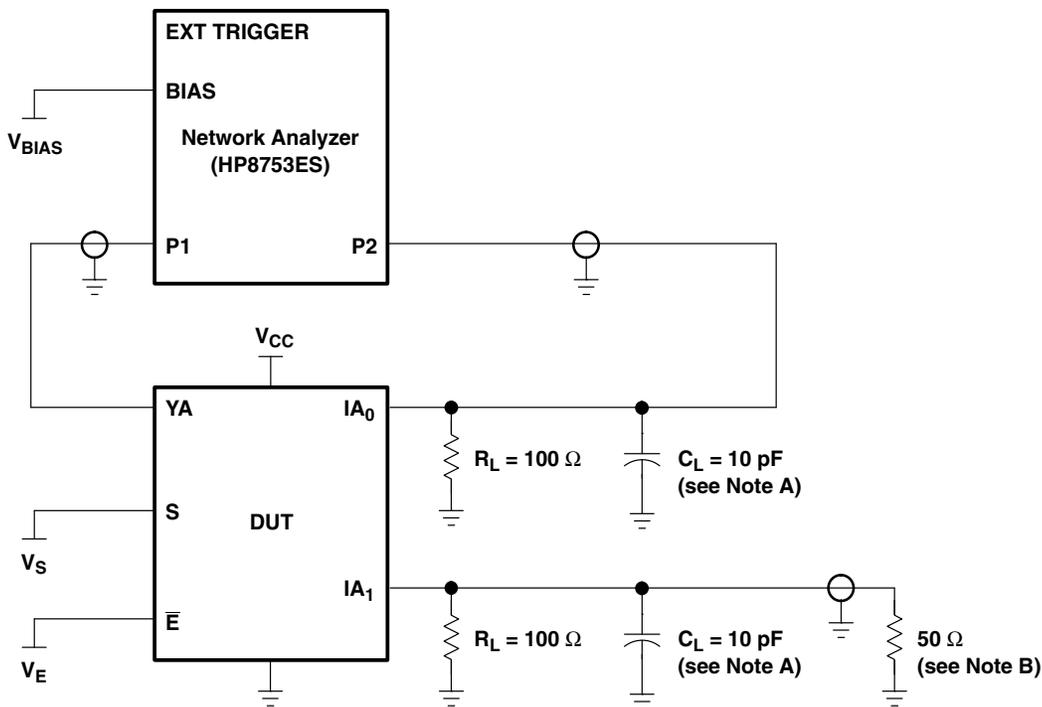
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IB_0 . All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES setup

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35$ V
- ST = 2 s
- P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0 . All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES setup

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35$ V
- ST = 2 s
- P1 = 0 dBm

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TS3L110D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3L110 | Samples |
| TS3L110DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TK110 | Samples |
| TS3L110DBQRE4 | ACTIVE | SSOP | DBQ | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110DBQRG4 | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TK110 | Samples |
| TS3L110DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3L110 | Samples |
| TS3L110DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3L110 | Samples |
| TS3L110DGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |
| TS3L110DGVRE4 | ACTIVE | TVSOP | DGV | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110DGVRG4 | ACTIVE | TVSOP | DGV | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3L110 | Samples |
| TS3L110DRE4 | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110DRG4 | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |
| TS3L110PWE4 | ACTIVE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TS3L110PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |
| TS3L110PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |
| TS3L110PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |
| TS3L110PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TK110 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TS3L110RGYR | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TK110 |  |
| TS3L110RGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TK110 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

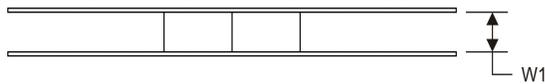
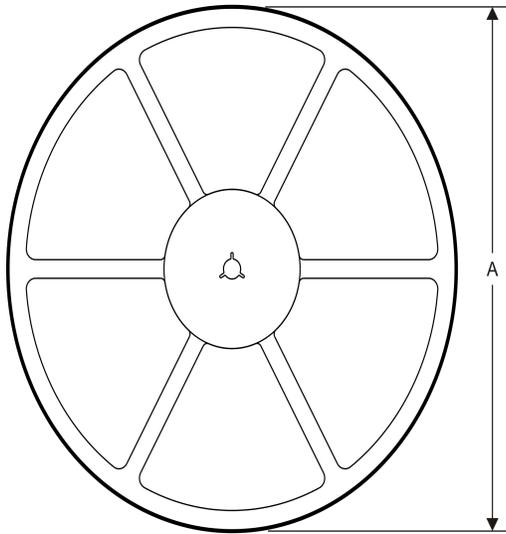
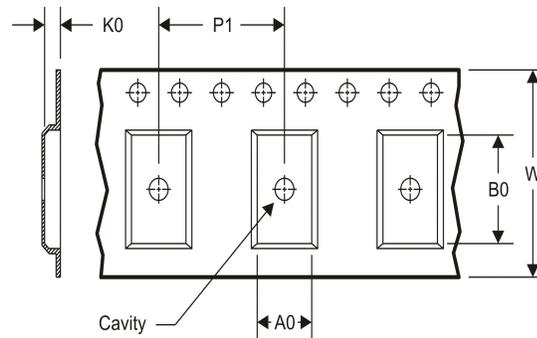
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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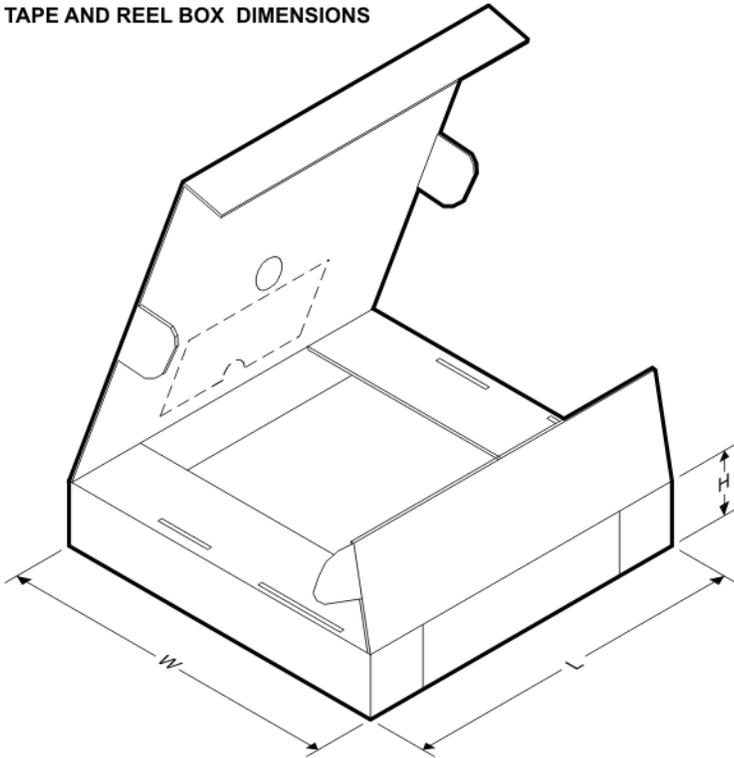
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS3L110DGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| TS3L110DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TS3L110PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TS3L110RGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


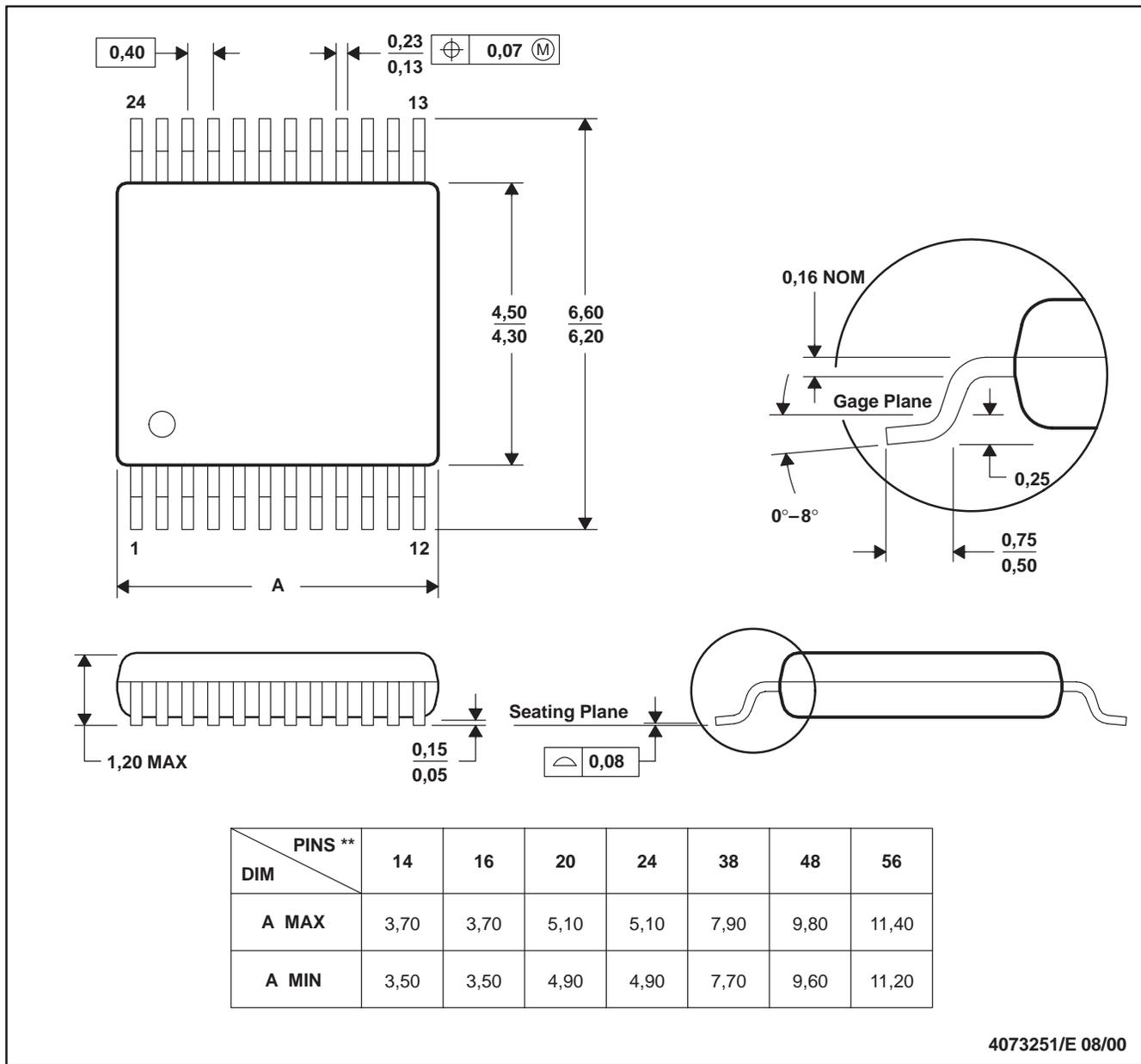
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS3L110DGVR | TVSOP | DGV | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TS3L110DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TS3L110PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TS3L110RGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

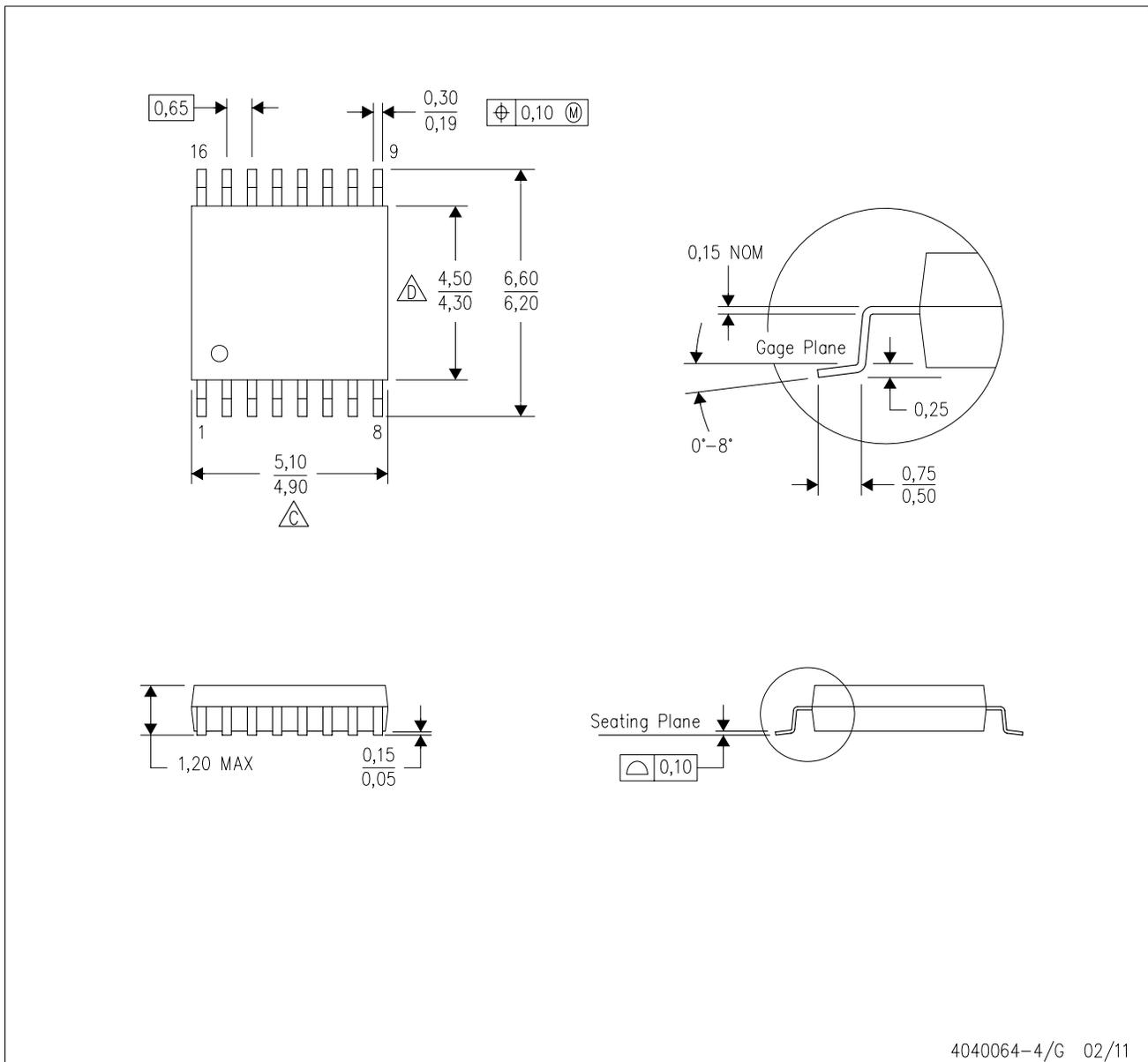
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

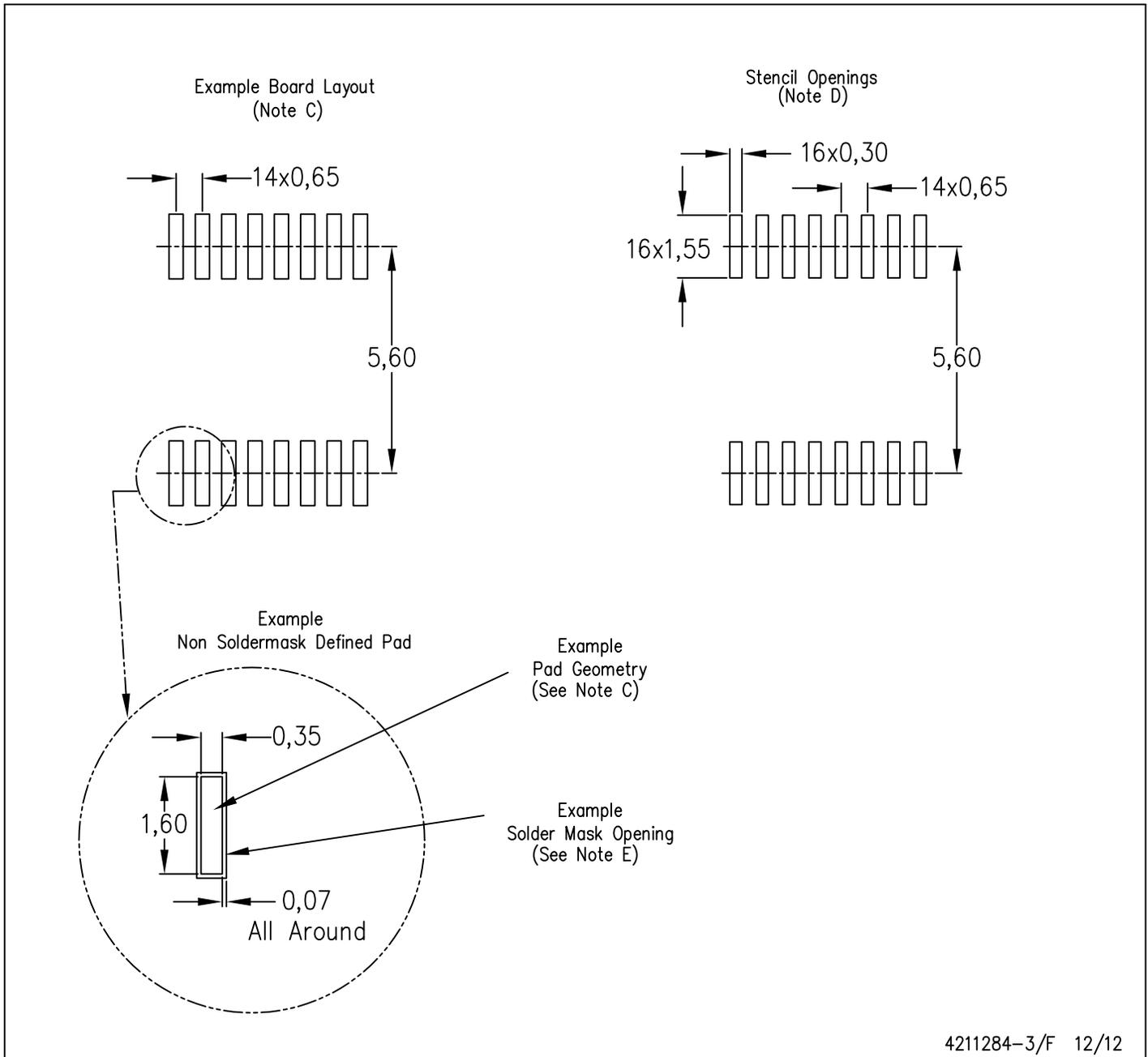


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

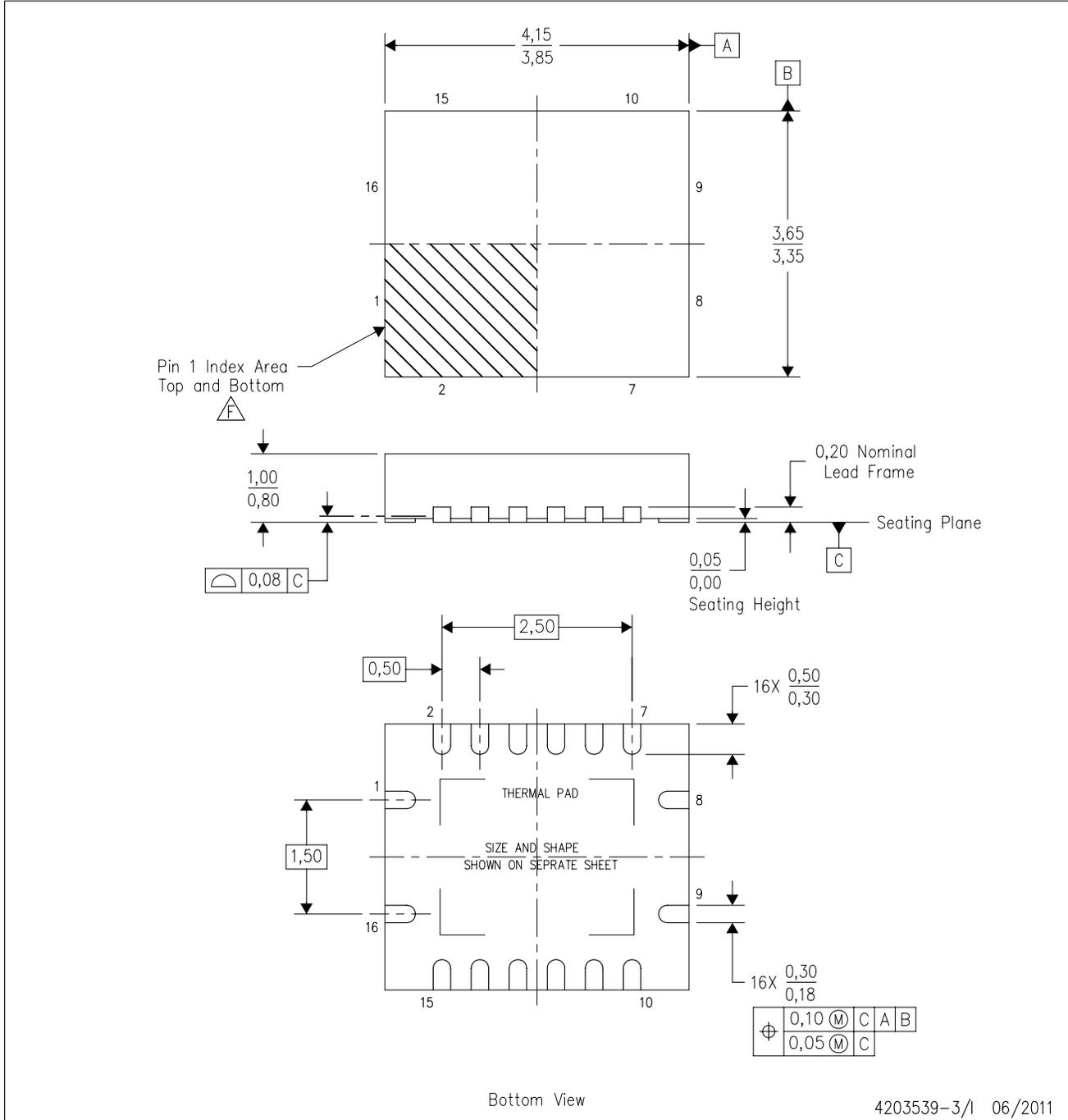
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

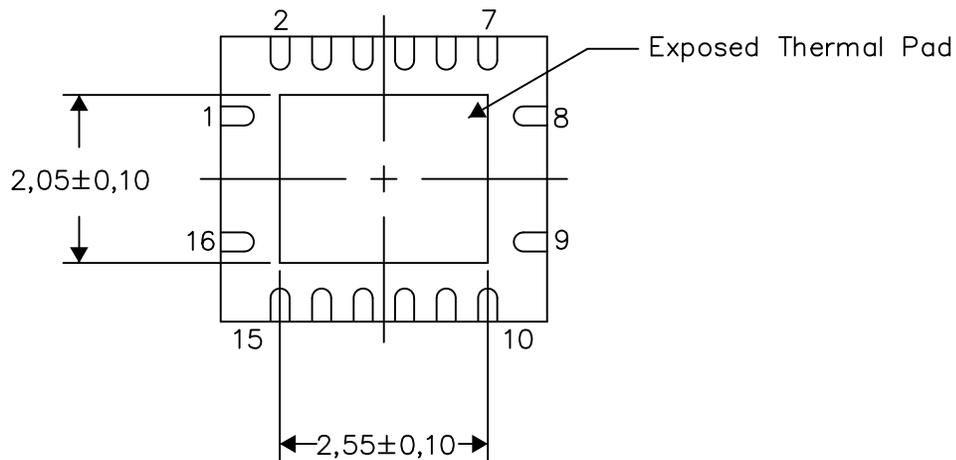
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

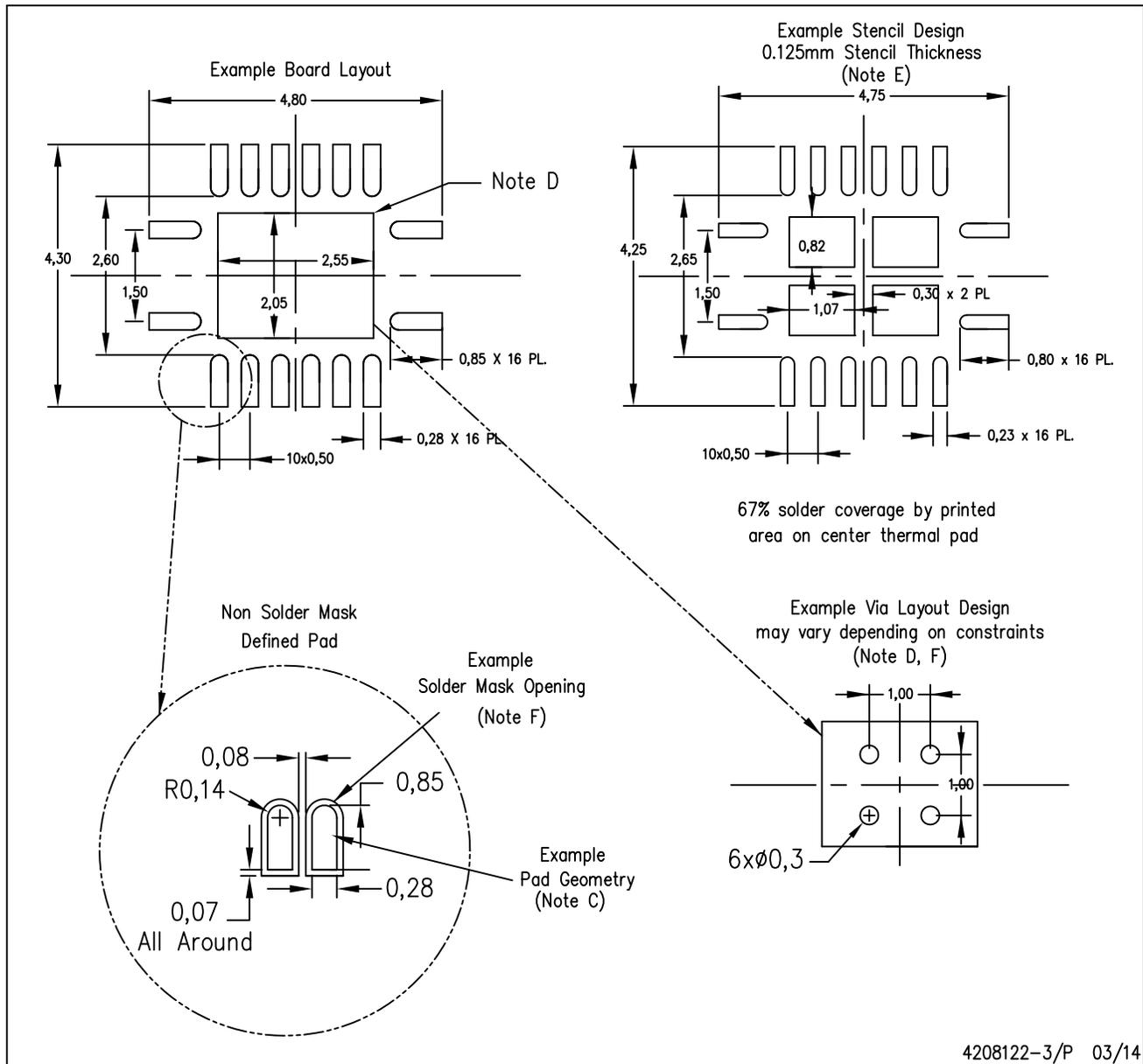
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

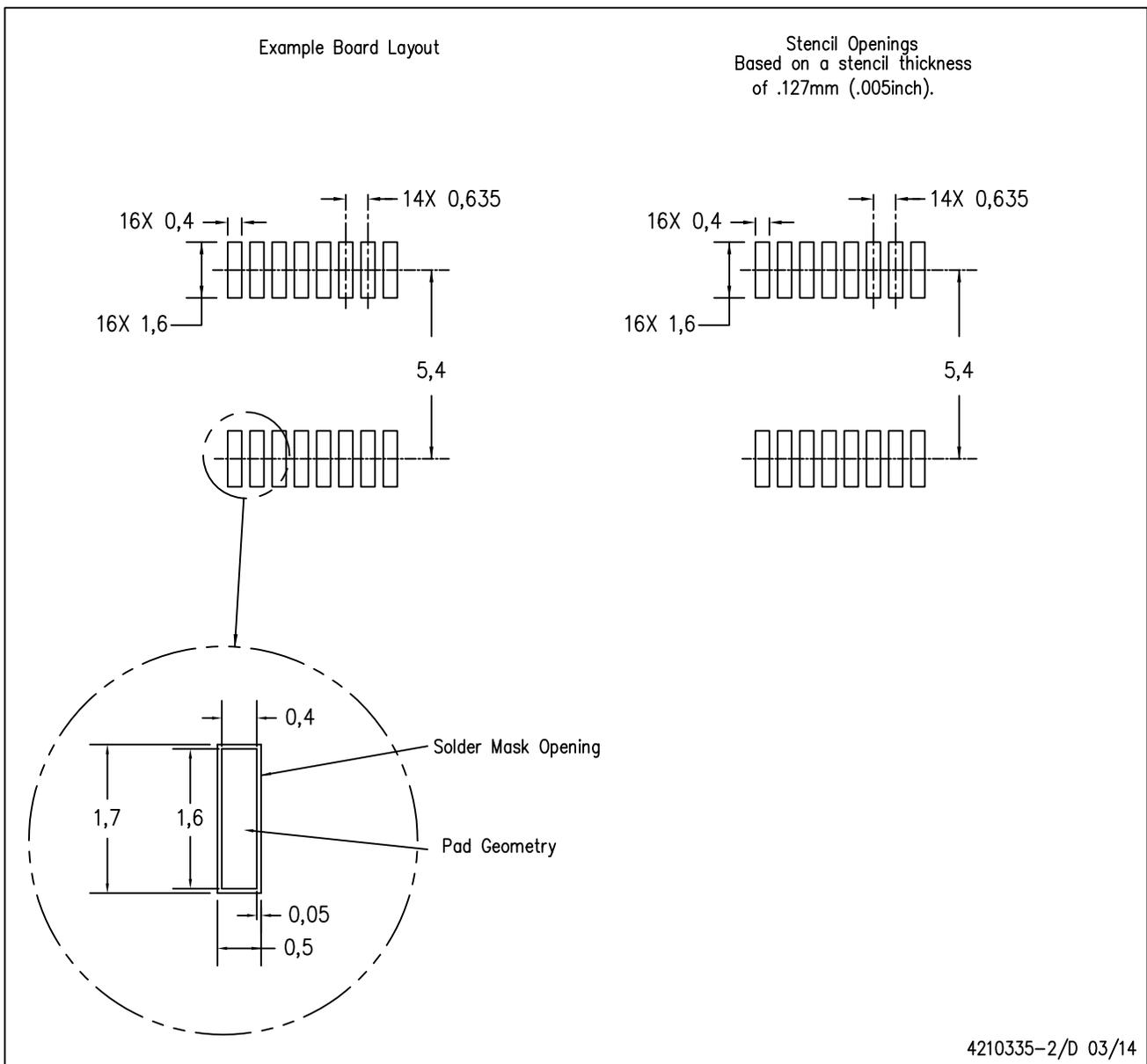


4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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