DUAL POWER DISTRIBUTION SWITCH AND MONOLITHIC SYNCHRONOUS BUCK REGULATOR WITH 5.5-V TO 18-V INPUT VOLTAGE, FIXED 5-V OUTPUT VOLTAGE AND 4-A MAXIMUM CURRENT

Check for Samples: TPS65280

FEATURES

INTEGRATED DUAL POWER DISTRIBUTION SWITCHES

- **Operating Input Voltage Range: 2.5 V to 6 V**
- **Integrated Back-to-Back Power MOSFETs With 80-mΩ On-Resistance**
- **Up to 1-A Maximum Load Current**
- **Current Limiting at Typical 1.2 A (0.8 A,1.6 A or 2 A Available With Manufacture Trim Options)**
- **Latch-off Over Current Protection Versions**
- **Reverse Input-Output Voltage Protection**
- **Built-In Soft-Start**
- **4-kV HBM and 200-V MM ESD Protection at Power Switch Output Pins**
  15-kV ESD Protection per IEC 61000-4-2 With 10-µF External Capacitance
- **Over Temperature Protection**
- **24-Lead QFN (RGE) 4-mm x 4-mm Package**

INTEGRATED BUCK DC/DC CONVERTER

- **Wide Input Voltage Range: 5.5 V to 18 V**
- **Maximum Continuous 4-A Output Load Current**
- **Fixed Output Voltage: 5 V ±1%**
- **Adjustable 300-kHz to 1.4-MHz Switching Frequency**
- **External Clock Synchronization**
- **Adjustable Soft Start and Tracking With Built-In 1-ms Internal Soft-start Time**
- **Cycle-by-Cycle Current Limit**
- **Output Over-voltage Protection**

APPLICATIONS

- **USB Ports and Hubs**
- **Digital TV**
- **Set-Top Boxes**
- **VOIP Phones**
- **Tablet PC**

DESCRIPTION/ORDERING INFORMATION

The TPS65280 incorporates dual N-channel MOSFET power switches for USB power distribution systems that require dual power switches in a single package. It also integrates a buck converter which regulates an accurate 5-V output voltage from a 5.5-V to 18-V power bus to supply the power for power switches. The device is intended to provide a total USB power distribution solution for digital TV, set-top boxes, VOIP phones and tablet PC applications, where precision current limiting is required or heavy capacitive loads or short circuits are encountered.

A dual 85-mΩ independent power distribution switch limits the output current to a typical 1.2 A (manufacture trim 0.8 A, 1.6 A, and 2 A available options) when output current load exceeds the current limit threshold. TPS65280 device limits output current to a safe level by using a constant current mode when output load exceeds the current limit threshold. After delitching time, TPS65280 provides circuit breaker functionality by latching off the power switch during over-current or reverse-voltage situations. Two back-to-back power MOSFETs prevent the current injects from output to input in shutdown. An internal reverse-voltage comparator disables the power switch when the output voltage is driven higher than the input to protect the circuits on the input side of the switch in normal operation. The nFAULT1/2 output asserts low during over-current and reverse-voltage conditions.

The buck DC/DC converter integrates power MOSFETs for optimized power efficiency and reduced external component count for a fixed 5-V output voltage. A wide 5.5-V to 18-V input supply range to buck encompasses most intermediate bus voltages operating off a 9-V, 12-V or 15-V power bus. Constant frequency peak current mode control simplifies the compensation and fast transient response. Equipped with enable and soft-start pins, the DC/DC can be precisely sequenced and ramp up in order to align with other rails in the system. Cycle-by-cycle over-current protection and operating in hiccup mode limit MOSFET power dissipation during buck output short circuit or over loading fault conditions. The switching frequency of the converter can be programmed from 300 kHz to 1.4 MHz with an external resistor at the ROSC pin. With the ROSC pin connecting to the V7V pin, floating, or grounding, a default fixed switching frequency can be selected to reduce the external component. The internal oscillator can be synchronized with a free-run external clock in frequency.

When continuous heavy overload or short circuit increases power dissipation in the buck converter or power switches, the internal thermal protection circuit shuts off both the buck regulator and power switches to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently.

The TPS65280 is available in a 24-lead thermally enhanced QFN (RGE) 4-mm x 4-mm thin package.

ORDERING INFORMATION(1)

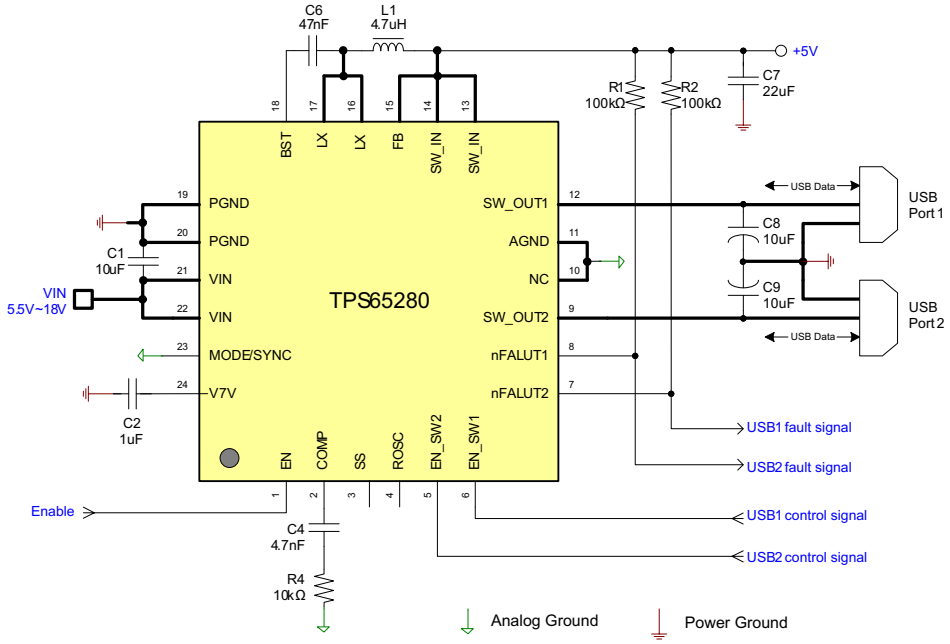
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	24-Pin QFN (RGE)	Reel 3000	TPS65280RGER	TPS65280
		Reel 250	TPS65280RGET	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

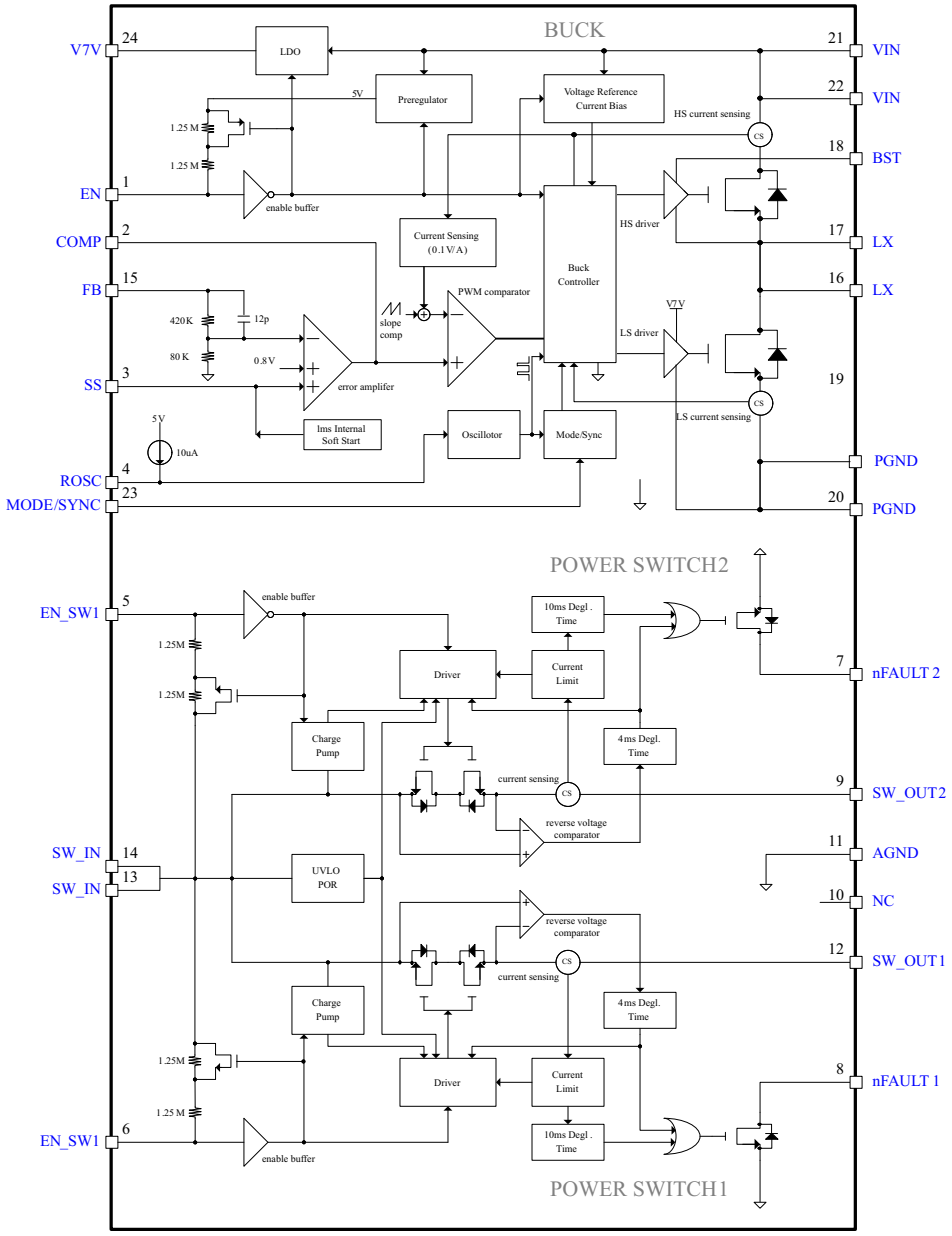
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION

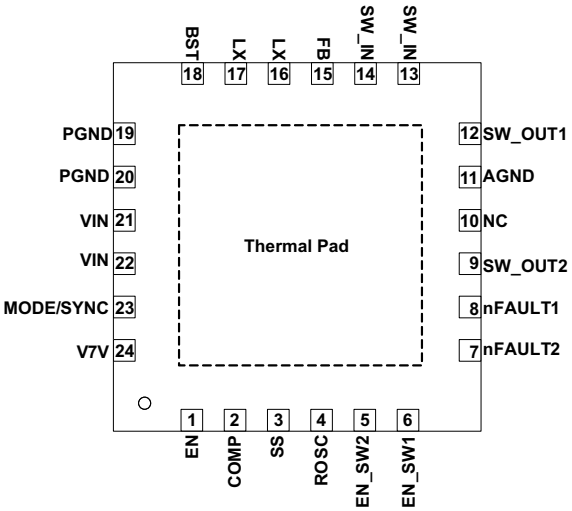


FUNCTION BLOCK DIAGRAM



PIN OUT

RGE PACKAGE
(TOP VIEW)



There is no electric signal down boned to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

TERMINAL FUNCTIONS

NAME	NO.	DESCRIPTION
EN	1	Enable for buck converter. Logic high enables buck converter and bias supply to power switches. Forcing the pin below 0.4 V shuts down the entire device, reducing the quiescent current to approximately 7 µA. There is a 1.25-MΩ pull-up resistor connecting this pin to internal 5-V power rail. Not recommend floating this pin. The device can be automatically started up with connecting EN pin to VIN though a 10-kΩ resistor or connecting a capacitor to program the delay of enabling the device.
COMP	2	Error amplifier output and Loop compensation pin for buck. Connect a series resistor and capacitor to compensate the control loop of buck converter with peak current PWM mode.
SS	3	Soft-start and tracking input for buck converter. An internal 5-µA pull-up current source is connected to this pin. An external soft-start can be programmed by connecting a capacitor between this pin and ground. Leave the pin floating to have a default 1 ms of soft-start time. This pin allows the start-up of buck output to track an external voltage using an external resistor divider at this pin.
ROSC	4	Oscillator clock frequency control pin. Connect the pin to ground for a fixed 300-kHz switching frequency. Connect the pin to V7V or float the pin for a fixed 600-kHz switching frequency. Other switch frequency between 300 kHz to 1.4 MHz can be programmed using a resistor connected from this pin to ground. An internal 10-µA pull-up current develops a voltage to be used in oscillator. Directly adjusting the ROSC pin voltage can linearly adjust switching frequency.
EN_SW2	5	Enable power switch 2. Logic high turns on power switch. Forcing the pin below 0.4 V shuts down power switch. Not recommend floating this pin, though there is a 1.25-MΩ pull-up resistor connecting this pin.
EN_SW1	6	Enable power switch 1. Logic high turns on power switch. Forcing the pin below 0.4 V shuts down power switch. Not recommend floating this pin, though there is a 1.25-MΩ pull-up resistor connecting this pin.
nFAULT2	7	Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 2.
nFAULT1	8	Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 1.
SW_OUT2	9	Power switch 2 output.
NC	10	No connection. Connection to ANGD recommended.
AGND	10, 11	Analog ground common to buck controller and power switch controller. Pin 10 must be routed separately from high current power grounds to the (-) terminal of bypass capacitor of internal V7V LDO output.
SW_OUT1	12	Power switch 1 output.
SW_IN	13, 14	Power switch input voltage. Connect to buck output, or other power supply input.
FB	15	Kelvin sensing pin for +5-V buck output voltage. Connect this pin to the (+) terminal of buck output capacitor. The internal feedback resistor divider (420 kΩ/80 kΩ) in buck converter sets a fixed 5-V ±1% output voltage at room temperature.
LX	16, 17	Switching node connection to the inductor and bootstrap capacitor for buck converter. This pin voltage swings from a diode voltage below the ground up to V^{IN} voltage.
BST	18	Bootstrapped supply to the high side floating gate driver in buck converter. Connect a capacitor (47 nF recommended) from this pin to LX.
PGND	19, 20	Power ground connection. Connect this pin as close as practical to the (-) terminal of input ceramic capacitor.
VIN	21, 22	Input power supply for buck. Connect this pin as close as practical to the (+) terminal of an input ceramic capacitor (10 µF recommended).
MODE/SYNC	23	External synchronization input to internal clock oscillator in forced continuous mode. When an external clock is applied to this pin, the internal oscillator will force the rising edge of clock signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, connecting this pin to ground forces a continuous current mode (CCM) operation of Buck.
V7V	24	Internal low-drop linear regulator (LDO) output. The internal driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum 1-µF ceramic capacitor. The output voltage level of LDO is regulated to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor.
Thermal PAD		Exposed pad beneath the IC. Connect to the power ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to the thermal pad inside the IC package.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	VIN, LX	–0.3 to 18	V
	LX (Maximum withstand voltage transient < 20ns)	–1.0 to 18	V
	BST referenced to LX pin	–0.3 to 7	V
	SW_IN, SW_OUT1, SW_OUT2	–0.3 to 7	V
	EN, EN_SW1, EN_SW2, nFAULT1, nFAULT2, V7V, ROSC, MODE/SYNC	–0.3 to 7	V
	SS, COMP	–0.3 to 3.6	V
	V7, R AGND, PGND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	5.5		18	V
T_A	Ambient temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION(1)

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

(1) SW_OUT1/2 pins' human body model (HBM) ESD protection rating 4 kV, and machine model (MM) rating 200V.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65280 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	38.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	45.3	
θ_{JB}	Junction-to-board thermal resistance(4)	16.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range	VIN1 and VIN2	5.5		18	V
IDD_{SDN}	Shutdown supply current	EN = EN_SW1 = EN_SW2 = low		7	20	µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN = high, EN_SWx = low, FB = 6 V With Buck not switching		0.8		mA
IDD_{Q_SW}	Switching quiescent current with no load at DCDC output, Buck switching	EN = high, EN_SWx = low, FB = 5 V With Buck switching		13		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}	4	4.25	4.50	V
		Falling V_{IN}	3.75	4	4.25	
		Hysteresis		0.25		
V_{7V}	Internal biasing supply	V_{7V} load current = 0 A, V_{IN} = 12 V	6.05	6.25	6.45	V
OSCILLATOR						
f_{SW_BK}	Switching frequency range	Set by external resistor ROSC	300		1400	kHz
f_{SW}	Programmable frequency	ROSC = 51 kΩ		500		kHz
		ROSC = 140 kΩ		1400		
		ROSC floating or connected to V7V	510	600	690	
		ROSC connected to ground	255	300	345	
BUCK CONVERTER						
V_{IN}	Input supply voltage	For a fixed 5-V output	5.5		18	V
V_{OUT}	Regulated +5-V output voltage	V_{COMP} = 1.2 V, T_J = 25°C	4.95	5	5.05	V
		V_{COMP} = 1.2 V, T_J = -40°C to 125°C	4.9	5	5.1	
$V_{LINEREG}$	Line regulation - DC	I_{OUT} = 2 A		0.5		%/V
$V_{LOADREG}$	Load regulation - DC	I_{OUT} = (10% - 90%) x I_{OUT_max}		0.5		%/A
G_{m_EA}	Error amplifier trans-conductance(1)	-2 µA < I_{COMP} < 2 µA		520		µs
G_{m_SRC}	COMP voltage to inductor current Gm(1)	I_{LX} = 0.5 A		10		A/V
V_{ENH}	EN high level input voltage		2			V
V_{ENL}	EN low level input voltage				0.4	V
I_{SS}	Soft-start charging current			4.5		µA
t_{SS_INT}	Internal soft-start time	SS pin floats	0.5	1	1.5	ms
I_{LIMIT}	Buck peak inductor current limit			5.2		A
R_{dson_HS}	On resistance of high side FET in buck	V_{7V} = 6.25 V		80		mΩ
R_{dson_LS}	On resistance of low side FET in buck	V_{IN} = 12 V		50		mΩ
POWER DISTRIBUTION SWITCH						
V_{SW_IN}	Power switch input voltage range		2.5		6	V
V_{UVLO_SW}	Input under-voltage lock out	V_{SW_IN} rising	2.15	2.25	2.35	V
		V_{SW_IN} falling	2.05	2.15	2.25	V
		Hysteresis		100		mV
R_{DSON_SW}	Power switch NDMOS on-resistance	V_{SW_INx} = 5 V, I_{SW_OUT} = 0.5 A, T_J = 25°C, including bond wire resistance		100		mΩ
		V_{SW_Inx} = 2.5 V, I_{SW_OUT} = 0.5 A, T_J = 25°C, includes bond wire resistance		100		
t_{D_on}	Turn-on delay time	V_{SW_IN} = 5 V, C_L = 1 µF, R_L = 100 Ω (see Figure 1)		1.1		ms
t_{D_off}	Turn-off delay time			1.2		ms
t_r	Output rise time			0.6		ms
t_f	Output fall time			0.3		ms
I_{OCP_SW}	Current limit threshold (maximum DC current delivered to load) and short circuit current, SW_OUTx connect to ground		1.05	1.2	1.35	A
t_{IOS}	Response time to short circuit	V_{SW_IN} = 5 V		2		us

(1) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DEGLITCH(OCP)}$	Switch over current fault deglitch	Fault assertion or de-assertion due to over-current condition	7	10	13	ms
V_{L_nFAULT}	nFAULTx pin output low voltage	$I_{nFAULTx}$ = 1 mA		150		mV
V_{EN_SWH}	EN_SWx high level input voltage	EN_SW1, EN_SW2	2			V
V_{EN_SWL}	EN_SWx high level input voltage	EN_SW1, EN_SW2			0.4	V
R_{DIS}	Discharge resistance	V_{SW_IN} = 5 V, EN_SW1/EN_SW2 = 0 V		100		Ω
THERMAL SHUTDOWN						
T_{TRIP_BUCK}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST_BUCK}	Thermal protection hysteresis			20		°C

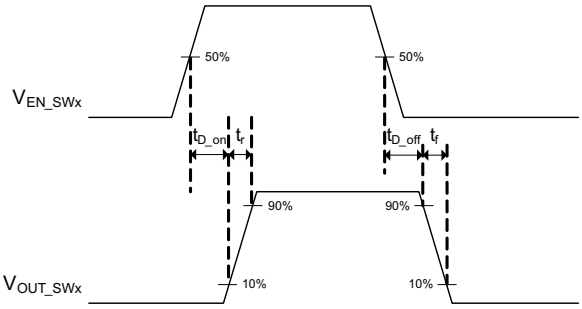


Figure 1. Power Switches Test Circuit and Voltage Waveforms

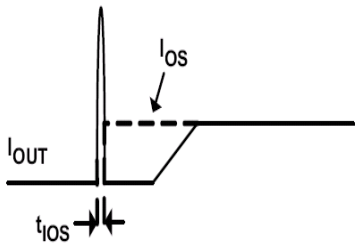


Figure 2. Response Time to Short Circuit Waveform

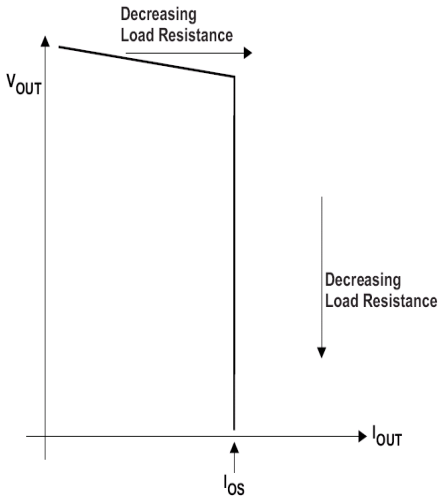


Figure 3. Output Voltage vs Current Limit Threshold

TYPICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

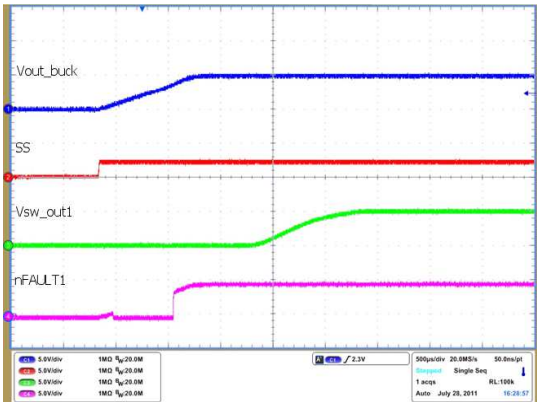


Figure 4. Buck Start Up by EN Pin With Internal Soft-Start (SS Pin Open)

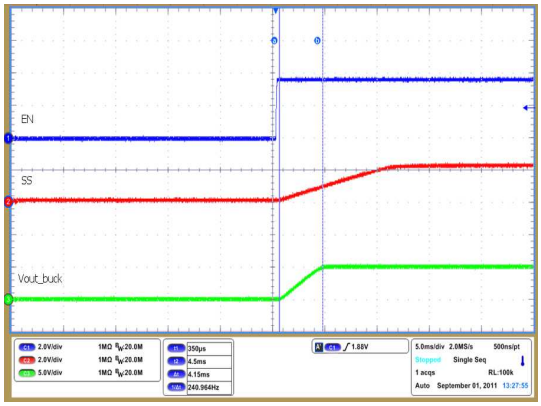


Figure 5. Buck Start Up by EN Pin With an External 22-nF SS Capacitor

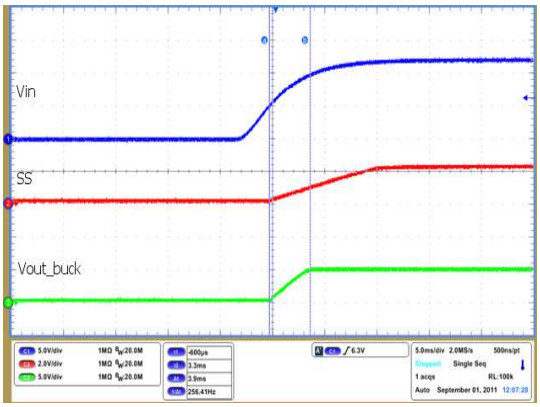


Figure 6. Ramp V_{IN} to Start Up Buck With an External 22-nF SS Capacitor

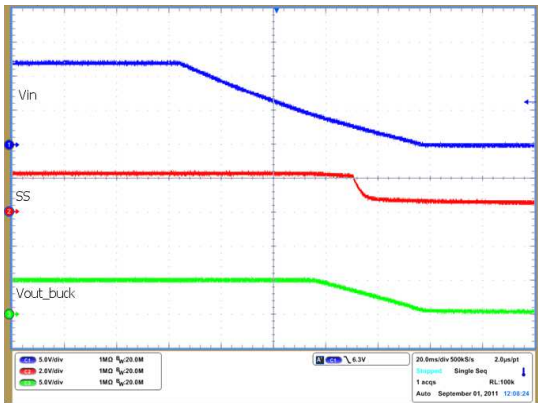


Figure 7. Ramp V_{IN} to Power Down With an External 22-nF SS Capacitor

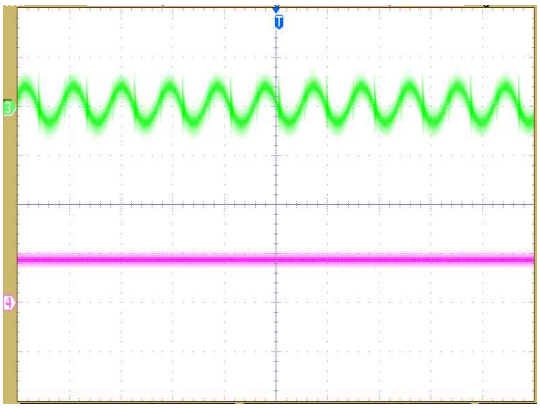


Figure 8. Buck Output Voltage Ripple (Chan3: V_{OUT}, 10 mV/DIV; Chan4: I_O, 2A/DIV; Time: 2 µs/DIV)

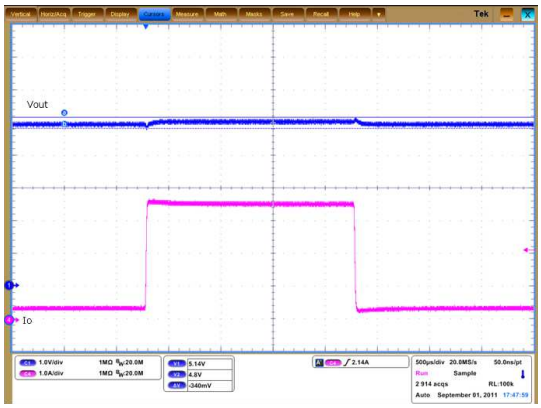


Figure 9. Buck Output Load Transient

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

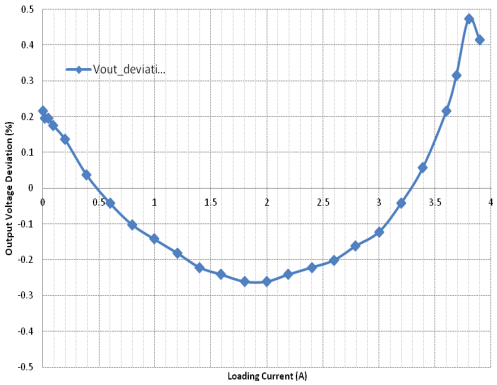


Figure 10. Buck Load Regulation

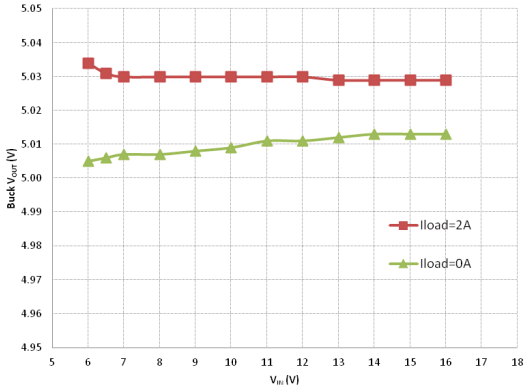


Figure 11. Buck Line Regulation

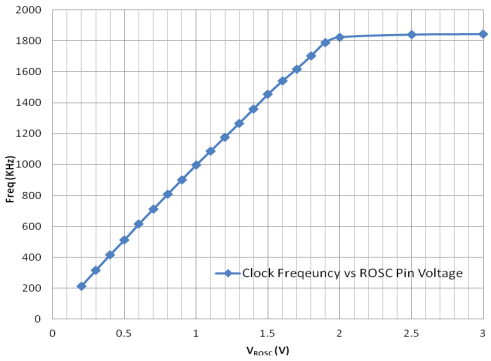


Figure 12. Oscillator Frequency vs Rosc Voltage (Note that Select ROSC Resistance = VROSC x 100 kΩ for Desired Frequency)

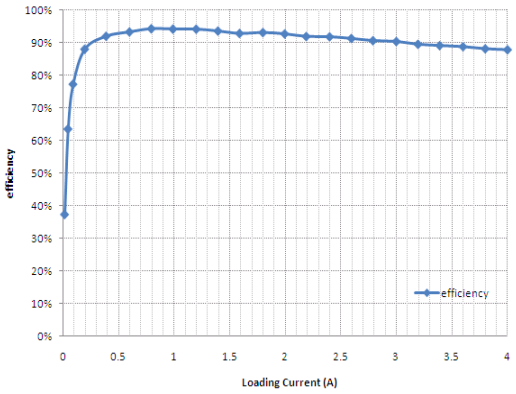


Figure 13. Buck Efficiency

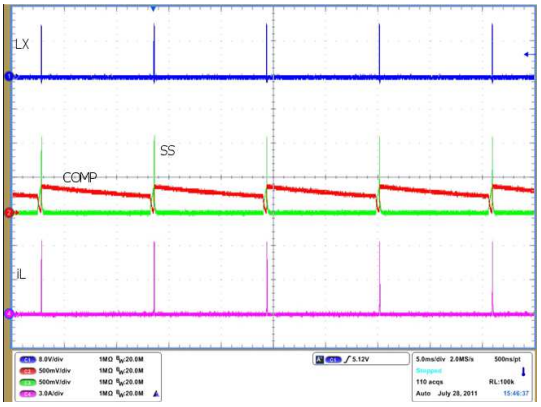


Figure 14. Buck Hiccup Response to Hard-Short Circuit

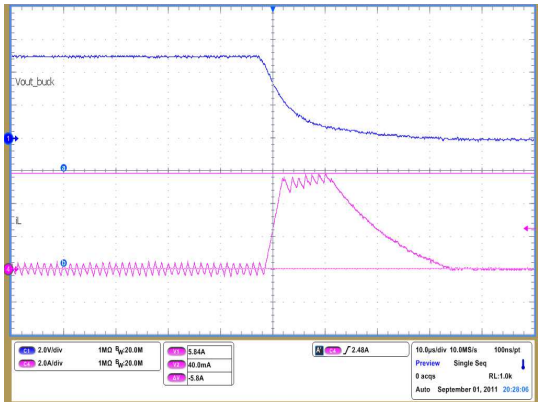


Figure 15. Zoom In Buck Output Hard Short Response

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

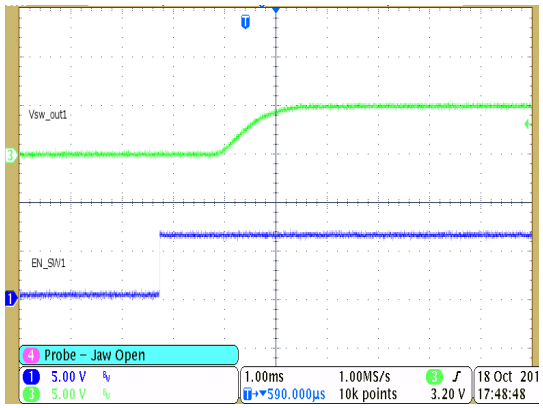


Figure 16. Power Switch 1 Turn On Delay and Rise Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

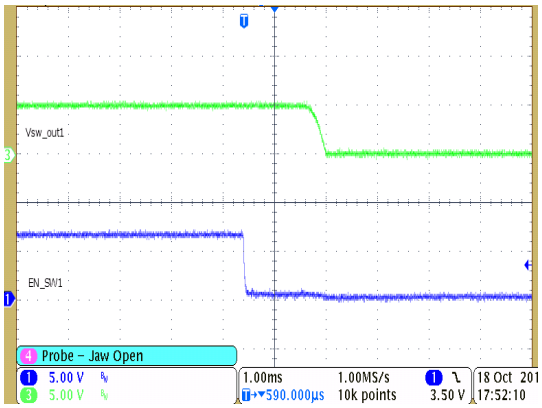


Figure 17. Power Switch 1 Turn Off Delay and Fall Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

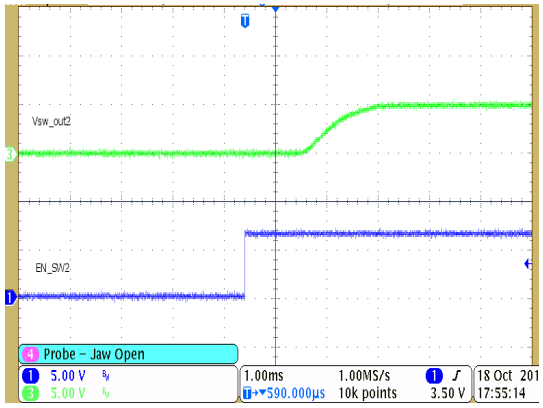


Figure 18. Power Switch 2 Turn On Delay and Rise Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

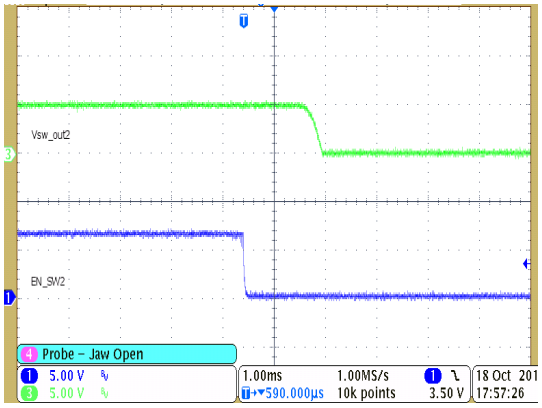


Figure 19. Power Switch 2 Turn Off Delay and Fall Time
R_{OUT} = 5 Ω, C_{OUT} = 22 µF

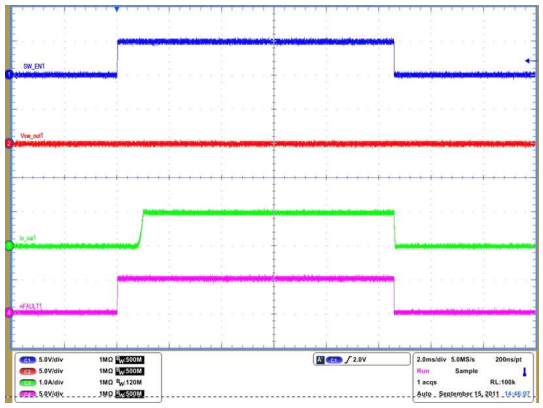


Figure 20. Power Switch 1 Enable Into Short Circuit

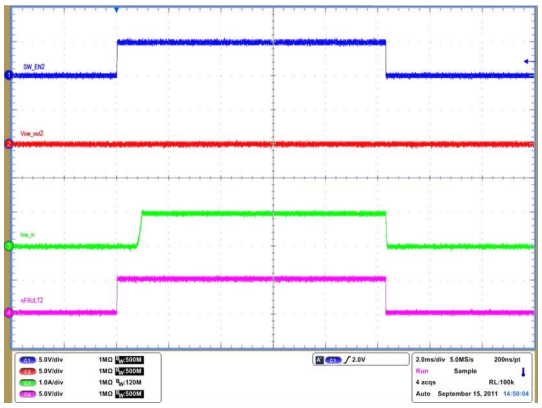


Figure 21. Power Switch 2 Enable Into Short Circuit

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

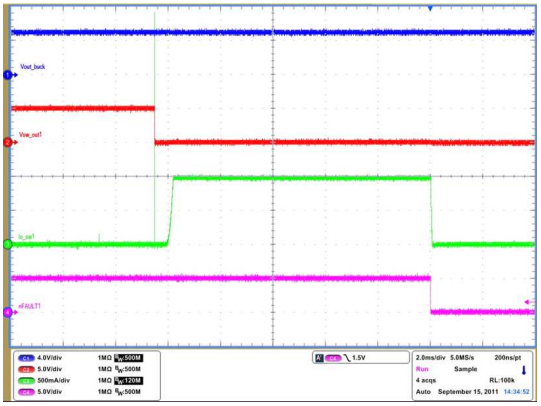


Figure 22. Power Switch 1 No Load to Short-Circuit Transient Response

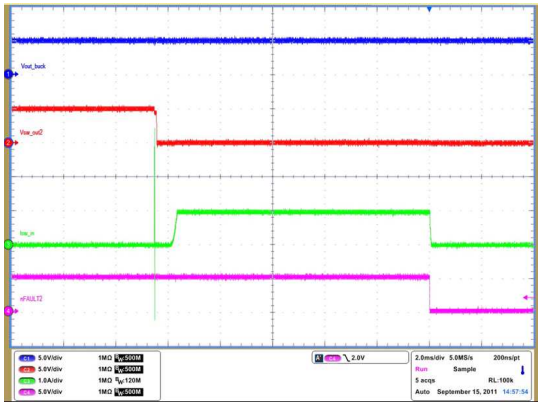


Figure 23. Power Switch 2 No Load to Short-Circuit Transient Response

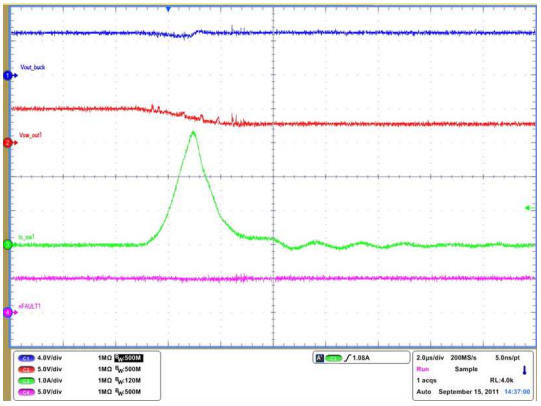


Figure 24. . Power Switch Reponses Time (T_{IOS}) to Output Hard Short

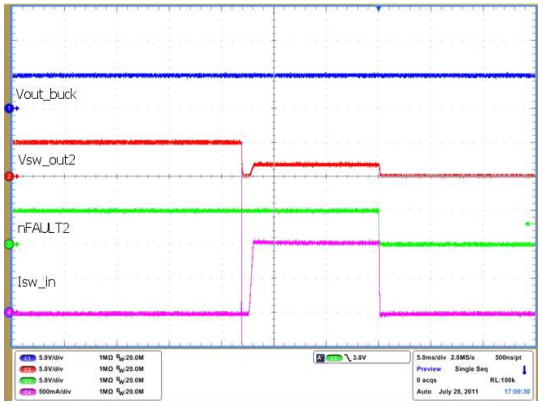


Figure 25. Power Switch No Load to 1-Ω Transient Response

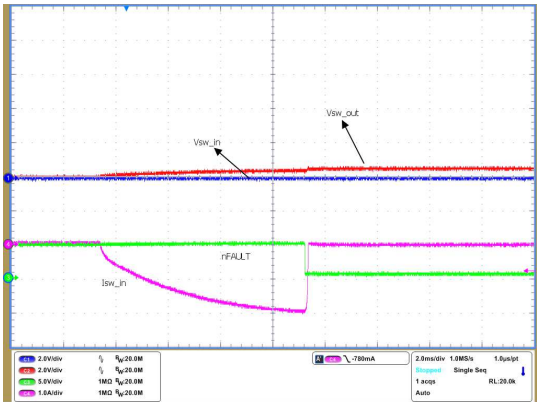


Figure 26. Power Switch Reverse Voltage Protection Response

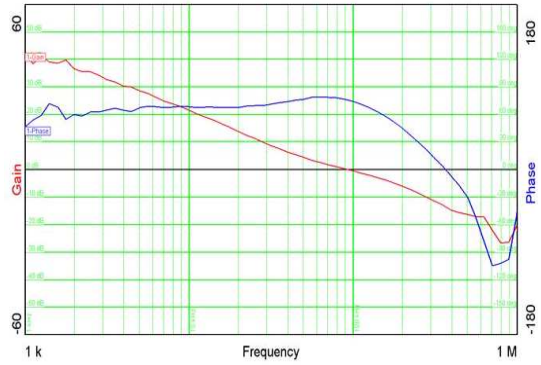


Figure 27. Bode Plot
V_{IN} = 12 V, V_{out_buck} = 5 V/0.5 A, I_{sw1} = I_{sw2} = 0.8 A

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

Figure 28. Loop Stability Bode Plot V_{IN} = 12 V, Buck Loads 0.5 A, Power Switch 1 and 2 Have No Load

Figure 29. Loop Stability Bode Plot V_{IN} = 12 V, Buck Load 0.5 A, Power Switch 1 and 2 Load 0.8 A Each

OVERVIEW

TPS65280 PMIC integrates two independent current-limited, power distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide up to 1-A of continuous load current. Additional device features include over temperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from the input voltage of power switches as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of output voltage to limit large current and voltage surges and provides built-in soft-start functionality. TPS65280 device limits output current to a safe level when the output load exceeds the current limit threshold. After deglitching time, device latches off when the load exceeds the current limit threshold. The device asserts the nFAULT1/2 signal during the over current or reverse voltage faulty condition.

TPS65280 PMIC also integrates a synchronous step-down converter with a fixed 5-V output voltage to provide the power for power switches in the USB ports. The synchronous buck converter incorporates an 80-mΩ high side power MOSFET and 50-mΩ low side power MOSFET to achieve high efficiency power conversion. The converter supports an input voltage range from 5.5 V to 18 V for a fixed 5-V output. The converter operates in continuous conduction mode with peak current mode control for simplified loop compensation. The switching clock frequency can be programmed from 300 kHz to 1.4 MHz from the ROSC pin connection. The peak inductor current limit threshold is internally set at 5 A. The soft-start time can be adjusted with connecting an external capacitor at the SS pin, or fixed at 1 ms with floating at the SS pin.

POWER SWITCH DETAILED DESCRIPTION

Over Current Condition

The TPS65280 responds to over-current conditions on power switches by limiting the output currents to the I_{OCP_SW} level, which is fixed internally. The load current is less than the current-limit threshold and the device does not limit current. During normal operation the N-channel MOSFET is fully enhanced, and $V_{SW\_OUT} = V_{SW\_IN} - (I_{SW\_OUT} \times R_{dson\_SW})$. The voltage drop across the MOSFET is relatively small compared to V_{SW_IN}, and $V_{SW\_OUT} \approx V_{SW\_IN}$. When an over current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. During current-limit operation, the N-channel MOSFET is no longer fully enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{SW\_IN} \neq V_{SW\_OUT}$), and V_{SW_OUT} decreases. The amount that V_{SW_OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{SW_OUT} can be calculated by $I_{OCP\_SW} \times R_{LOAD}$, where I_{OCP_SW} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition.

The manufacture trim options are available for the current limiting thresholds at 0.8 A, 1.2 A, 1.6 A and 2 A.

Three possible overload conditions can occur as summarized in Table 1.

Table 1. Possible Overload Conditions

CONDITIONS	BEHAVIORS
Short circuit or partial short circuit present when the device is powered up or enabled	The output voltage is held near zero potential with respect to ground and the TPS65280 ramps output current to I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.
Gradually increasing load (<100 A/s) from normal operating current to I_{OCP_SW}	The current rises until current limit. Once the threshold has been reached, the device switches into its current limiting at I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.
Short circuit, partial short circuit or fast transient overload occurs while the device is enabled and powered on	The device responds to the over-current condition within time t_{IOS} (see Figure 3).The current sensing amplifier is overdriven during this time, and needs time for loop response. Once t_{IOS} has passed, the current sensing amplifier recovers and limits the current to I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.

Reverse Current and Voltage Protection

A power switch in the TPS65280 incorporates two back-to-back N-channel power MOSFETs as to prevent the reverse current flowing back the input through body diode of MOSFET when power switches are off.

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typical) for 4 ms (typical). This prevents damage to devices on the input side of the TPS65280 by preventing significant current from sinking into the input capacitance of power switch or buck output capacitance. The TPS65280 device keeps the power switch turned off even if the reverse-voltage condition is removed and do not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the nFAULT1/2 output (active-low) after 4 ms.

nFAULT1/2 Response

The nFAULT1/nFAULT2 open-drain output is asserted (active low) during an over current, over temperature or reverse-voltage condition. The TPS65280 asserts the nFAULT signal during a fault condition and remains asserted while the part is latched-off. The nFAULT signal is de-asserted once device power is cycled or the enable is toggled and the device resumes normal operation. The TPS65280 is designed to eliminate false nFAULT reporting by using an internal delay deglitch circuit for over current (10 ms typical) and reverse-voltage (4 ms typical) conditions without the need for external circuitry. This ensures that nFAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Deglitching circuitry delays entering and leaving fault conditions. Over temperature conditions are not deglitched and assert the FAULT signal immediately.

Under-Voltage Lockup (UVLO)

The under-voltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

Enable and Output Discharge

The logic enable EN_SW1/EN_SW2 controls the power switch, bias for the charge pump, driver, and other circuits. The supply current from power switch driver is reduced to less than 1 µA when a logic low is present on EN_SW1/2. A logic high input on EN_SW1/EN_SW2 enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

When enable is de-asserted, the discharge function is active. The output capacitor of power switch is discharged through an internal NMOS that has a discharge resistance of 100 Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

Power Switch Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. It is recommended to place the output capacitor in the buck converter between SW_IN and AGND as close to the device as possible for local noise de-coupling. Additional capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the input of power switches in the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

UNIVERSAL SERIAL BUS (USB) POWER-DISTRIBUTION REQUIREMENTS

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold.

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS65280 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

Self-Powered and Bus-Powered HUBs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V and 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

USB Power Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

SPHs must:

- Current limit downstream ports
- Report over-current conditions

BPHs must:

- Enable/disable power to downstream ports
- Power up at < 100 mA
- Limit inrush current (< 44 Ω and 10 µF)

Functions must:

- Limit inrush currents
- Power up at < 100 mA

The feature set of the TPS65280 meets each of these requirements. The integrated current limiting and over-current reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

BUCK DC/DC CONVERTER DETAILED DESCRIPTION

Output Voltage

The TPS65280 regulates a fixed +5-V output voltage set by an internal feedback resistor divider as shown in Figure 30. Pin 15 is a Kelvin sensing feedback of output voltage. This pin should be directly connected to (+) terminal of output capacitor. Great care should be taken to route the FB line away from noise sources, such as the inductor or the LX switching node line.

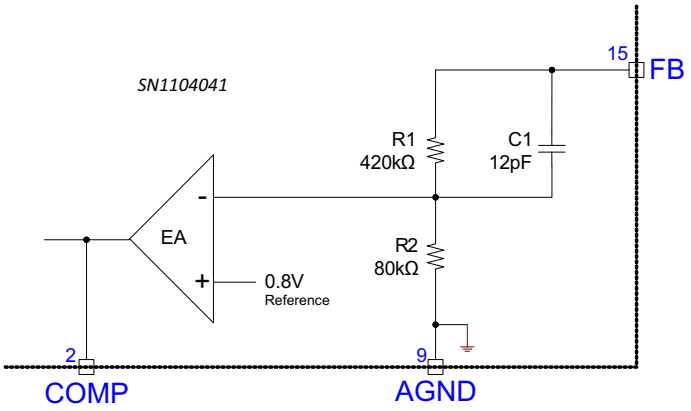


Figure 30. Buck Internal Feedback Resistor Divider

Switching Frequency Selection and Clock Synchronization

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and capacitance to maintain low output ripple voltage. The switching frequency of the TPS65280 buck controller can be selected with the connection at ROSC pin. The ROSC pin can be connected to AGND, tied to V7V, open or programmed through an external resistor. Tying ROSC pin to AGND selects 300 kHz, while tying ROSC ping to V7V or floating ROSC pin selects 600 kHz. Placing a resistor between ROSC and AGND allows the buck switching frequency to be programmed between 300 kHz to 1.4 MHz, as shown in Figure 12. The programmed clock frequency by an external resistor can be calculated with the following equation:

$$f_{SW} = 10 \times R_{OSC} \quad (1)$$

An external clock source can be connected to the MODE/SYNC pin. The internal oscillator synchronizes the internal clock and rising edge of the on, high side power MOSFET to the rising edge of the synchronized external clock signal. When not using clock synchronization, always connect MODE/SYNC pin to ground.

Soft-Start Time

The start-up of buck output is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.8-V reference, the TPS65280 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.8 V. The SS pin can be used to program an external soft-start function or to allow output of the buck to track another supply during start-up. The device has an internal pull-up current source of 4.5 µA that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The SN1104041 will regulate the internal feedback voltage (and hence 5-V output of buck) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from 0 V to its final regulated 5 V value. The total soft-start time will be approximately:

$$Tss = Css \cdot \left(\frac{0.8 \cdot V}{4.5 \cdot \mu A} \right) \quad (2)$$

Internal V7V Regulator

The TPS65280 features an internal P-channel low dropout linear regulator (LDO) that supplies power at the V7V pin from the VIN supply. V7V powers the gate drivers and much of the TPS65280's internal circuitry. The LDO regulates V7V to 6.3 V of over drive voltage on the power MOSFET for the best efficiency performance. The LDO can supply a peak current of 50 mA and must be bypassed to ground with a minimum 1-µF ceramic capacitor. The capacitor placed directly adjacent to the V7V and PGND pins is highly recommended to supply the high transient currents required by the MOSFET gate drivers.

Short Circuit Protection

During the PWM on-time, the current through the internal high side switching MOSFET is sampled. The sampled current is compared to a nominal 5-A over-current limit. If the sampled current exceeds the over-current limit reference level, an internal over-current fault counter is set to 1 and an internal flag is set. Both internal high side and low side power MOSFETs are immediately turned off and will not be turned on again until the next switching cycle. If the over-current condition persists for eight sequential clock cycles, the over-current fault counter overflows indicating an over-current fault condition exists. The buck regulator is shut down and stays turned off for 10 ms. If the over-current condition clears prior to the counter reaching eight consecutive cycles, the internal flag and counter are reset. The protection circuitry attempts to recover from the over-current condition after 10-ms power down time. The internal over-current flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the over-current fault condition has cleared. If the over-current fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

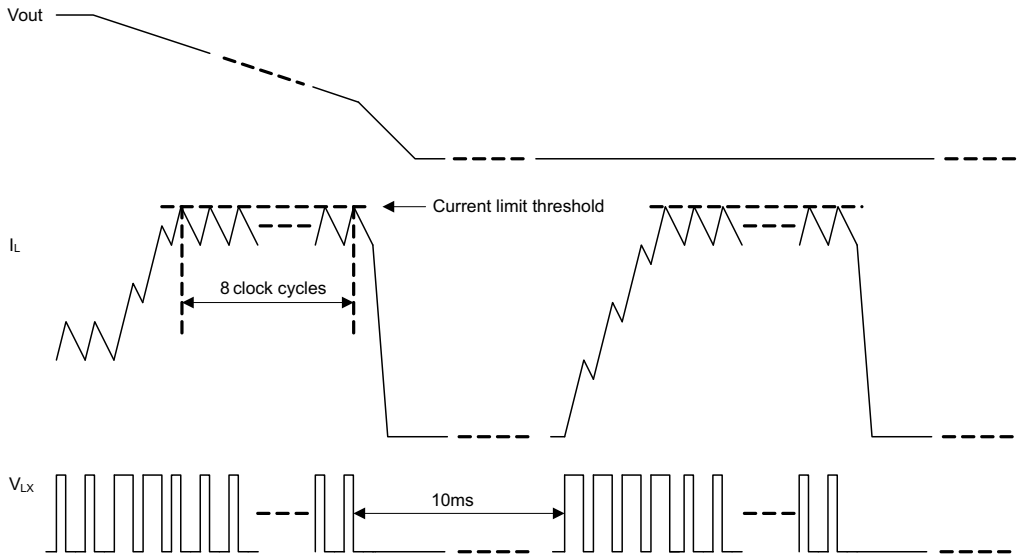


Figure 31. DC/DC Over-Current Protection

Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current, i_L, decreases with higher inductance or higher frequency and increases with higher input voltage, V_{IN}. Accepting larger values of i_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

Use Equation 3 to calculate the value of the output inductor. LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. It is suggested to use 0.1 ~ 0.3 for most LIR applications.

Actual core loss of the inductor is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from Equation 5 and Equation 6.

$$L = \frac{V_{in} - V_{out}}{I_O \cdot LIR} \cdot \frac{V_{out}}{V_{in} \cdot fsw} \quad (3)$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{I_O} \cdot \frac{V_{out}}{V_{in} \cdot fsw} \quad (4)$$

$$i_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \cdot (V_{inmax} - V_{out})}{V_{inmax} \cdot L \cdot fsw}\right)^2}{12}} \quad (5)$$

$$I_{Lpeak} = I_O^2 \cdot \frac{\Delta i_L}{2} \quad (6)$$

For this design example, use LIR = 0.3, and the inductor is calculated to be 5.40 µH with V_{IN} = 12 V. Choose a 4.7 µH standard inductor, the peak to peak inductor ripple is about 34% of 3-A DC load current.

Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 7 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 3 A – 0.0 A = 3 A and ΔV_{OUT} = 500 mV (10% of regulated 5 V). Using these numbers gives a minimum capacitance of 17 µF. A standard 22 µF ceramic capacitor is used in the design.

$$Co > \frac{\Delta I_{OUT}{}^2 \cdot L}{V_{out} \cdot \Delta V_{out}} \quad (7)$$

The selection of C_{OUT} is driven by the effective series resistance (ESR). Equation 8 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, ΔV_{OUT} is the maximum allowable output voltage ripple, and Δi_L is the inductor ripple current. In this case, the maximum output voltage ripple is 50 mV (1% of regulated 5 V). From Equation 4, the output current ripple is 1 A. From Equation 8, the minimum output capacitance meeting the output voltage ripple requirement is 4.6 µF with 3-mΩ esr resistance.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{\Delta V_{out}}{\Delta i_L} - esr} \quad (8)$$

After considering both requirements, for this example, one 22 µF 6.3 V X7R ceramic capacitor with 3 mΩ of ESR will be used.

Input Capacitor Selection

A minimum 10 µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters, as they handle the RMS ripple current shown in Equation 9. For this example, I_{OUT} = 2 A, V_{OUT} = 5 V, minimum V_{in_min} = 9.6 V. Tthe input capacitors must support a ripple current of 1 A RMS.

$$I_{inrms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{inmin}} \cdot \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (9)$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, I_{out_max} = 2 A, C_{IN} = 10 µF, f_{SW} = 600 kHz, yields an input voltage ripple of 83 mV.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{sw}} \quad (10)$$

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

Output Capacitor Selection

The external bootstrap capacitor connected to the BST pins supply the gate drive voltages for the topside MOSFETs. The capacitor between BST pin and LX pin is charged through an internal diode from V7V when the LX pin is low. When high side MOSFETs are to be turned on, the driver places the bootstrap voltage across the gate-source of the desired MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, LX, rises to VIN and the BST pin follows. With the internal high side MOSFET on, the bootstrap voltage is above the input supply: $V_{BST} = V_{IN} + V_{7V}$. The selection on bootstrap capacitance is related with internal high side power MOSFET gate capacitance. A 0.047-µF ceramic capacitor is recommended to be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

Loop Compensation

The integrated buck DC/DC converter in TPS65280 incorporates a peak current mode. The error amplifier is a trans-conductance amplifier with a gain of 350 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow these steps:

1. Select switching frequency, f_{SW}, that is appropriate for application depending on L and C sizes, output ripple and EMI. Switching frequency between 500 kHz and 1 MHz gives the best trade off between performance and cost. To optimize efficiency, a lower switching frequency is desired.
2. Set up cross over frequency, fc, which is typically between 1/5 and 1/20 of f_{SW}.
3. RC can be determined by:

   $$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}} \quad (11)$$

   where gm is the error amplifier gain (350 µA/V) and gm_{ps} is the power stage voltage to current conversion gain (10 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole, $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$.

   $$C_C = \frac{R_L \cdot Co}{R_C} \quad (12)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

   $$C_b = \frac{Resr \cdot Co}{R_C} \quad (13)$$

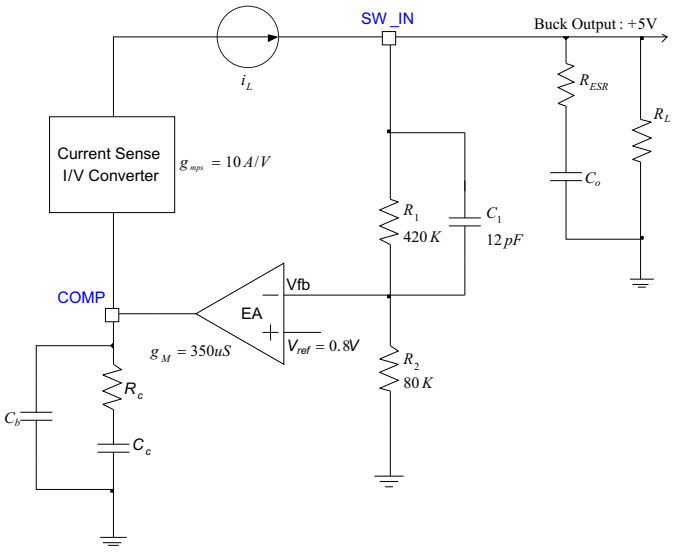


Figure 32. DC/DC Loop Compensation

APPLICATION INORMATION

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the buck converter to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Power Dissipation and Junction Temperature

The total power dissipation inside TPS65280 should not exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package, θ_{JA}, and ambient temperature. The analysis below gives an approximation in calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

To calculate the temperature inside the device under continuous load, use the following procedure.

1. Define the total continuous current through the buck converter (including the load current through power switches). Make sure the continuous current does not exceed the maximum load current requirement.
2. From the graphs below, determine the expected losses (Y axis) in Watts for the buck converter inside the device. The loss P_{D_BUCK} depends on the input supply and the selected switching frequency. Please note, the data is measured in the provided evaluation board (EVM).
3. Determine the load current I_{OUT1} and I_{OUT2} through the power switches. Read $R_{DS(on)1/2}$ of the power switch from the typical characteristics graph.
4. The power loss through power switches can be calculated by:
   $$P_{D\_PW} = R_{DS1(on)} \times I_{OUT1} + R_{DS2(on)} \times I_{OUT2} \quad (14)$$
5. The Dissipating Rating Table provides the thermal resistance, θ_{JA}, for specific packages and board layouts.
6. The maximum temperature inside the IC can be calculated by:
   $$T_J = P_{D\_BUCK} + P_{D\_PW} \times \theta_{JA} + T_A \quad (15)$$

   Where:

   T_A = Ambient temperature (°C)

   θ_{JA} = Thermal resistance (°C/W)

   P_{D_BUCK} = Total power dissipation in buck converter (W)

   P_{D_PW} = Total power dissipation in power switches (W)

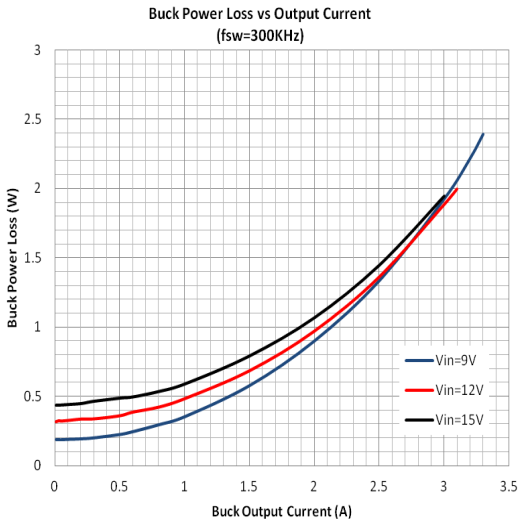


Figure 33. Buck Loss vs Output Current (V_{IN} = 9 V, 12 V and 15 V, f_{SW} = 300 kHz)

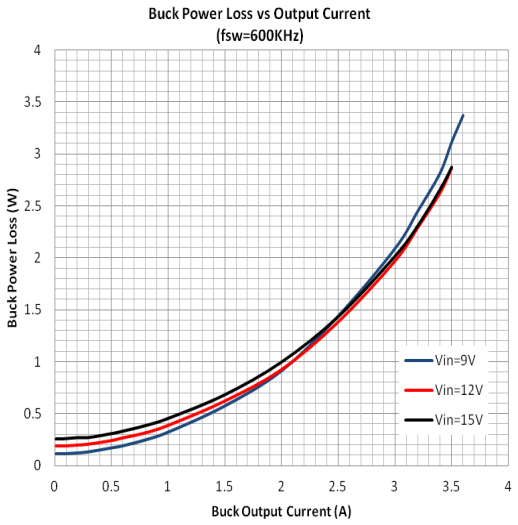


Figure 34. Buck Loss vs Output Current (V_{IN} = 9 V, 12 V and 15 V, f_{SW} = 600 kHz)

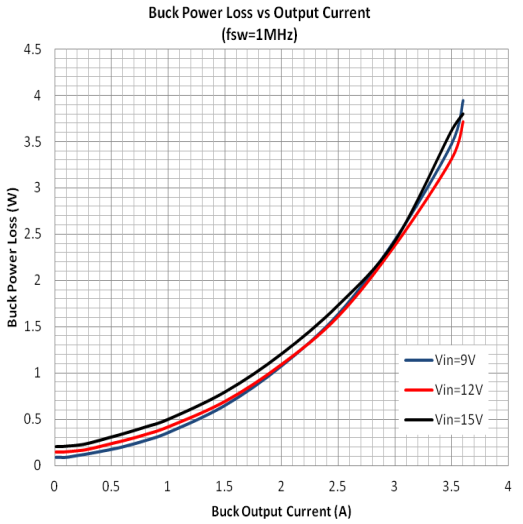


Figure 35. Buck Loss vs Output Current (V_{IN} = 9 V, 12 V and 15 V, f_{SW} = 1 MHz)

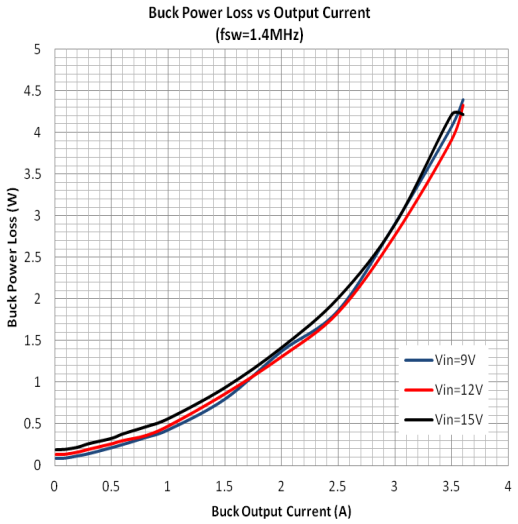


Figure 36. Buck Loss vs Output Current (V_{IN} = 9 V, 12 V and 15 V, f_{SW} = 1.4 MHz)

Auto-Retry Functionality

Some applications require that an over-current condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor shown in Figure 37. During a fault condition, nFAULT pulls low disabling the part. The part is disabled when EN is pulled low, and nFAULT goes high impedance allowing CRETRY to begin charging. The part re-enables when the voltage on EN_SW reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

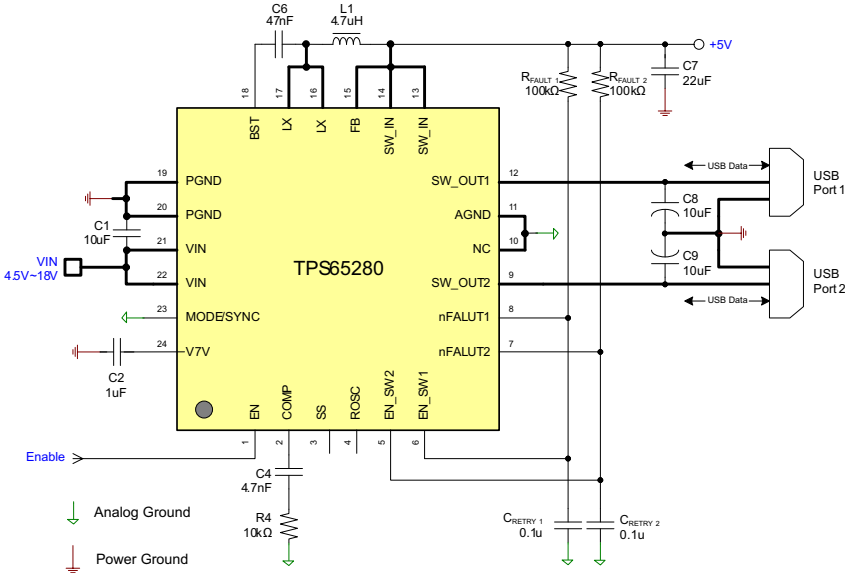


Figure 37. Auto Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 38 shows how an external logic signal can drive EN_SW through RFAULT and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

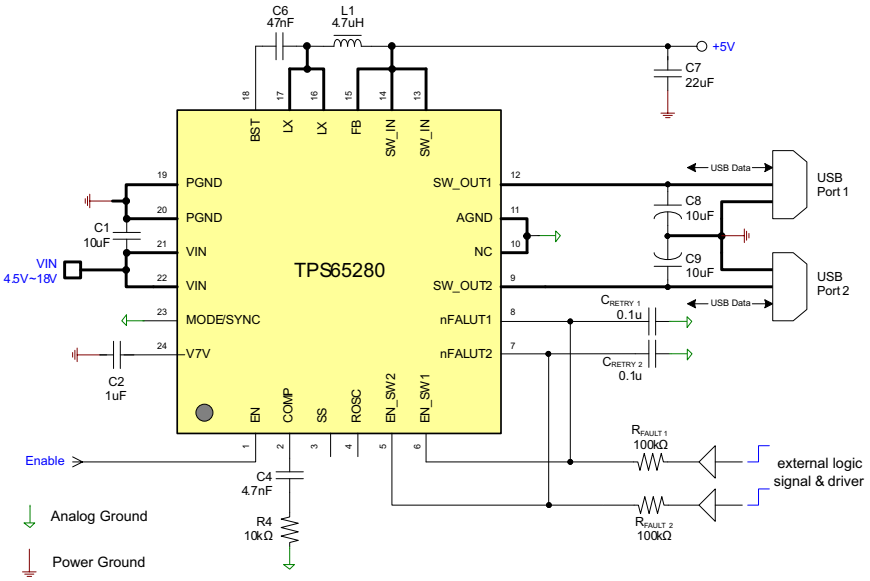


Figure 38. Auto Retry Functionality With External Enable Signal

PCB Layout Recommendation

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 39.

- There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. This capacitor provides the AC current into the internal power MOSFETs. Connect the (+) terminal of the input capacitor as close as possible to the VIN pin, and connect the (-) terminal of the input capacitor as close as possible to the PGND pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the power ground PGND connections.
- Since the LX connection is the switching node, the output inductor should be located close to the LX pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. Keep the switching node, LX, away from all sensitive small-signal nodes.
- Connect V7V decoupling capacitor (connected close to the IC), between the V7V and the power ground PGND pin. This capacitor carries the MOSFET drivers' current peaks.
- Place the output filter capacitor of the buck converter close to SW_IN pins and AGND pin. Try to minimize the ground conductor length while maintaining adequate width.
- The AGND pin should be separately routed to the (-) terminal of V7V bypass capacitor to avoid switching grounding path. A ground plane is recommended connecting to this ground path.
- The compensation should be as close as possible to the COMP pins. The COMP and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of the power components. You can connect the copper areas to PGND, AGND, VIN or any other DC rail in your system.
- There is no electric signal internal connected to thermal pad in the device. Nevertheless connect the exposed pad beneath the IC to ground. Always solder the thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation.

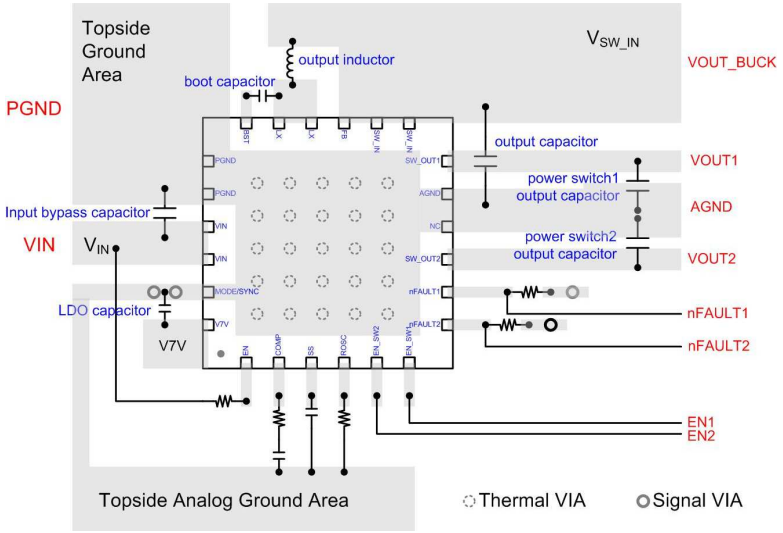


Figure 39. 2-Layers PCB Layout Recommendation Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65280RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65280
TPS65280RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65280

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

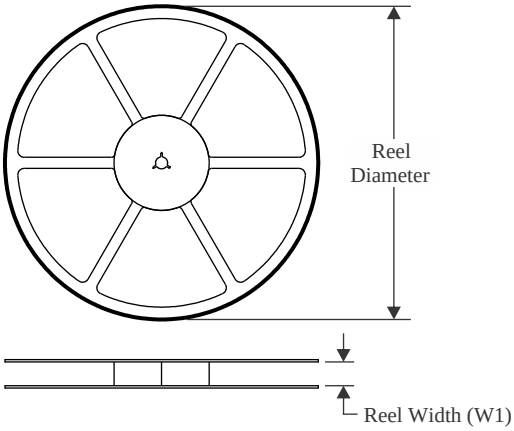
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

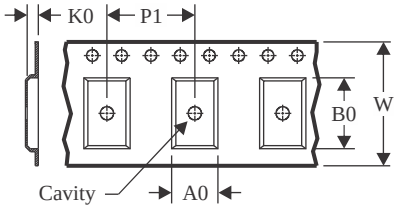
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

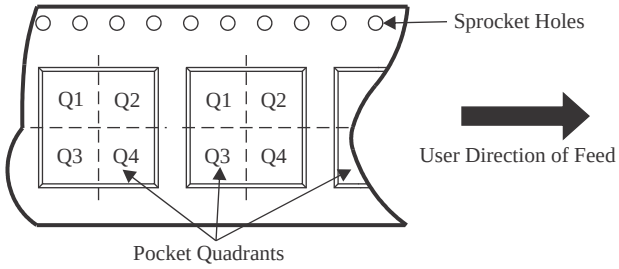


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

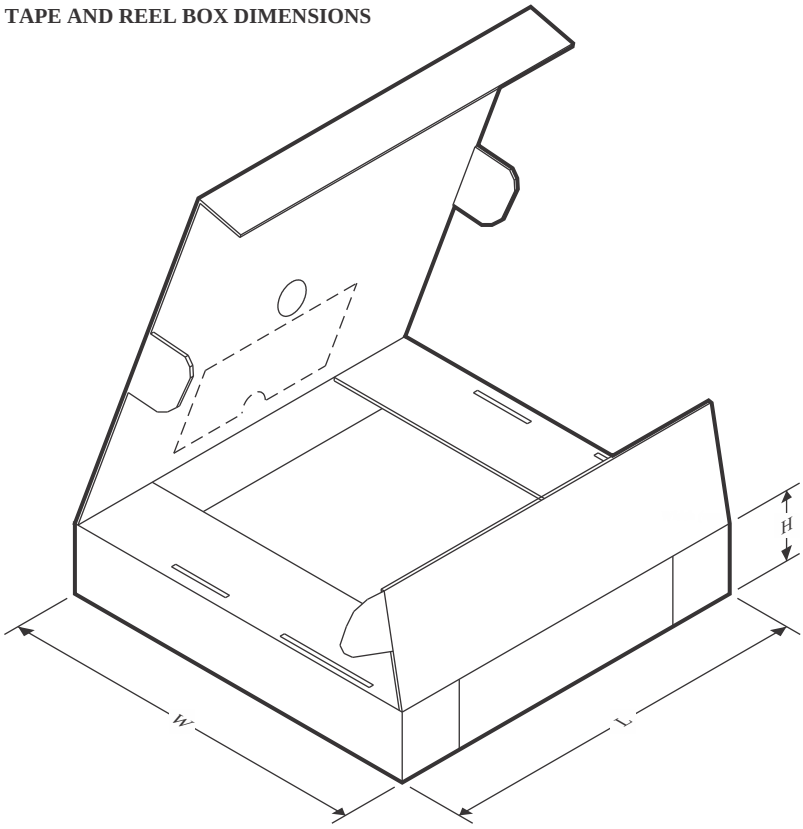
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65280RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



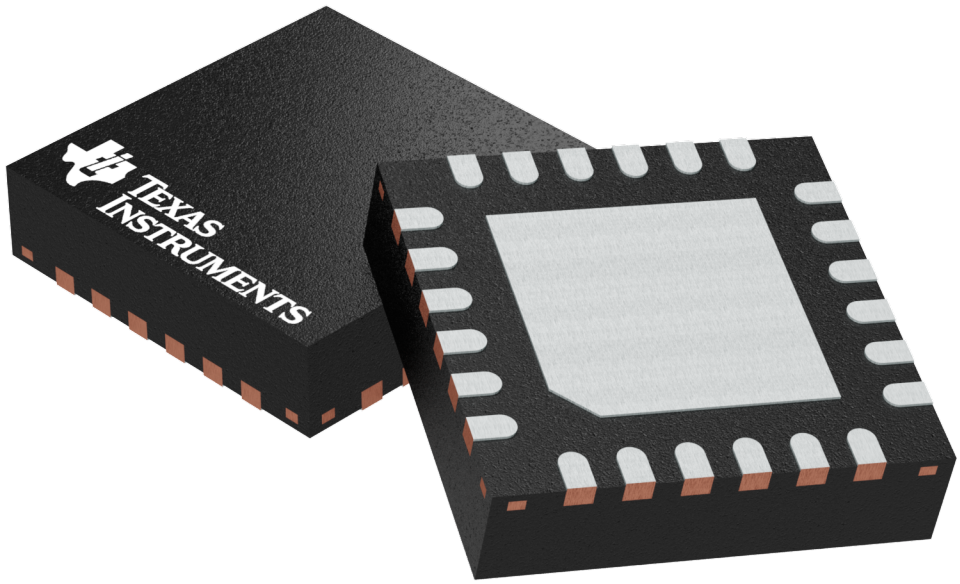
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65280RGER	VQFN	RGE	24	3000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

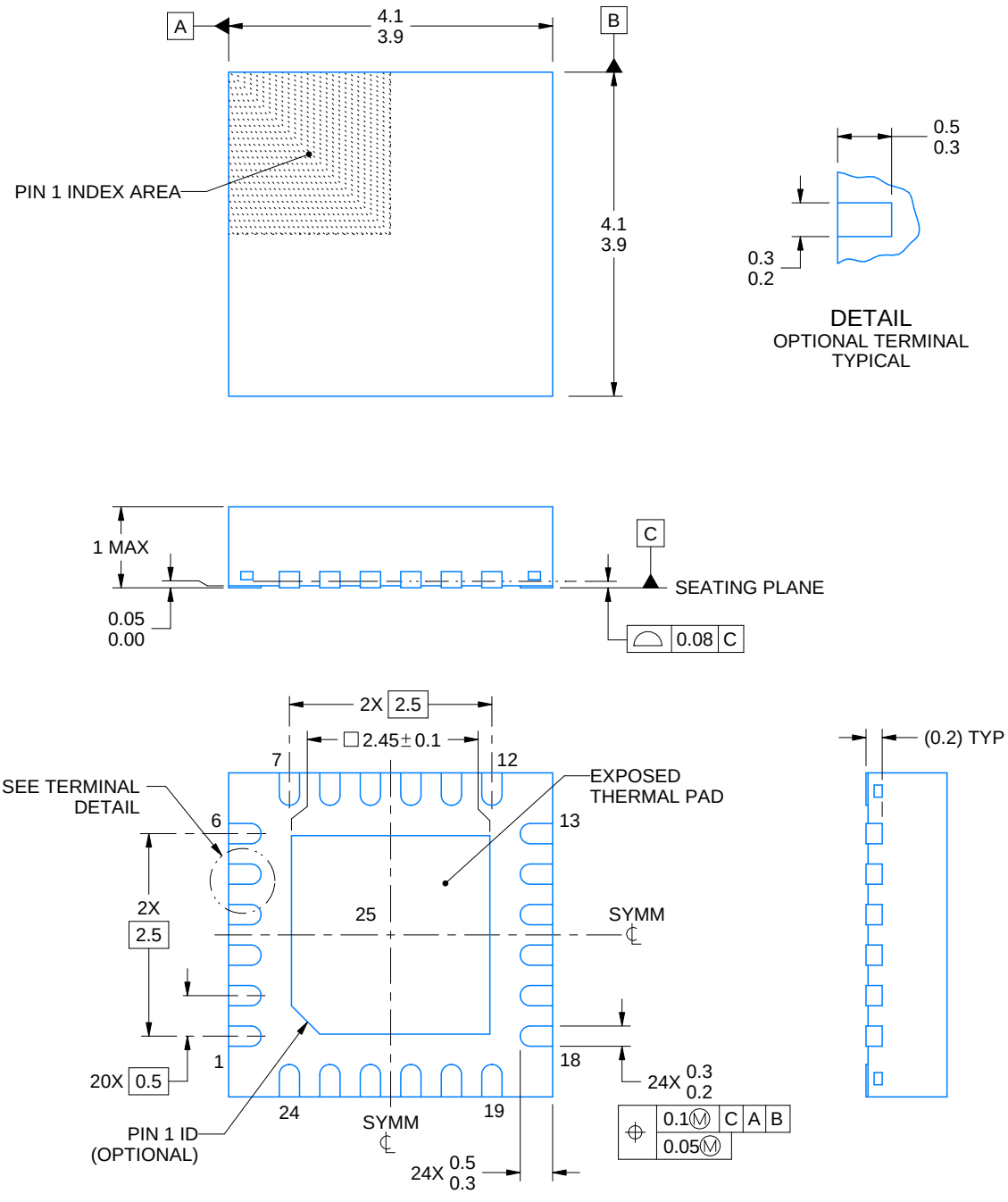
4204104/H

PACKAGE OUTLINE

RGE0024B

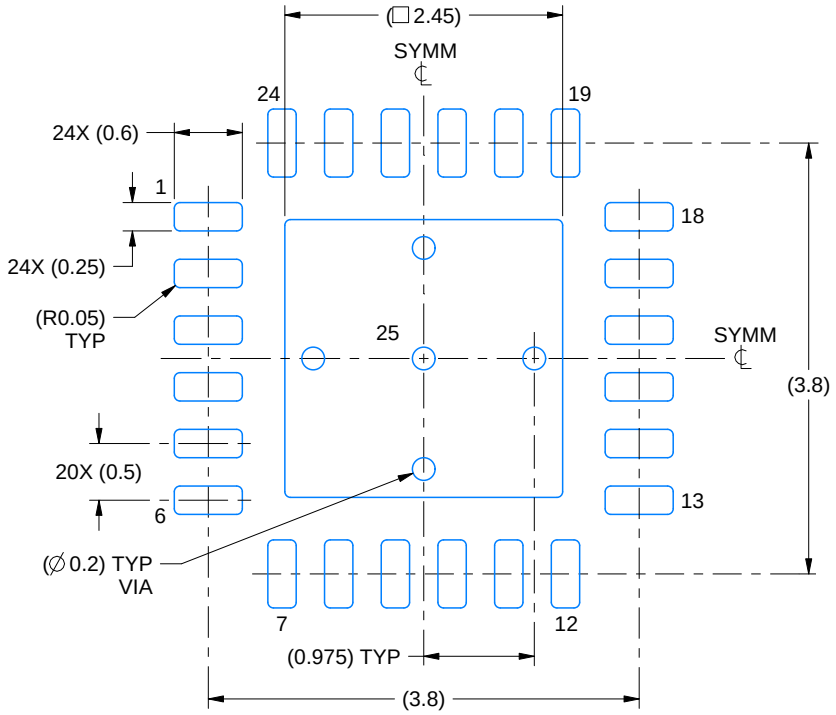
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

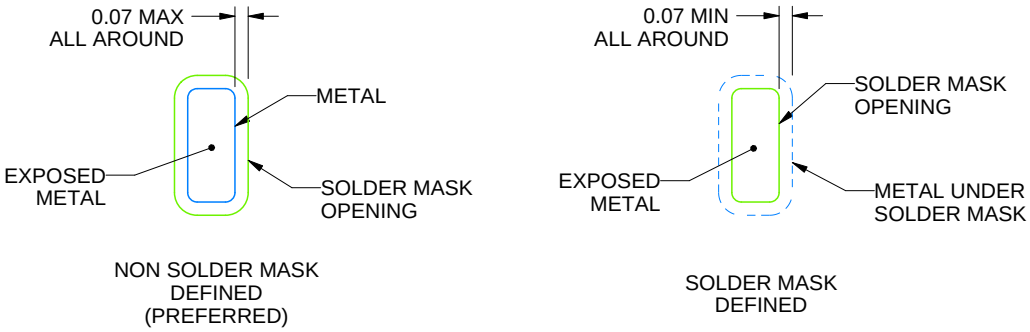


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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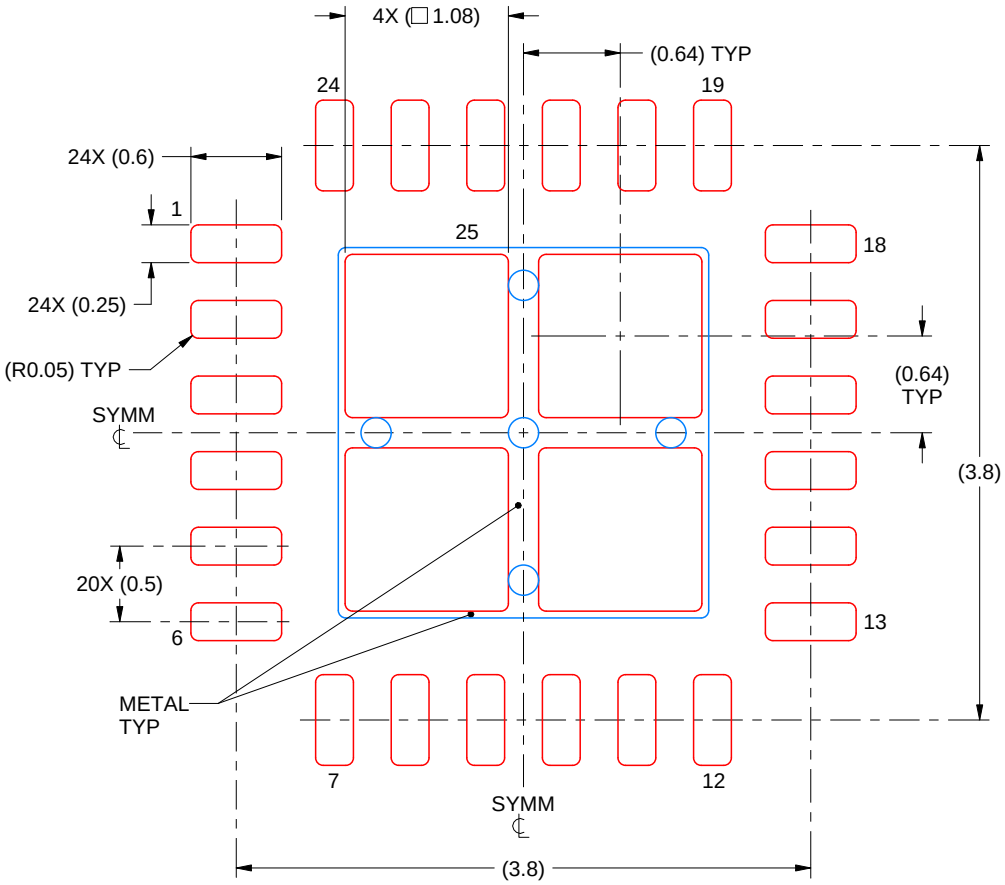
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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