8-Channel, 625 kSPS, 12-Bit Parallel ADCs with a Sequencer

AD7938-6

FEATURES

Fast throughput rate: 625 kSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low power
- **3.6 mW max at 625 kSPS with 3 V supplies**
- **7.5 mW max at 625 kSPS with 5 V supplies**

8 analog input channels with a sequencer
Software configurable analog inputs
- **8-channel single-ended inputs**
- **4-channel fully differential inputs**
- **4-channel pseudo-differential inputs**
- **7-channel pseudo-differential inputs**

Accurate on-chip 2.5 V reference
±0.2% max @ 25°C, 25 ppm/°C max
70 dB SINAD at 50 kHz input frequency
No pipeline delays
High speed parallel interface—word/byte modes
Full shutdown mode: 2 µA max
32-lead LFCSP and TQFP package

FUNCTIONAL BLOCK DIAGRAM

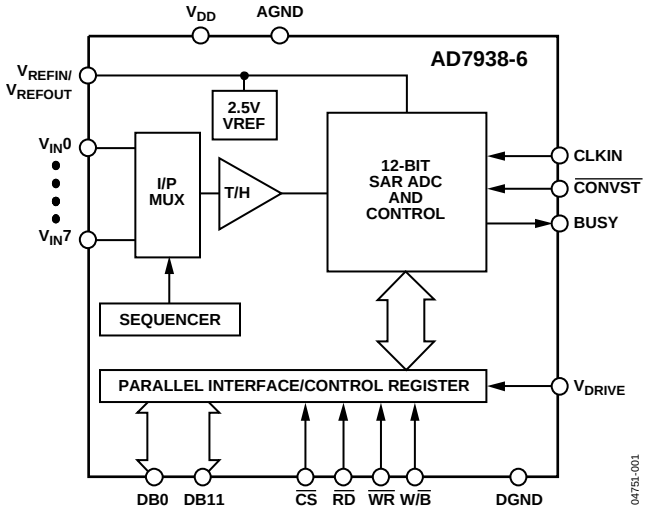

Figure 1.

GENERAL DESCRIPTION

The AD7938-6 is a 12-bit high speed, low power, successive approximation (SAR) ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 625 kSPS. The part contains a low noise, wide bandwidth, differential track-and-hold amplifier that can handle input frequencies up to 50 MHz.

The AD7938-6 features eight analog input channels with a channel sequencer that allows a preprogrammed selection of channels to be converted sequentially. The part can operate with either single-ended, fully differential, or pseudo-differential analog inputs.

The conversion process and data acquisition are controlled using standard control inputs that allow easy interfacing with microprocessors and DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and the conversion is also initiated at this point.

The AD7938-6 has an accurate on-chip 2.5 V reference that can be used as the reference source for the analog-to-digital conversion. Alternatively, this pin can be overdriven to provide an external reference.

The AD7938-6 uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also features flexible power management options. An on-chip control register allows the user to set up different operating conditions, including analog input range and configuration, output coding, power management, and channel sequencing.

PRODUCT HIGHLIGHTS

1. High throughput with low power consumption.
2. Eight analog inputs with a channel sequencer.
3. Accurate on-chip 2.5 V reference.
4. Software configurable analog inputs. Single-ended, pseudo-differential, or fully differential analog inputs that are software selectable.
5. Single-supply operation with V_{DRIVE} function. The V_{DRIVE} function allows the parallel interface to connect directly to 3 V, or 5 V processor systems independent of V_{DD}.
6. No pipeline delay.
7. Accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

Rev. 0
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REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, internal/external V_{REF} = 2.5 V, unless otherwise noted, F_{CLKIN} = 10 MHz, F_{SAMPLE} = 625 kSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 50 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	Differential mode
	68	dB min	Single-ended mode
Signal-to-Noise Ratio (SNR)[2]	71	dB min	Differential mode
	69	dB min	Single-ended mode
Total Harmonic Distortion (THD)[2]	−73	dB max	−85 dB typ, differential mode
	−70	dB max	−80 dB typ, single-ended mode
Peak Harmonic or Spurious Noise (SFDR)[2]	−73	dB max	−82 dB typ
Intermodulation Distortion (IMD)[2]			fa = 30 kHz, fb = 50 kHz
Second-Order Terms	−86	dB typ	
Third-Order Terms	−90	dB typ	
Channel-to-Channel Isolation	−85	dB typ	F_{IN} = 50 kHz, F_{NOISE} = 300 kHz
Aperture Delay[2]	5	ns typ	
Aperture Jitter[2]	72	ps typ	
Full Power Bandwidth[2]	50	MHz typ	@ 3 dB
	10	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	Differential mode
	±1.5	LSB max	Single-ended mode
Differential Nonlinearity[2]			
Differential Mode	±0.95	LSB max	Guaranteed no missed codes to 12 bits
Single-Ended Mode	−0.95/+1.5	LSB max	Guaranteed no missed codes to 12 bits
Single-Ended and Pseudo-Differential Input			Straight binary output coding
Offset Error[2]	±6	LSB max	
Offset Error Match[2]	±1	LSB max	
Gain Error[2]	±3	LSB max	
Gain Error Match[2]	±1	LSB max	
Fully Differential Input			Twos complement output coding
Positive Gain Error[2]	±3	LSB max	
Positive Gain Error Match[2]	±1	LSB max	
Zero-Code Error[2]	±6	LSB max	
Zero-Code Error Match[2]	±1	LSB max	
Negative Gain Error[2]	±3	LSB max	
Negative Gain Error Match[2]	±1	LSB max	
ANALOG INPUT			
Single-Ended Input Range	0 to V_{REF} or 0 to 2 × V_{REF}	V	RANGE bit = 0, or RANGE bit = 1, respectively
Pseudo-Differential Input Range: V_{IN+}	0 to V_{REF} or 2 × V_{REF}	V	RANGE bit = 0, or RANGE bit = 1, respectively
V_{IN-}	−0.3 to +0.7	V typ	V_{DD} = 3 V
	−0.3 to +1.8	V typ	V_{DD} = 3 V
Fully Differential Input Range: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = common-mode voltage[3] = V_{REF}/2
V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}	V	V_{CM} = V_{REF}, V_{IN+} or V_{IN-} must remain within GND/V_{DD}
DC Leakage Current[4]	±1	µA max	
Input Capacitance	45	pF typ	When in track
	10	pF typ	When in hold

Parameter	B Version[1]	Unit	Test Conditions/Comments
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage[5]	2.5	V	±1% for specified performance
DC Leakage Current	±1	µA max	
V_{REFOUT} Output Voltage	2.5	V	±0.2% max @ 25°C
V_{REFOUT} Temperature Coefficient	25	ppm/°C max	5 ppm/°C typ
V_{REF} Noise	10	µV typ	0.1 Hz to 10 Hz bandwidth
	130	µV typ	0.1 Hz to 1 MHz bandwidth
V_{REF} Output Impedance	10	Ω typ	
V_{REF} Input Capacitance	15	pF typ	When in track
	25	pF typ	When in hold
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±5	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±3	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit = 0
	Twos Complement		CODING bit = 1
CONVERSION RATE			
Conversion Time	t_2 + 13 t_{CLK}	ns	
Track-and-Hold Acquisition Time	125	ns max	Full-scale step input
Throughput Rate	625	kSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[6]			Digital I/P_S = 0 V or V_{DRIVE}
Normal Mode (Static)	0.8	mA typ	V_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	1.5	mA max	V_{DD} = 4.75 V to 5.25 V
	1.2	mA max	V_{DD} = 2.7 V to 3.6 V
Autostandby Mode	0.3	mA typ	F_{SAMPLE} = 100 kSPS, V_{DD} = 5 V
	160	µA typ	(Static)
Full/Autoshutdown Mode (Static)	2	µA max	SCLK on or off
Power Dissipation			
Normal Mode (Operational)	7.5	mW max	V_{DD} = 5 V
	3.6	mW max	V_{DD} = 3 V
Autostandby Mode (Static)	800	µW typ	V_{DD} = 5 V
	480	µW typ	V_{DD} = 3 V
Full/Autoshutdown Mode (Static)	10/6	µW max	V_{DD} = 5 V/3 V

[1] Temperature ranges as follows: B Versions: −40°C to +85°C.
[2] See the Terminology section.
[3] For full common-mode range, see Figure 25 and Figure 26.
[4] Sample tested during initial release to ensure compliance.
[5] This device is operational with an external reference in the range 0.1 V to V_{DD}. See the Reference Section for more information.
[6] Measured with a midscale dc analog input.

TIMING SPECIFICATIONS[1]

V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, internal/external V_{REF} = 2.5 V, unless otherwise noted; F_{CLKIN} = 10MHz, F_{SAMPLE} = 625 kSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} AD7938-6	Unit	Description
f_{CLKIN}	50	kHz min	
	10	MHz max	
t_{QUIET}	30	ns min	Minimum time between end of read and start of next conversion, i.e., time from when the data bus goes into three-state until the next falling edge of $\overline{CONVST}$.
t_1	10	ns min	$\overline{CONVST}$ Pulse Width.
t_2	15	ns min	$\overline{CONVST}$ Falling Edge to CLKIN Falling Edge Setup Time.
t_3	50	ns min	CLKIN Falling Edge to BUSY Rising Edge.
t_4	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time.
t_5	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time.
t_6	10	ns min	$\overline{WR}$ Pulse Width.
t_7	10	ns min	Data Setup Time before $\overline{WR}$.
t_8	10	ns min	Data Hold after $\overline{WR}$.
t_9	10	ns min	New Data Valid before Falling Edge of BUSY.
t_{10}	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time.
t_{11}	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time.
t_{12}	30	ns min	$\overline{RD}$ Pulse Width.
t_{13}[2]	30	ns max	Data Access Time after $\overline{RD}$.
t_{14}[3]	3	ns min	Bus Relinquish Time after $\overline{RD}$.
	50	ns max	Bus Relinquish Time after $\overline{RD}$.
t_{15}	0	ns min	HBEN to $\overline{RD}$ Setup Time.
t_{16}	0	ns min	HBEN to $\overline{RD}$ Hold Time.
t_{17}	10	ns min	Minimum Time between Reads/Writes.
t_{18}	0	ns min	HBEN to $\overline{WR}$ Setup Time.
t_{19}	10	ns min	HBEN to $\overline{WR}$ Hold Time.
t_{20}	40	ns max	CLKIN Falling Edge to BUSY Falling Edge.
t_{21}	15.7	ns min	CLKIN Low Pulse Width.
t_{22}	7.8	ns min	CLKIN High Pulse Width.

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. All timing specifications given above are with a 25 pF load capacitance (see Figure 35, Figure 36, Figure 37, and Figure 38).

[2] The time required for the output to cross 0.4 V or 2.4 V.

[3] t_{14} is derived from the measured time taken by the data outputs to change 0.5 V. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_{14}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND/DGND	−0.3 V to +7 V
V_{DRIVE} to AGND/DGND	−0.3 V to V_{DD} +0.3 V
Analog Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
V_{DRIVE} to V_{DD}	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REFIN} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	108.2°C/W (LFCSP)
	121°C/W (TQFP)
θ_{JC} Thermal Impedance	32.71°C/W (LFCSP)
	45°C/W (TQFP)
Lead Temperature, Soldering	
Reflow Temperature (10 sec to 30 sec)	255°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

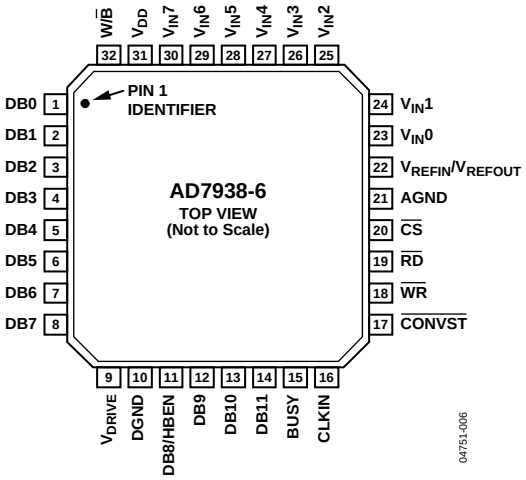


Figure 2. Pin Configuration

Table 4. Pin Function Description

Pin No	Mnemonic	Function
1 to 8	DB0 to DB7	Data Bits 0 to 7. Three-state parallel digital I/O pins that provide the conversion result and also allow the control and shadow registers to be programmed. These pins are controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input.
9	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the parallel interface of the AD7938-6 operates. This pin should be decoupled to DGND. The voltage at this pin may be different to that at V_{DD} but should never exceed V_{DD} by more than 0.3 V.
10	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7938-6. This pin should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
11	DB8/HBEN	Data Bit 8/High Byte Enable. When W/$\overline{B}$ is high, this pin acts as Data Bit 8, a three-state I/O pin that is controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. When W/$\overline{B}$ is low, this pin acts as the high byte enable pin. When HBEN is low, the low byte of data being written to or read from the AD7938-6 is on DB0 to DB7. When HBEN is high, the top four bits of the data being written to or read from the AD7938-6 are on DB0 to DB3. When reading from the device, DB4 to DB6 of the high byte contains the ID of the channel to which the conversion result corresponds (see the channel address bits in Table 8). When writing to the device, DB4 to DB7 of the high byte must be all 0s.
12 to 14	DB9 to DB11	Data Bits 9 to 11. Three-state parallel digital I/O pins that provide the conversion result and also allow the control and shadow registers to be programmed in word mode. These pins are controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input.
15	BUSY	Busy Output. Logic output indicating the status of the conversion. The BUSY output goes high following the falling edge of $\overline{CONVST}$ and stays high for the duration of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output goes low. The track-and-hold returns to track mode just prior to the falling edge of BUSY on the 13th rising edge of SCLK, see Figure 35.
16	CLKIN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7938-6 takes 13 clock cycles + t_2. The frequency of the master clock input therefore determines the conversion time and achievable throughput rate. The CLKIN signal may be a continuous or burst clock.
17	$\overline{CONVST}$	Conversion Start Input. A falling edge on $\overline{CONVST}$ is used to initiate a conversion. The track-and-hold goes from track to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initiated at this point. Following power-down, when operating in autoshutdown or autostandby modes, a rising edge on $\overline{CONVST}$ is used to power-up the device.
18	$\overline{WR}$	Write Input. Active low logic input used in conjunction with $\overline{CS}$ to write data to the internal registers.
19	$\overline{RD}$	Read Input. Active low logic input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of $\overline{RD}$ read while $\overline{CS}$ is low.
20	$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ and $\overline{WR}$ to read conversion data or to write data to the internal registers.

Pin No	Mnemonic	Function
21	AGND	Analog Ground. This is the ground reference point for all analog circuitry on the AD7938-6. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
22	V_{REFIN}/V_{REFOUT}	Reference Input/Output. This pin is connected to the internal reference and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V and this appears at this pin. This pin can be overdriven by an external reference. The input voltage range for the external reference is 0.1 V to V_{DD}; however, care must be taken to ensure that the analog input range does not exceed V_{DD} + 0.3 V. See the Reference Section.
23 to 30	$V_{IN}0$ to $V_{IN}7$	Analog Input 0 to Analog Input 7. Eight analog input channels that are multiplexed into the on-chip track-and-hold. The analog inputs can be programmed to be eight single-ended inputs, four fully differential pairs, four pseudo-differential pairs, or seven pseudo-differential inputs by setting the MODE bits in the control register appropriately (see Table 8). The analog input channel to be converted can either be selected by writing to the address bits (ADD2 to ADD0) in the control register prior to the conversion or the on-chip sequencer can be used. The SEQ and SHDW bits in conjunction with the address bits in the control register allow the shadow register to be programmed. The input range for all input channels can either be 0 V to V_{REF} or 0 V to 2 × V_{REF}, and the coding can be binary or twos complement, depending on the states of the RANGE and CODING bits in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
31	V_{DD}	Power Supply Input. The V_{DD} range for the AD7938-6 is 2.7 V to 5.25 V. The supply should be decoupled to AGND with a 0.1 µF capacitor and a 10 µF tantalum capacitor.
32	W/$\overline{B}$	Word/Byte Input. When this input is logic high, data is transferred to and from the AD7938-6 in 12-bit words on Pins DB0 to DB11. When this pin is logic low, byte transfer mode is enabled. Data and the channel ID are transferred on Pins DB0 to DB7, and Pin DB8/HBEN assumes its HBEN functionality. Unused data lines when operating in byte transfer mode should be tied off to DGND.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . .000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . .110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Zero-Code Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REF} input range with –V_{REF} to +V_{REF} biased about the V_{REFIN} point. It is the deviation of the mid scale transition (all 0s to all 1s) from the ideal V_{IN} voltage, i.e., V_{REF}.

Zero-Code Error Match
This is the difference in zero-code error between any two channels.

Positive Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REF} input range with –V_{REF} to +V_{REF} biased about the V_{REFIN} point. It is the deviation of the last code transition (011. . .110) to (011 .. . 111) from the ideal (i.e., +V_{REF} – 1 LSB) after the zero-code error has been adjusted out.

Positive Gain Error Match
This is the difference in positive gain error between any two channels.

Negative Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REF} input range with –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (i.e., –V_{REFIN} + 1 LSB) after the zero-code error has been adjusted out.

Negative Gain Error Match
This is the difference in negative gain error between any two channels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale sine wave signal to all seven nonselected input channels and applying a 50 kHz signal to the selected channel. The channel-to-channel isolation is defined as the ratio of the power of the 50 kHz signal on the selected channel to the power of the noise signal on the unselected channels that appears in the FFT of this channel. The noise frequency on the unselected channels varies from 40 kHz to 740 kHz. The noise amplitude is at 2 × V_{REF}, while the signal amplitude is at 1 × V_{REF}.

Power Supply Rejection Ratio (PSRR)
PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S. The frequency of the noise varies from 1 kHz to 1 MHz.

$$PSRR \text{ (dB)} = 10\log(Pf/Pf_S)$$

Pf is the power at frequency *f* in the ADC output; Pf_S is the power at frequency f_S in the ADC output.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and $V_{IN–}$ of frequency f_S as

$$CMRR \text{ (dB)} = 10\log (Pf/Pf_S)$$

Pf is the power at frequency f in the ADC output; Pf_S is the power at frequency f_S in the ADC output.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7938-6, it is defined as

$$THD\,(\text{dB}) = -20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7938-6 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

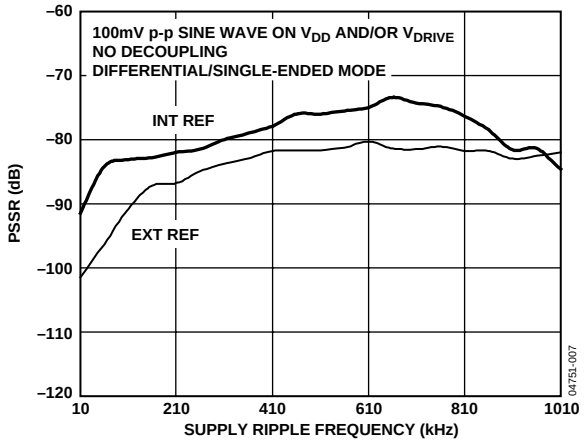


Figure 3. PSRR vs. Supply Ripple Frequency without Supply Decoupling

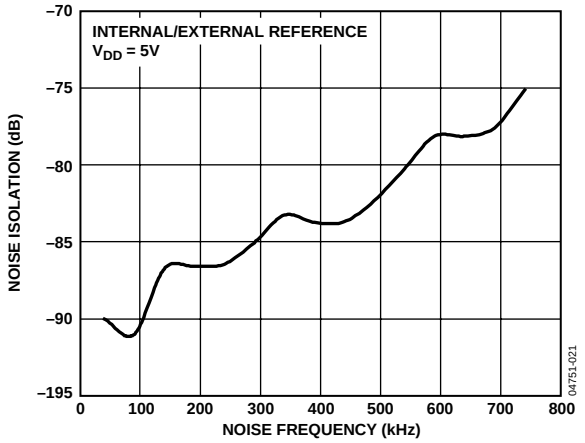


Figure 4. AD7938-6 Channel-to-Channel Isolation

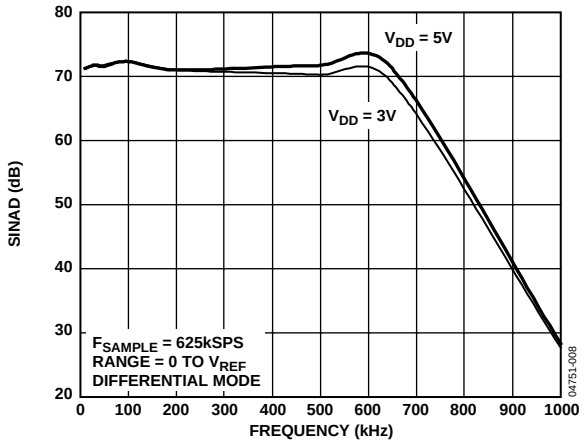


Figure 5. AD7938-6 SINAD vs. Analog Input Frequency for Various Supply Voltages

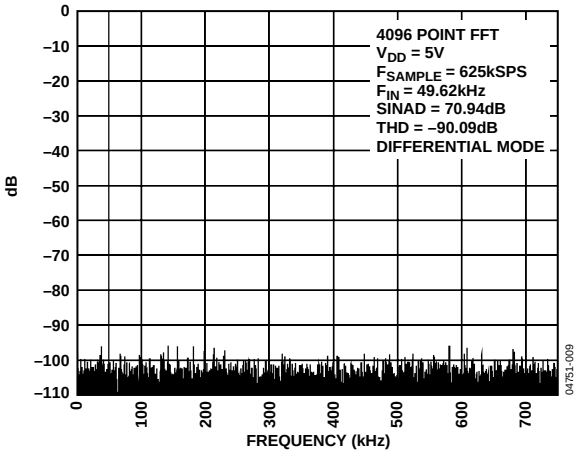


Figure 6. AD7938-6 FFT @ V_{DD} = 5 V

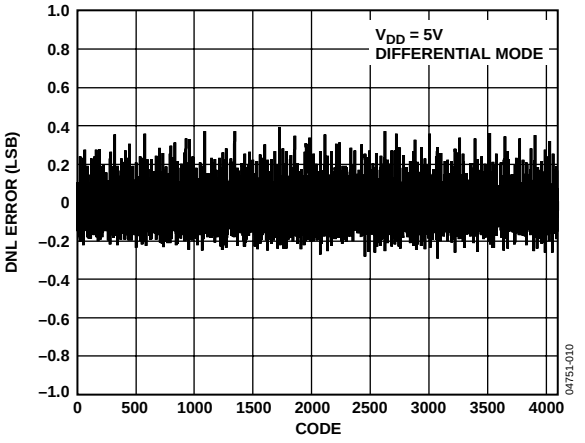


Figure 7. AD7938-6 Typical DNL @ V_{DD} = 5 V

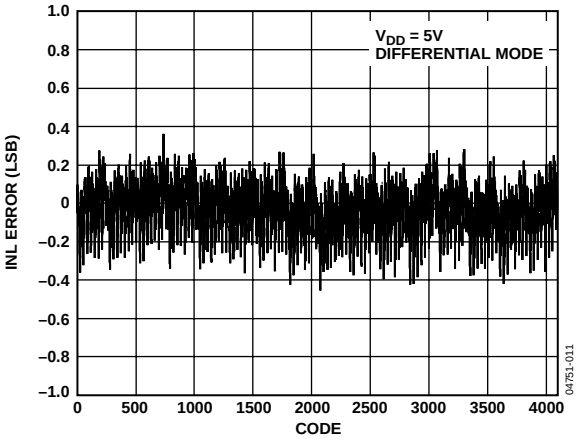


Figure 8. AD7938-6 Typical INL @ V_{DD} = 5 V

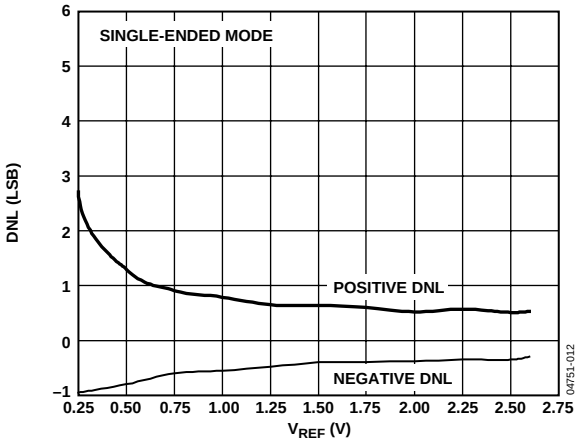


Figure 9. AD7938-6 DNL vs. V_{REF} for V_{DD} = 3 V

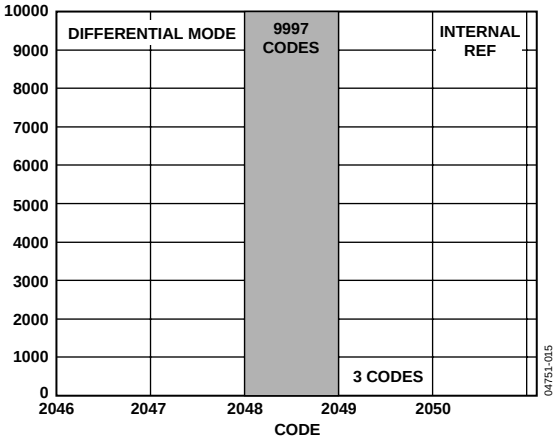


Figure 12. AD7938-6 Histogram of Codes for 10k Samples @ V_{DD} = 5 V with the Internal Reference

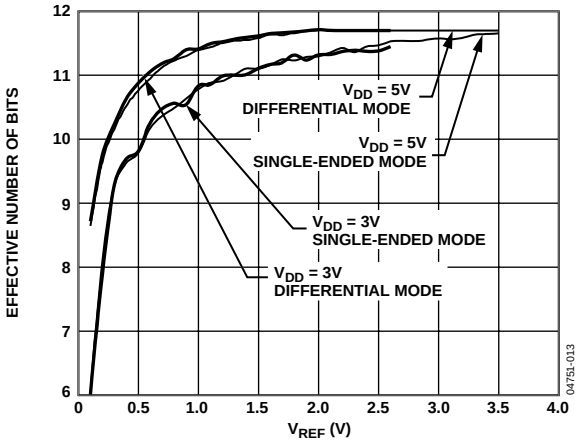


Figure 10. AD7938-6 ENOB vs. V_{REF}

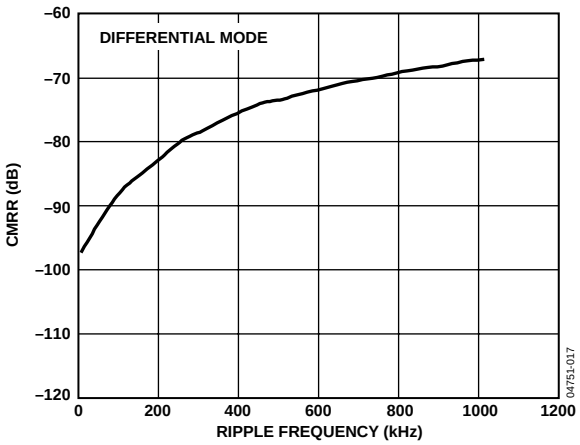


Figure 13. CMRR vs. Input Frequency with V_{DD} = 5 V and 3 V

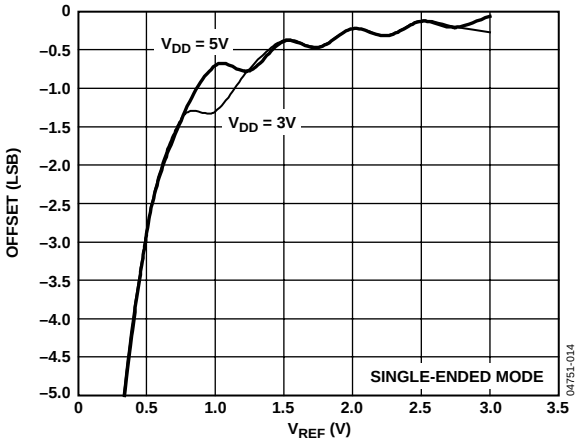


Figure 11. AD7938-6 Offset vs. V_{REF}

ON-CHIP REGISTERS

The AD7938-6 has two on-chip registers that are necessary for the operation of the device. These are the control register, which is used to set up different operating conditions, and the shadow register, which is used to program the analog input channels to be converted.

CONTROL REGISTER

The control register on the AD7938-6 is a 12-bit, write-only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins. The control register is shown below and the functions of the bits are described in Table 6. At power up, the default bit settings in the control register are all 0s.

Table 5. Control Register Bits

MSB											LSB
DB11	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
PM1	PM0	CODING	REF	ADD2	ADD1	ADD0	MODE1	MODE0	SHDW	SEQ	RANGE

Table 6. Control Register Bit Function Description

Bit No.	Mnemonic	Description
11, 10	PM1, PM0	Power Management Bits. These two bits are used to select the power mode of operation. The user can choose between either normal mode or various power-down modes of operation as shown in Table 7.
9	CODING	This bit selects the output coding of the conversion result. If this bit is set to 0, the output coding is straight (natural) binary. If this bit is set to 1, the output coding is twos complement.
8	REF	This bit selects whether the internal or external reference is used to perform the conversion. If this bit is Logic 0, an external reference should be applied to the V_{REF} pin, and if this bit is Logic 1, the internal reference is selected (see the Reference Section).
7 to 5	ADD2 to ADD0	These three address bits are used to either select which analog input channel is converted in the next conversion if the sequencer is not used, or to select the final channel in a consecutive sequence when the sequencer is used as described in Table 9. The selected input channel is decoded as shown in Table 8.
4, 3	MODE1, MODE0	The two mode pins select the type of analog input on the eight V_{IN} pins. The AD7938-6 can have either eight single-ended inputs, four fully differential inputs, four pseudo-differential inputs, or seven pseudo-differential inputs (see Table 8).
2	SHDW	The SHDW bit in the control register is used in conjunction with the SEQ bit to control the sequencer function and access the SHDW register (see Table 9).
1	SEQ	The SEQ bit in the control register is used in conjunction with the SHDW bit to control the sequencer function and access the SHDW register (see Table 9).
0	RANGE	This bit selects the analog input range of the AD7938-6. If it is set to 0, then the analog input range extends from 0 V to V_{REF}. If it is set to 1, then the analog input range extends from 0 V to 2 × V_{REF}. When this range is selected, AV_{DD} must be 4.75 V to 5.25 V if a 2.5 V reference is used; otherwise, care must be taken to ensure that the analog input remains within the supply rails. See Analog Inputs section for more information.

Table 7. Power Mode Selection using the Power Management Bits in the Control Register

PM1	PM0	Mode	Description
0	0	Normal Mode	When operating in normal mode, all circuitry is fully powered up at all times.
0	1	Autoshutdown	When operating in autoshutdown mode, the AD7938-6 enters full shutdown mode at the end of each conversion. In this mode, all circuitry is powered down.
1	0	Autostandby	When the AD7938-6 enters this mode, all circuitry is powered down except for the reference and reference buffer. This mode is similar to autoshutdown mode, but it allows the part to power-up in 7 µs (or 600 ns if an external reference is used). See the Power Modes of Operation section for more information.
1	1	Full Shutdown	When the AD7938-6 enters this mode, all circuitry is powered down. The information in the control register is retained.

Table 8. Analog Input Type Selection

Channel Address			MODE0 = 0, MODE1 = 0		MODE0 = 0, MODE1 = 1		MODE0 = 1, MODE1 = 0		MODE0 = 1, MODE1 = 1	
			Eight Single-Ended I/P Channels		Four Fully Differential I/P Channels		Four Pseudo-Differential I/P Channels (Pseudo Mode 1)		Seven Pseudo-Differential I/P Channels (Pseudo Mode 2)	
ADD2	ADD1	ADD0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}
0	0	0	VIN0	AGND	VIN0	VIN1	VIN0	VIN1	VIN0	VIN7
0	0	1	VIN1	AGND	VIN1	VIN0	VIN1	VIN0	VIN1	VIN7
0	1	0	VIN2	AGND	VIN2	VIN3	VIN2	VIN3	VIN2	VIN7
0	1	1	VIN3	AGND	VIN3	VIN2	VIN3	VIN2	VIN3	VIN7
1	0	0	VIN4	AGND	VIN4	VIN5	VIN4	VIN5	VIN4	VIN7
1	0	1	VIN5	AGND	VIN5	VIN4	VIN5	VIN4	VIN5	VIN7
1	1	0	VIN6	AGND	VIN6	VIN7	VIN6	VIN7	VIN6	VIN7
1	1	1	VIN7	AGND	VIN7	VIN6	VIN7	VIN6	Not Allowed	

SEQUENCER OPERATION

The configuration of the SEQ and SHDW bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table 9 outlines the four modes of operation of the sequencer.

Table 9. Sequence Selection

SEQ	SHDW	Sequence Type
0	0	This configuration is selected when the sequence function is not used. The analog input channel selected on each individual conversion is determined by the contents of the channel address bits, ADD2 to ADD0, in each prior write operation. This mode of operation reflects the traditional operation of a multichannel ADC, without the sequencer function being used, where each write to the AD7938-6 selects the next channel for conversion.
0	1	This configuration selects the shadow register for programming. The following write operation loads the data on DB0 to DB7 to the shadow register. This programs the sequence of channels to be converted continuously after each $\overline{\text{CONVST}}$ falling edge (see the shadow register description and Table 10).
1	0	If the SEQ and SHADOW bits are set in this way, the sequence function is not interrupted upon completion of the write operation. This allows other bits in the control register to be altered between conversions while in a sequence without terminating the cycle.
1	1	This configuration is used in conjunction with the channel address bits (ADD2 to ADD0) to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the channel address bits in the control register.

SHADOW REGISTER

The shadow register on the AD7938-6 is an 8-bit, write-only register. Data is loaded from DB0 to DB7 on the rising edge of $\overline{\text{WR}}$. The eight LSBs load into the shadow register. The information is written into the shadow register provided that the SEQ and SHDW bits in the control register were set to 0 and 1, respectively, in the previous write to the control register. Each bit represents an analog input from Channel 0 through Channel 7. A sequence of channels may be selected through which the AD7938-6 cycles with each consecutive conversion after the write to the shadow register. To select a sequence of channels to be converted, if operating in single-ended mode or Pseudo Mode 2, the associated channel bit in the shadow register must be set for each required analog input. When operating in differential mode or Pseudo Mode 1, the associated pair of channels' bits must be set for each pair of analog inputs required in the sequence. With each consecutive $\overline{\text{CONVST}}$ pulse after the sequencer has been set up, the AD7938-6 progresses through the selected channels in ascending order, beginning with the lowest channel. This continues until a write operation occurs with the SEQ and SHDW bits configured in any way except 1, 0 (see Table 9). When a sequence is set up in differential or Pseudo Mode 1, the ADC does not convert on the inverse pairs (i.e., VIN1, VIN0). The bit functions of the shadow register are outlined in Table 10. See the Analog Input Selection section for further information on using the sequencer.

Table 10. Shadow Register Bit Functions

$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$

CIRCUIT INFORMATION

The AD7938-6 is a fast, 8-channel, 12-bit, single-supply, successive approximation analog-to-digital converter. The part can operate from a 2.7 V to 5.25 V power supply and features throughput rates up to 625 kSPS.

The AD7938-6 provides the user with an on-chip track-and-hold, an accurate internal reference, an analog-to-digital converter, and a parallel interface housed in a 32-lead LFCSP or TQFP package.

The AD7938-6 has eight analog input channels that can be configured to be eight single-ended inputs, four fully differential pairs, four pseudo-differential pairs, or seven pseudo-differential inputs with respect to one common input. There is an on-chip user-programmable channel sequencer that allows the user to select a sequence of channels through which the ADC can progress and cycle with each consecutive falling edge of $\overline{\text{CONVST}}$.

The analog input range for the AD7938-6 is 0 to V_{REF} or 0 to $2 \times V_{REF}$ depending on the status of the RANGE bit in the control register. The output coding of the ADC can be either binary or twos complement, depending on the status of the CODING bit in the control register.

The AD7938-6 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the control register.

CONVERTER OPERATION

The AD7938-6 is a successive approximation ADC based around two capacitive DACs. Figure 14 and Figure 15 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises of control logic, a SAR, and two capacitive DACs. Both figures show the operation of the ADC in differential/pseudo-differential mode. Single-ended mode operation is similar but V_{IN-} is internally tied to AGND. In acquisition phase, SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

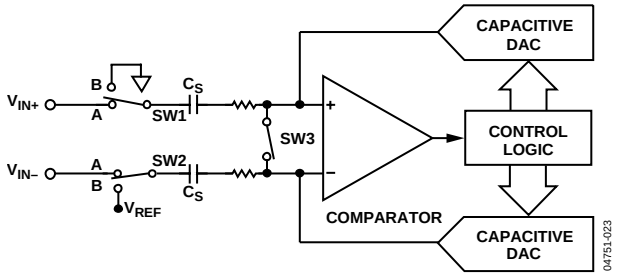


Figure 14. ADC Acquisition Phase

When the ADC starts a conversion (Figure 15), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the $V_{IN}+$ and the V_{IN-} pins must match; otherwise, the two inputs have different settling times, which result in errors.

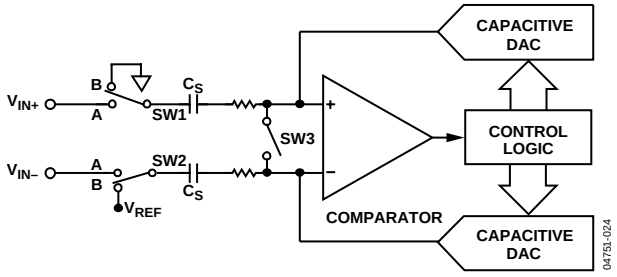


Figure 15. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7938-6 is either straight binary or twos complement, depending on the status of the CODING bit in the control register. The designed code transitions occur at successive LSB values (i.e., 1 LSB, 2 LSBs, and so on) and the LSB size is $V_{REF}/4096$. The ideal transfer characteristics of the AD7938-6 for both straight binary and twos complement output coding are shown in Figure 16 and Figure 17, respectively.

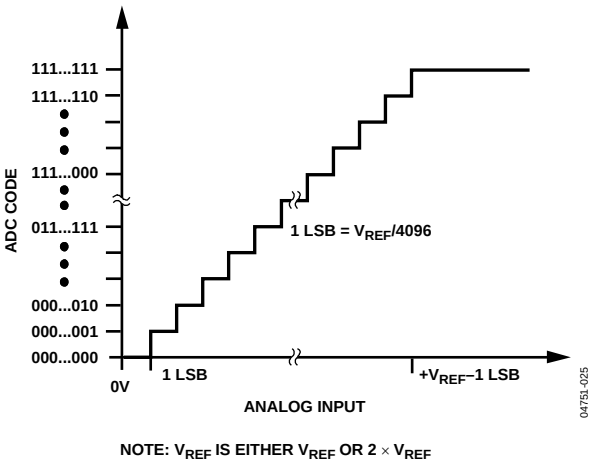


Figure 16. AD7938-6 Ideal Transfer Characteristic with Straight Binary Output Coding

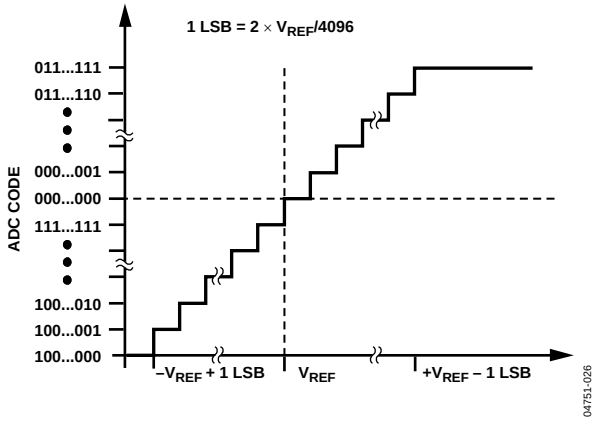


Figure 17. AD7938-6 Ideal Transfer Characteristic with Twos Complement Output Coding and 2 × V_{REF} Range

TYPICAL CONNECTION DIAGRAM

Figure 18 shows a typical connection diagram for the AD7938-6. The AGND and DGND pins are connected together at the device for good noise suppression. The V_{REFIN}/V_{REFOUT} pin is decoupled to AGND with a 0.47 µF capacitor to avoid noise pickup if the internal reference is used. Alternatively, V_{REFIN}/V_{REFOUT} can be connected to an external reference source, and in this case, the reference pin should be decoupled with a 0.1 µF capacitor. In both cases, the analog input range can either be 0 V to V_{REF} (RANGE bit = 0) or 0 V to 2 × V_{REF} (RANGE bit = 1). The analog input configuration can be either eight single-ended inputs, four differential pairs, four pseudo-differential pairs, or seven pseudo-differential inputs (see Table 8). The V_{DD} pin is connected to either a 3 V or 5 V supply. The voltage applied to the V_{DRIVE} input controls the voltage of the digital interface and here, it is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see the Digital Inputs section).

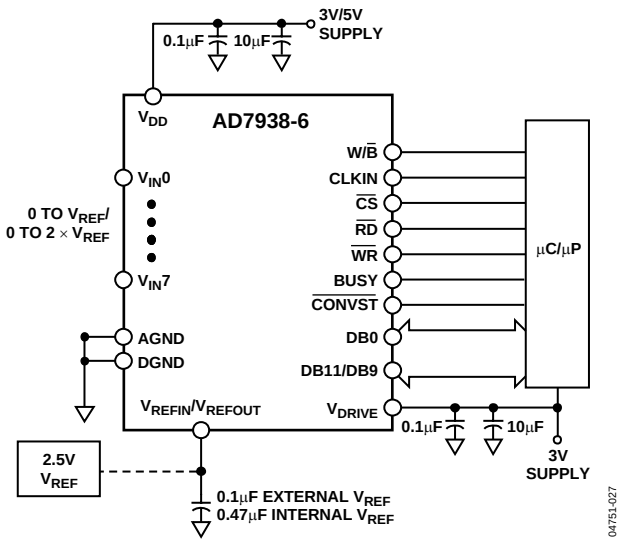


Figure 18. Typical Connection Diagram

ANALOG INPUT STRUCTURE

Figure 19 shows the equivalent circuit of the analog input structure of the AD7938-6 in differential/pseudo differential mode. In single-ended mode, V_{IN-} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 19 are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC's sampling capacitors and have a capacitance of 40 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

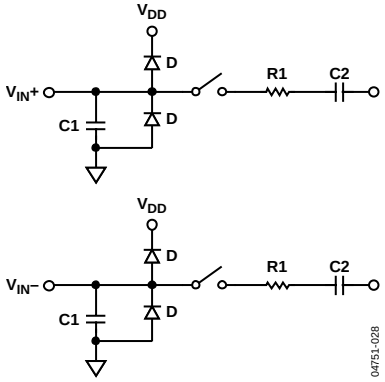


Figure 19. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 20 and Figure 21 show a graph of the THD vs. source impedance with a 50 kHz input tone for both V_{DD} = 5 V and 3 V in single-ended mode and differential mode, respectively.

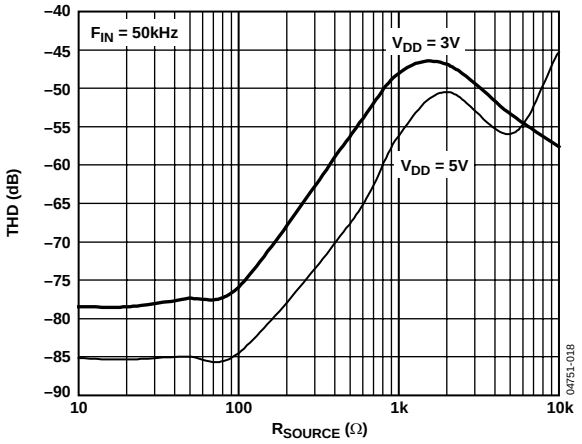


Figure 20. THD vs. Source Impedance in Single-Ended Mode

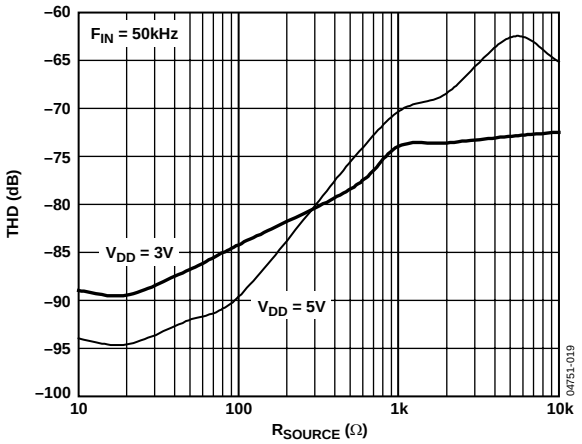


Figure 21. THD vs. Source Impedance in Differential Mode

Figure 22 shows a graph of the THD vs. the analog input frequency for various supplies while sampling at 625 kHz with an SCLK of 10 MHz. In this case, the source impedance is 10 Ω.

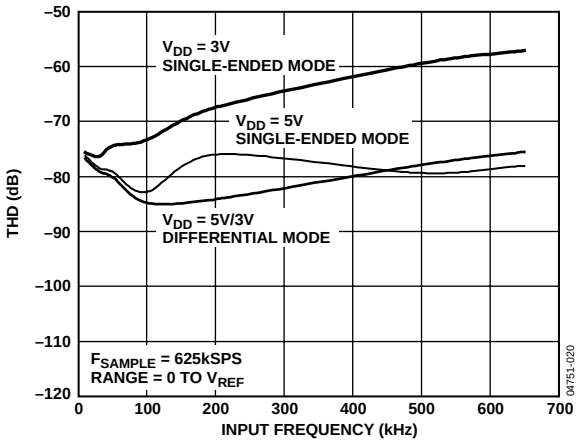


Figure 22. THD vs. Analog Input Frequency for Various Supply Voltages

ANALOG INPUTS

The AD7938-6 has software selectable analog input configurations. The user can choose either eight single-ended inputs, four fully differential pairs, four pseudo-differential pairs, or seven pseudo-differential inputs. The analog input configuration is chosen by setting the MODE0/MODE1 bits in the internal control register (see Table 8).

Single-Ended Mode

The AD7938-6 can have eight single-ended analog input channels by setting the MODE0 and MODE1 bits in the control register to 0. In applications where the signal source has a high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to $2 \times V_{REF}$.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it the correct format for the ADC.

Figure 23 shows a typical connection diagram when operating the ADC in single-ended mode.

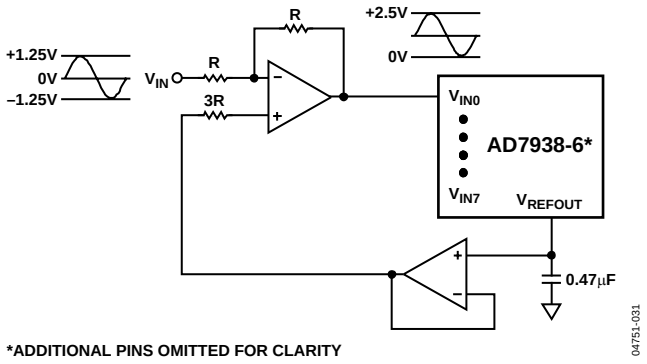


Figure 23. Single-Ended Mode Connection Diagram

Differential Mode

The AD7938-6 can have four differential analog input pairs by setting the MODE0 and MODE1 bits in the control register to 0 and 1, respectively.

Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 24 defines the fully differential analog input of the AD7938-6.

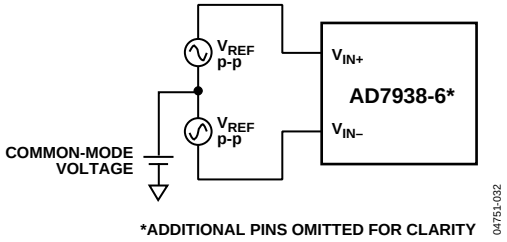


Figure 24. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (i.e., $V_{IN+} - V_{IN-}$). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} (or $2 \times V_{REF}$ depending on the range chosen) that are 180° out of phase (assuming the 0 to V_{REF} range is selected). The amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ peak-to-peak (i.e., $2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e. $(V_{IN+} + V_{IN-})/2$ and is therefore the voltage on which the two inputs are centered. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally and its range varies with the reference value V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 25 and Figure 26 show how the common-mode range typically varies with V_{REF} for a 5 V power supply using the 0 to V_{REF} range or $2 \times V_{REF}$ range, respectively. The common mode must be in this range to guarantee the functionality of the AD7938-6.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to the digital codes of 0 to 4096. If the $2 \times V_{REF}$ range is used then the input signal amplitude would extend from $-2V_{REF}$ to $+2V_{REF}$ after conversion.

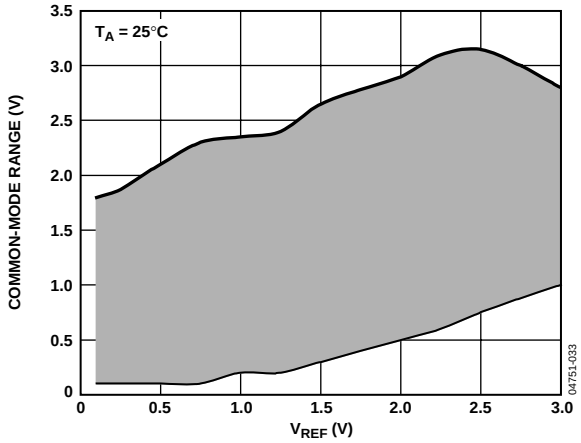


Figure 25. Input Common-Mode Range vs. V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

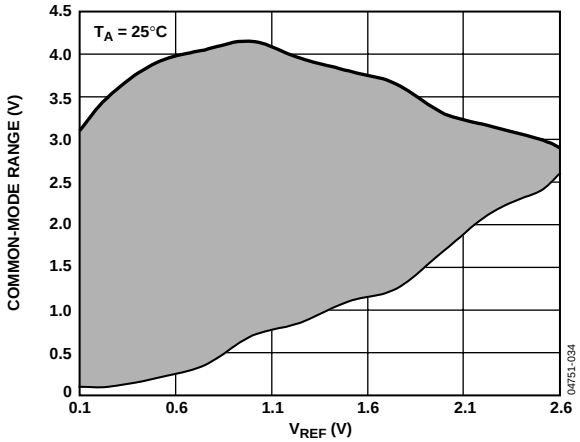


Figure 26. Input Common-Mode Range vs. V_{REF} ($2 \times V_{REF}$ Range, V_{DD} = 5 V)

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range that is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7938-6. The circuit configurations shown in Figure 27 and Figure 28 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. A suitable dual op amp that could be used in this configuration to provide differential drive to the AD7938-6 is the AD8022.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 27 and Figure 28 are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 27 converts a unipolar, single-ended signal into a differential signal.

The differential op amp driver circuit in Figure 28 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

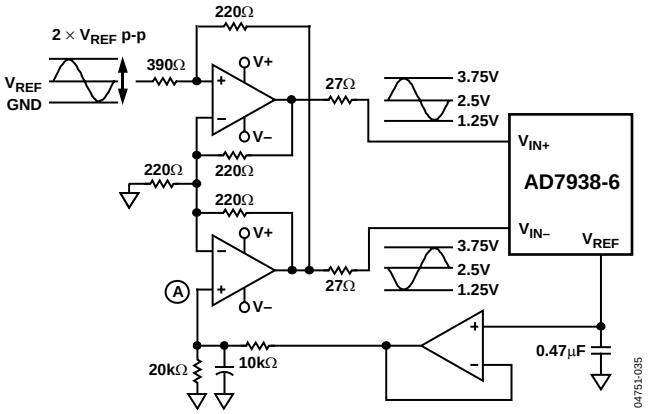


Figure 27. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

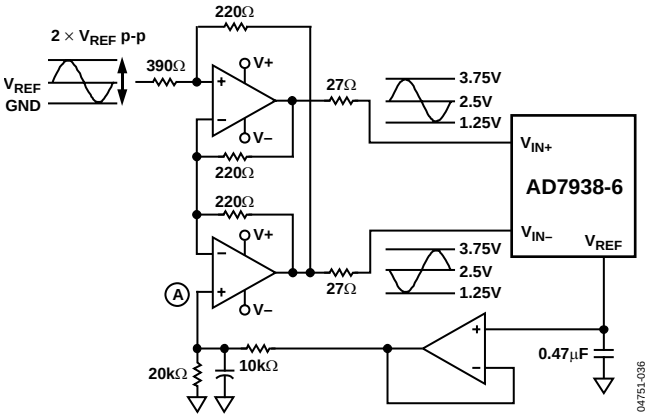


Figure 28. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

Pseudo-Differential Mode

The AD7938-6 can have four pseudo-differential pairs (Pseudo Mode 1) or seven pseudo differential inputs (Pseudo Mode 2) by setting the MODE0 and MODE1 bits in the control register to 1, 0 and 1, 1, respectively. In the case of the four pseudo-differential pairs, $V_{IN}+$ is connected to the signal source which must have an amplitude of V_{REF} (or $2 \times V_{REF}$ depending on the range chosen) to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. In the case of the seven pseudo-differential inputs, the seven analog input signals inputs are referred to a dc voltage applied to $V_{IN}7$. The benefit of pseudo-differential inputs is that they separate the analog input signal ground from the ADC's ground allowing dc common-mode voltages to be cancelled. The specified voltage range for the V_{IN-} pin while in pseudo-differential mode is −0.1 V to +0.4 V; however, typically this range can extend to −0.3 V to +0.7 V when V_{DD} = 3 V or −0.3 V to +1.8 V when V_{DD} = 5 V. Figure 29 shows a connection diagram for pseudo-differential mode.

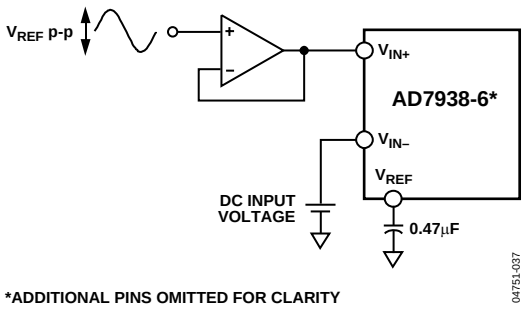


Figure 29. Pseudo-Differential Mode Connection Diagram

ANALOG INPUT SELECTION

As shown in Table 8, the user can set up their analog input configuration by setting the values in the MODE0 and MODE1 bits in the control register. Assuming the configuration has been chosen, there are different ways of selecting the analog input to be converted depending on the state of the SEQ and SHDW bits in the control register.

Traditional Multichannel Operation (SEQ = SHDW = 0)

Any one of eight analog input channels or four pairs of channels may be selected for conversion in any order by setting the SEQ and SHDW bits in the control register to 0. The channel to be converted is selected by writing to the address bits, ADD2 to ADD0, in the control register to program the multiplexer prior to the conversion. This mode of operation is that of a traditional multichannel ADC where each data write selects the next channel for conversion. Figure 30 shows a flow chart of this mode of operation. The channel configurations are shown in Table 8.

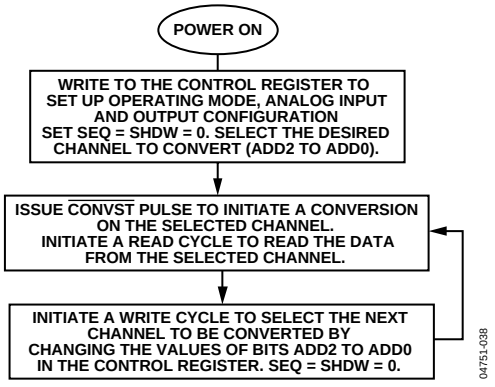


Figure 30. Traditional Multichannel Operation Flow Chart

Using the Sequencer: Programmable Sequence (SEQ = 0, SHDW = 1)

The AD7938-6 may be configured to automatically cycle through a number of selected channels using the on-chip programmable sequencer by setting SEQ = 0 and SHDW = 1 in the control register. The analog input channels to be converted are selected by setting the relevant bits in the shadow register to 1, see Table 10.

Once the shadow register has been programmed with the required sequence, the next conversion executed is on the lowest channel programmed in the SHDW register. The next conversion executed is on the next highest channel in the sequence and so on. When the last channel in the sequence is converted, the internal multiplexer returns to the first channel selected in the shadow register and commences the sequence again.

It is not necessary to write to the control register again once a sequencer operation has been initiated. The $\overline{WR}$ input must be kept high to ensure that the control register is not accidentally overwritten or that a sequence operation is not interrupted. If the control register is written to at any time during the sequence, then ensure that the SEQ and SHDW bits are set to 1, 0 to avoid interrupting the conversion sequence. The sequence program remains in force until such time as the AD7938-6 is written to and the SEQ and SHDW bits are configured with any bit combination except 1, 0. Figure 31 shows a flow chart of the programmable sequence operation.

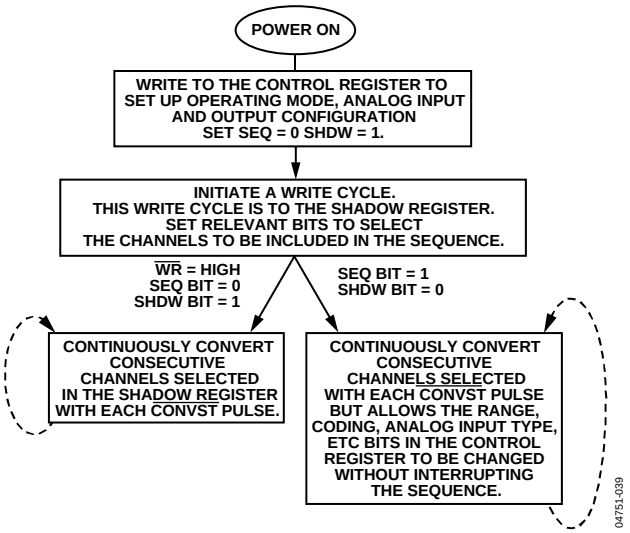


Figure 31. Programmable Sequence Flow Chart

Consecutive Sequence (SEQ = 1, SHDW = 1)

A sequence of consecutive channels can be converted beginning with Channel 0 and ending with a final channel selected by writing to the ADD2 to ADD0 bits in the control register. This is done by setting the SEQ and SHDW bits in the control register to 1. In this mode, the sequencer can be used without having to write to the shadow register. Once the control register is written to, to set this mode up, the next conversion is on Channel 0, then Channel 1, and so on until the channel selected by the address bits (ADD2 to ADD0) is reached. The cycle begins again provided the $\overline{WR}$ input is tied high. If low, the SEQ and SHDW bits must be set to 1, 0 to allow the ADC to continue its preprogrammed sequence uninterrupted. Figure 32 shows the flow chart of the consecutive sequence mode.

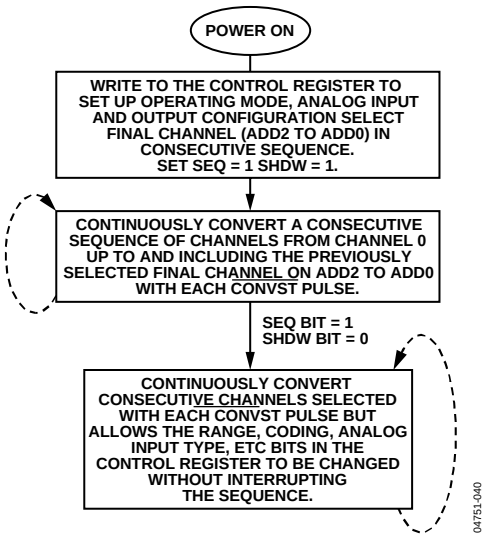


Figure 32. Consecutive Sequence Mode Flow Chart

REFERENCE SECTION

The AD7938-6 can operate with either the on-chip or external reference. The internal reference is selected by setting the REF bit in the internal control register to 1. A block diagram of the internal reference circuitry is shown in Figure 33. The internal reference circuitry includes an on-chip 2.5 V band gap reference and a reference buffer. When using the internal reference, the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.47 μF capacitor. This internal reference not only provides the reference for the analog-to-digital conversion, but it can also be used externally in the system. It is recommended that the reference output is buffered using an external precision op amp before applying it anywhere in the system.

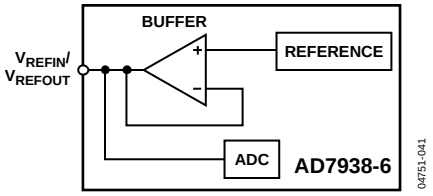


Figure 33. Internal Reference Circuit Block Diagram

Alternatively, an external reference can be applied to the V_{REFIN}/V_{REFOUT} pin of the AD7938-6. An external reference input is selected by setting the REF bit in the internal control register to 0. The external reference input range is 0.1 V to V_{DD}. It is important to ensure that, when choosing the reference value, the maximum analog input range ($V_{IN\ MAX}$) is never greater than V_{DD} + 0.3 V to comply with the maximum ratings of the device. For example, if operating in differential mode and the reference is sourced from V_{DD}, then the 0 to 2 × V_{REF} range cannot be used. This is because the analog input signal range would now extend to 2 × V_{DD}, which would exceed maximum rating conditions. In the pseudo-differential modes, the user must

ensure that $V_{REF} + (V_{IN-}) \leq V_{DD}$ when using the 0 to V_{REF} range, or when using the $2 \times V_{REF}$ range that $2 \times V_{REF} + (V_{IN-}) \leq V_{DD}$.

In all cases, the specified reference is 2.5 V.

The performance of the part with different reference values is shown in Figure 9 to Figure 11. The value of the reference sets the analog input span and the common-mode voltage range. Errors in the reference source result in gain errors in the AD7938-6 transfer function and add to specified full-scale errors on the part.

Table 11 lists examples of suitable voltage references that could be used that are available from Analog Devices and Figure 34 shows a typical connection diagram for an external reference.

Table 11. Examples of Suitable Voltage References

Reference	Output Voltage	Initial Accuracy (% Max)	Operating Current (μA)
AD780	2.5/3	0.04	1000
ADR421	2.5	0.04	500
ADR420	2.048	0.05	500

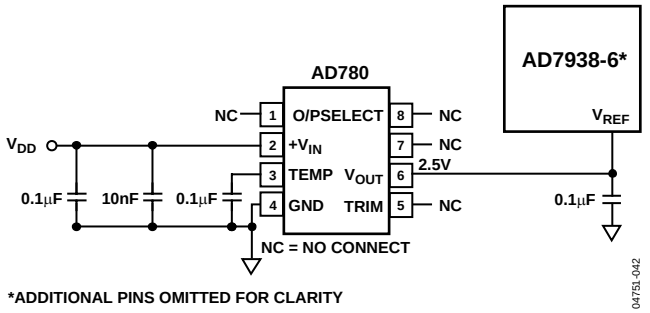


Figure 34. Typical V_{REF} Connection Diagram

Digital Inputs

The digital inputs applied to the AD7938-6 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the AV_{DD} + 0.3 V limit as on the analog inputs.

Another advantage of the digital inputs not being restricted by the AV_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If any of these inputs are applied before AV_{DD}, then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to AV_{DD}.

V_{DRIVE} Input

The AD7938-6 has a V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the parallel interface operates. V_{DRIVE} allows the ADC to easily interface to 3 V and 5 V processors.

For example, if the AD7938-6 is operated with an AV_{DD} of 5 V and the V_{DRIVE} pin is powered from a 3 V supply, the AD7938-6 has better dynamic performance with an AV_{DD} of 5 V while still being able to interface directly to 3 V processors. Care should be taken to ensure V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

PARALLEL INTERFACE

The AD7938-6 has a flexible, high speed, parallel interface. This interface is 12-bits wide and is capable of operating in either word (W/$\overline{B}$ tied high) or byte (W/$\overline{B}$ tied low) mode. The $\overline{CONVST}$ signal is used to initiate conversions and when operating in autoshutdown or autostandby mode, it is used to initiate power up.

A falling edge on the $\overline{CONVST}$ signal is used to initiate conversions and it also puts the ADC track-and-hold into track. Once the $\overline{CONVST}$ signal goes low, the BUSY signal goes high for the duration of the conversion. In between conversions, $\overline{CONVST}$ must be brought high for a minimum time of t_1. This must happen after the 14th falling edge of CLKIN; otherwise, the conversion is aborted and the track-and-hold goes back into track. At the end of the conversion, BUSY goes low and can be used to activate an interrupt service routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated in parallel to read the 12 bits of conversion data. When power supplies are first applied to the device, a rising edge on $\overline{CONVST}$ is necessary to put the track-and-hold into track. The acquisition time of 125 ns minimum must be allowed before $\overline{CONVST}$ is brought low to initiate a conversion. The ADC then goes into hold on the falling edge of $\overline{CONVST}$ and back into track on the 13th rising edge of CLKIN after this (see Figure 35). When operating the device in autoshutdown or autostandby mode, where the ADC powers down at the end of each conversion, a rising edge on the $\overline{CONVST}$ signal is used to power up the device.

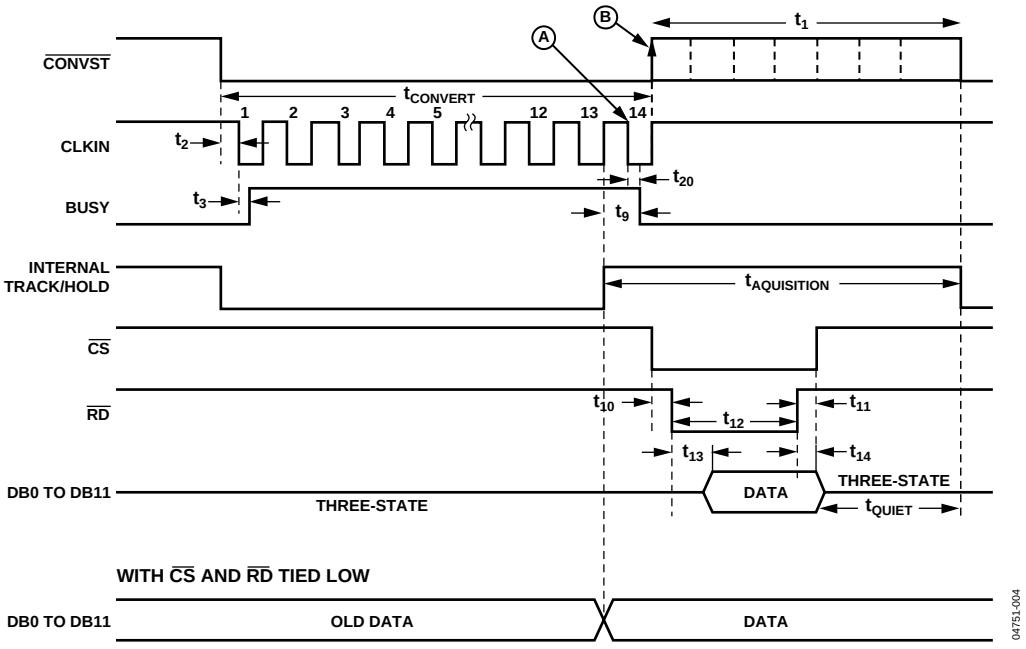


Figure 35. AD7938-6 Parallel Interface—Conversion and Read Cycle in Word Mode (W/$\overline{B}$ = 1)

Reading Data from the AD7938-6

With the W/$\overline{B}$ pin tied logic high, the AD7938-6 interface operates in word mode. In this case, a single read operation from the device accesses the conversion data-word on Pins DB0 to DB11. The DB8/HBEN pin assumes its DB8 function. With the W/$\overline{B}$ pin tied to logic low, the AD7938-6 interface operates in byte mode. In this case, the DB8/HBEN pin assumes its HBEN function. Conversion data from the AD7938-6 must be accessed in two read operations with eight bits of data provided on DB0 to DB7 for each of the read operations. The HBEN pin determines whether the read operation accesses the high byte or the low byte of the12-bit word. For a low byte read, DB0 to DB7 provide the eight LSBs of the 12-bit word. For a high byte read, DB0 to DB3 provide the four MSBs of the 12-bit word. DB5 to DB7 of the high byte provide the Channel ID. Figure 35 shows the read cycle timing diagram for a 12-bit transfer. When operated in word mode, the HBEN input does not exist, and only the first read operation is required to access data from the device. When operated in byte mode, the two read cycles shown in Figure 36 are required to access the full data-word from the device.

The $\overline{CS}$ and $\overline{RD}$ signals are gated internally and level triggered active low. In either word mode or byte mode, $\overline{CS}$ and $\overline{RD}$ may be tied together as the timing specifications for t_{10} and t_{11} are 0 ns minimum. This would mean the bus would be constantly driven by the AD7938-6.

The data is placed onto the data bus a time, t_{13}, after both $\overline{CS}$ and $\overline{RD}$ go low. The $\overline{RD}$ rising edge can be used to latch data out of the device. After a time, t_{14}, the data lines become three-stated.

Alternatively, $\overline{CS}$ and $\overline{RD}$ can be tied permanently low and the conversion data is valid and placed onto the data bus a time, t_9, before the falling edge of BUSY.

Note that if $\overline{RD}$ is pulsed during the conversion time then this causes a degradation in linearity performance of approximately 0.25 LSB. Reading during conversion by way of tying $\overline{CS}$ and $\overline{RD}$ low does not cause any degradation.

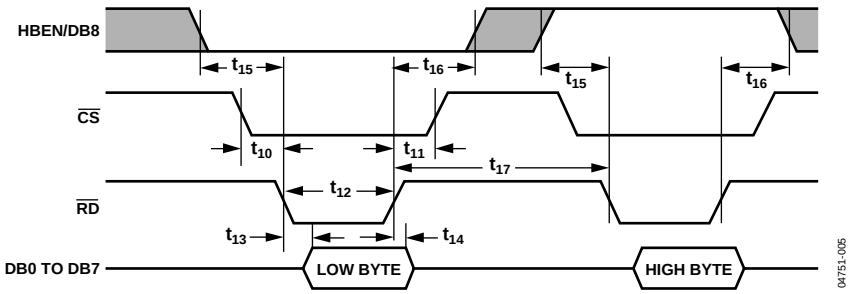


Figure 36. AD7938-6 Parallel Interface—Read Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

Writing Data to the AD7938-6

With W/$\overline{B}$ tied logic high, a single write operation transfers the full data-word on DB0 to DB11 to the control register on the AD7938-6. The DB8/HBEN pin assumes its DB8 function. Data written to the AD7938-6 should be provided on the DB0 to DB11 inputs with DB0 being the LSB of the data-word. With W/$\overline{B}$ tied logic low, the AD7938-6 requires two write operations to transfer a full 12-bit word. DB8/HBEN assumes its HBEN function. Data written to the AD7938-6 should be provided on the DB0 to DB7 inputs. HBEN determines whether the byte written is high byte or low byte data. The low byte of the data-word should be written first with DB0 being the LSB of the full data-word. For the high byte write, HBEN should be high and the data on the DB0 input should be data Bit 8 of the 12-bit word. In both word and byte mode, a single write operation to the shadow register is always sufficient since it is only 8-bits wide.

Figure 37 shows the write cycle timing diagram of the AD7938-6. When operated in word mode, the HBEN input does not exist and only one write operation is required to write the word of data to the device. Data should be provided on DB0 to DB11. When operated in byte mode, the two write cycles shown in Figure 38 are required to write the full data-word to the AD7938-6. In Figure 38, the first write transfers the lower eight bits of the data-word from DB0 to DB7, and the second write transfers the upper four bits of the data-word. When writing to the AD7938-6, the top four bits in the high byte must be 0s.

The data is latched into the device on the rising edge of $\overline{WR}$. The data needs to be setup a time, t_7, before the $\overline{WR}$ rising edge and held for a time, t_8, after the $\overline{WR}$ rising edge. The $\overline{CS}$ and $\overline{WR}$ signals are gated internally. $\overline{CS}$ and $\overline{WR}$ may be tied together as the timing specifications for t_4 and t_5 are 0 ns minimum (assuming $\overline{CS}$ and $\overline{RD}$ have not already been tied together).

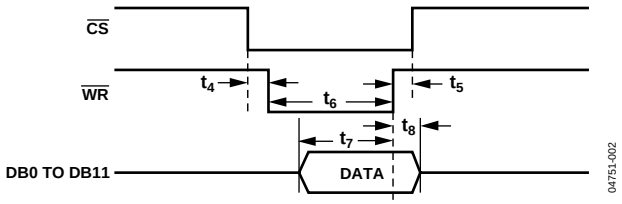


Figure 37. AD7938-6 Parallel Interface—Write Cycle Timing for Word Mode Operation (W/$\overline{B}$ = 1)

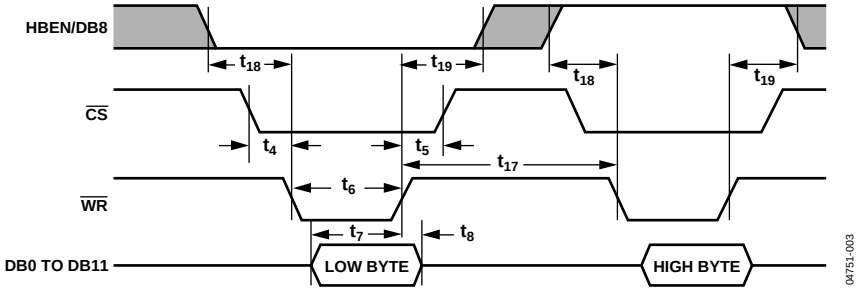


Figure 38. AD7938-6 Parallel Interface—Write Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

POWER MODES OF OPERATION

The AD7938-6 have four different power modes of operation. These modes are designed to provide flexible power management options. Different options can be chosen to optimize the power dissipation/throughput rate ratio for differing applications. The mode of operation is selected by the power management bits, PM1 and PM0, in the control register, as detailed in Table 7. When power is first applied to the AD7938-6 an on-chip, power-on reset circuit ensures that the default power-up condition is normal mode.

Note that, after power-on, the track-and-hold is in hold mode and the first rising edge of $\overline{\text{CONVST}}$ places the track-and-hold into track mode.

Normal Mode (PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times associated with the AD7938-6 because it remains fully powered up at all times. At power-on reset, this mode is the default setting in the control register.

Autoshutdown (PM1 = 0; PM0 = 1)

In this mode of operation, the AD7938-6 automatically enters full shutdown at the end of each conversion, which is shown at Point A in Figure 35 and Figure 39. In shutdown mode, all internal circuitry on the device is powered down. The part retains information in the control register during shutdown. The track-and-hold also goes into hold at this point and remains in hold as long as the device is in shutdown. The AD7938-6 remains in shutdown mode until the next rising edge of $\overline{\text{CONVST}}$ (see Point B in Figure 35 or Figure 39). In order to keep the device in shutdown for as long as possible, $\overline{\text{CONVST}}$ should idle low between conversions as shown in Figure 39. On this rising edge, the part begins to power-up and the track-and-hold returns to track mode. The power-up time required is 10 ms minimum regardless of whether the user is operating with the internal or external reference. The user should ensure that the power-up time has elapsed before initiating a conversion.

Autostandby (PM1 = 1; PM0 = 0)

In this mode of operation, the AD7938-6 automatically enters standby mode at the end of each conversion, which is shown as Point A in Figure 35. When this mode is entered, all circuitry on the AD7938-6 is powered down except for the reference and reference buffer. The track-and-hold goes into hold at this point also and remains in hold as long as the device is in standby. The part remains in standby until the next rising edge of $\overline{\text{CONVST}}$ powers up the device. The power-up time required depends on whether the internal or external reference is used. With an external reference, the power-up time required is a minimum of 600 ns, while when using the internal reference, the power-up time required is a minimum of 7 μs. The user should ensure this power-up time has elapsed before initiating another conversion as shown in Figure 39. This rising edge of $\overline{\text{CONVST}}$ also places the track-and-hold back into track mode.

Full Shutdown Mode (PM1 =1; PM0 = 1)

When this mode is programmed, all circuitry on the AD7938-6 is powered down upon completion of the write operation, i.e., on rising edge of $\overline{\text{WR}}$. The track-and-hold enters hold mode at this point. The part retains the information in the control register while the part is in shutdown. The AD7938-6 remains in full shutdown mode and the track-and-hold in hold mode, until the power management bits (PM1 and PM0) in the control register are changed. If a write to the control register occurs while the part is in full shutdown mode, and the power management bits are changed to PM0 = PM1 = 0, i.e., normal mode, the part begins to power-up on the $\overline{\text{WR}}$ rising edge and the track-and-hold returns to track. To ensure the part is fully powered up before a conversion is initiated, the power-up time of 10 ms minimum should be allowed before the next $\overline{\text{CONVST}}$ falling edge; otherwise, invalid data is read.

Note that all power-up times quoted apply with a 470 nF capacitor on the V_{REFIN} pin.

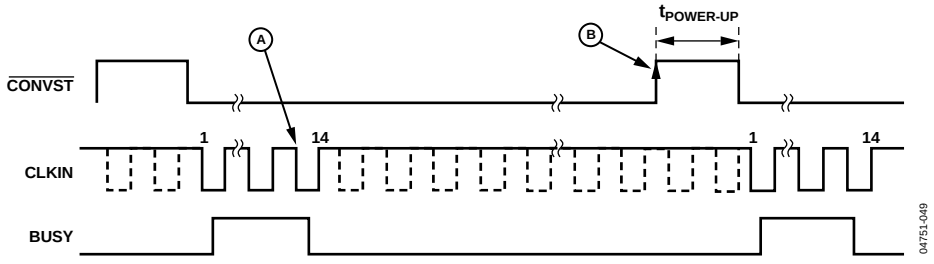


Figure 39. Autoshutdown/Autostandby Mode

POWER VS. THROUGHPUT RATE

A big advantage of powering the ADC down after a conversion is that the power consumption of the part is significantly reduced at lower throughput rates. When using the different power modes, the AD7938-6 is only powered up for the duration of the conversion. Therefore, the average power consumption per cycle is significantly reduced. Figure 40 shows a plot of the power vs. the throughput rate when operating in autostandby mode for both V_{DD} = 5 V and 3 V. For example, if the maximum CLKIN frequency of 10 MHz is used to minimize the conversion time, this accounts for only 1.315 µs of the overall cycle time while the AD7938-6 remains in standby mode for the remainder of the cycle. If the device runs at a throughput rate of 10 kSPS, for example, then the overall cycle time would be 100 µs.

Figure 41 shows a plot of the power vs. the throughput rate when operating in normal mode for both VDD = 5 V and 3 V. In both plots, the figures apply when using the internal reference. If an external reference is used, the power-up time reduces to 600 ns; therefore, the AD7938-6 remains in standby for a greater time in every cycle. Additionally, the current consumption, when converting, should be lower than the specified maximum of 1.5 mA or 1.2 mA with VDD = 5 V or 3 V, respectively.

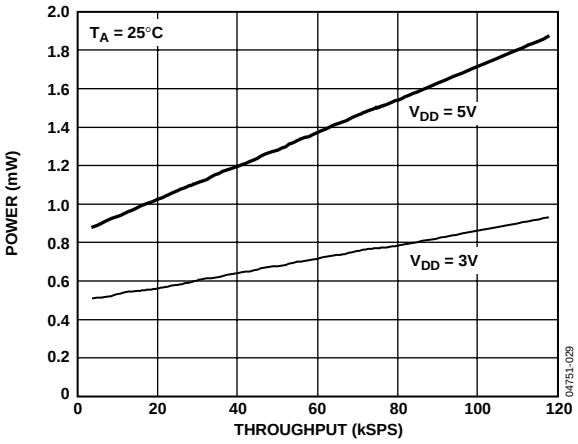


Figure 40. Power vs. Throughput in Autostandby Mode Using Internal Reference

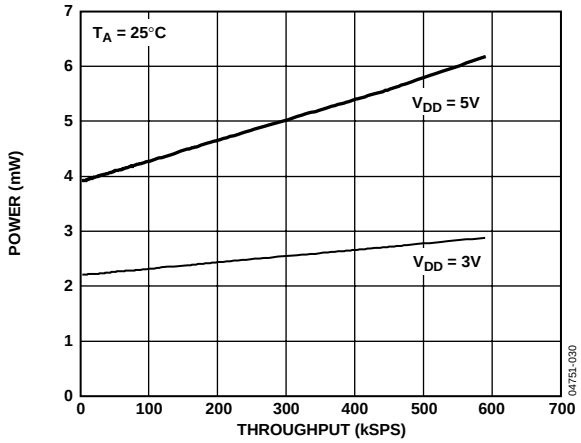


Figure 41. Power vs. Throughput in Normal Mode Using Internal Reference

MICROPROCESSOR INTERFACING

AD7938-6 to ADSP-21xx Interface

Figure 42 shows the AD7938-6 interfaced to the ADSP-21xx series of DSPs as a memory mapped device. A single wait state may be necessary to interface the AD7938-6 to the ADSP-21xx depending on the clock speed of the DSP. The wait state can be programmed via the data memory wait state control register of the ADSP-21xx (see the ADSP-21xx family User's Manual for details). The following instruction reads from the AD7938-6:

MR = DM (ADC)

where *ADC* is the address of the AD7938-6.

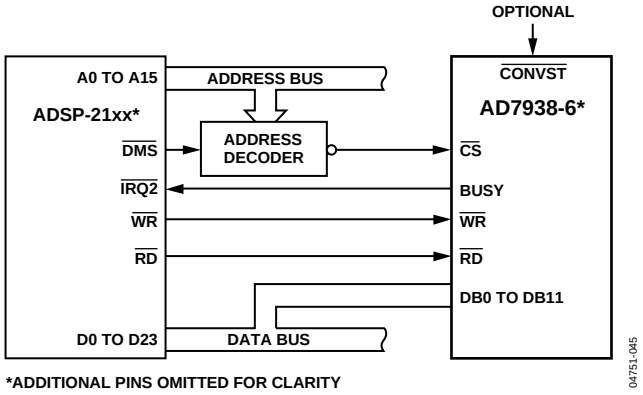
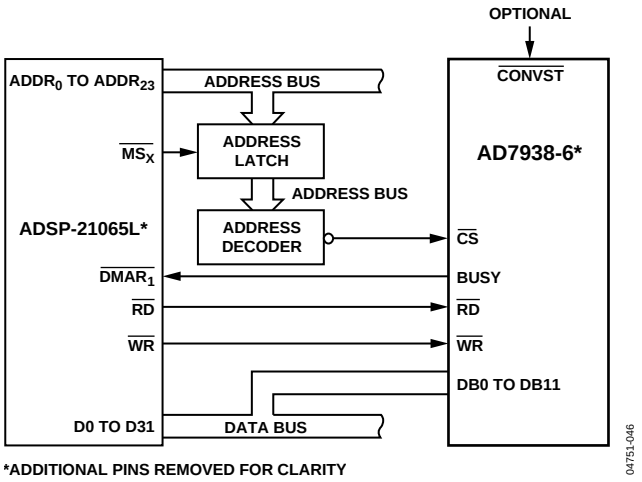


Figure 42. Interfacing to the ADSP-21xx

AD7938-6 to ADSP-21065L Interface

Figure 43 shows a typical interface between the AD7938-6 and the ADSP-21065L SHARC® processor. This interface is an example of one of three DMA handshake modes. The $\overline{MS_x}$ control line is actually three memory select lines. Internal $ADDR_{25-24}$ are decoded into $\overline{MS_{3-0}}$, these lines are then asserted as chip selects. The $\overline{DMAR_1}$ (DMA request 1) is used in this setup as the interrupt to signal the end of conversion. The rest of the interface is standard handshaking operation.



*ADDITIONAL PINS REMOVED FOR CLARITY

Figure 43. Interfacing to the ADSP-21065L

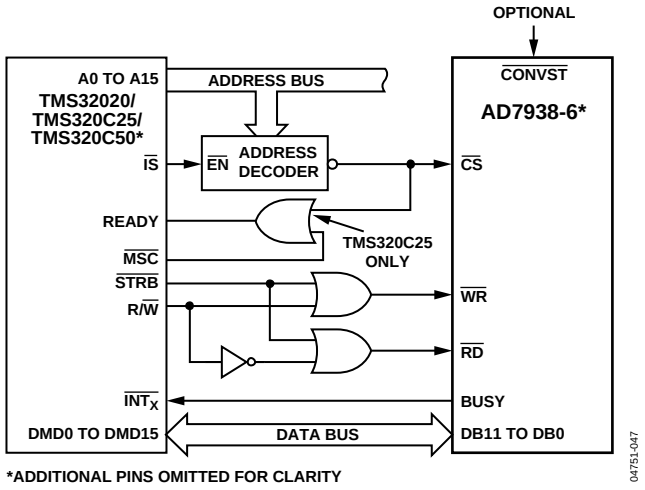
AD7938-6 to TMS32020, TMS320C25, and TMS320C5x Interface

Parallel interfaces between the AD7938-6 and the TMS32020, TMS320C25, and TMS320C5x family of DSPs are shown in Figure 44. The memory mapped address chosen for the AD7938-6 should be chosen to fall in the I/O memory space of the DSPs. The parallel interface on the AD7938-6 is fast enough to interface to the TMS32020 with no extra wait states. If high speed glue logic, such as 74AS devices, are used to drive the $\overline{RD}$ and the $\overline{WR}$ lines when interfacing to the TMS320C25, then again, no wait states are necessary. However, if slower logic is used, data accesses may be slowed sufficiently when reading from, and writing to, the part to require the insertion of one wait state. Extra wait states are necessary when using the TMS320C5x at their fastest clock speeds (see the TMS320C5x User's Guide for details).

Data is read from the ADC using the following instruction

IN D, ADC

where *D* is the data memory address and *ADC* is the AD7938-6 address.

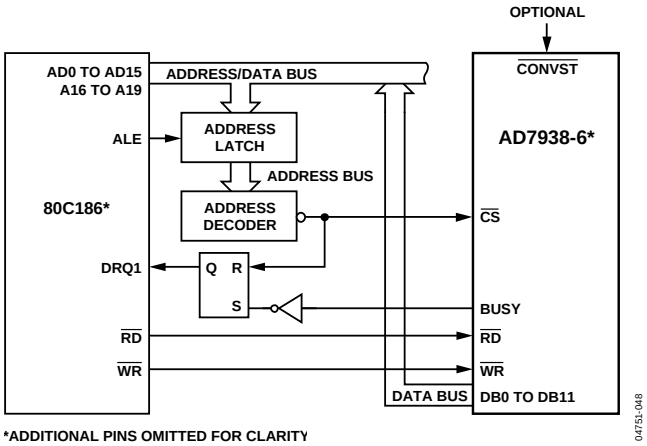


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 44. Interfacing to the TMS32020/C25/C5x

AD7938-6 to 80C186 Interface

Figure 45 shows the AD7938-6 interfaced to the 80C186 microprocessor. The 80C186 DMA controller provides two independent high speed DMA channels where data transfer can occur between memory and I/O spaces. Each data transfer consumes two bus cycles, one cycle to fetch data and the other to store data. After the AD7938-6 has finished a conversion, the BUSY line generates a DMA request to Channel 1 (DRQ1). Because of the interrupt, the processor performs a DMA read operation that also resets the interrupt latch. Sufficient priority must be assigned to the DMA channel to ensure that the DMA request is serviced before the completion of the next conversion.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 45. Interfacing to the 80C186

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7938-6 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the ground pins on the AD7938-6 as possible. Avoid running digital lines under the device as this couples noise onto the die. The analog ground plane should be allowed to run under the AD7938-6 to avoid noise coupling. The power supply lines to the AD7938-6 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 μF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-32) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided. Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

EVALUATING THE AD7938-6 PERFORMANCE

The recommended layout for the AD7938-6 is outlined in the evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7938-6 evaluation board, as well as many other ADI evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7938-6.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7938-6. The software and documentation are on the CD that ships with the evaluation board.

OUTLINE DIMENSIONS

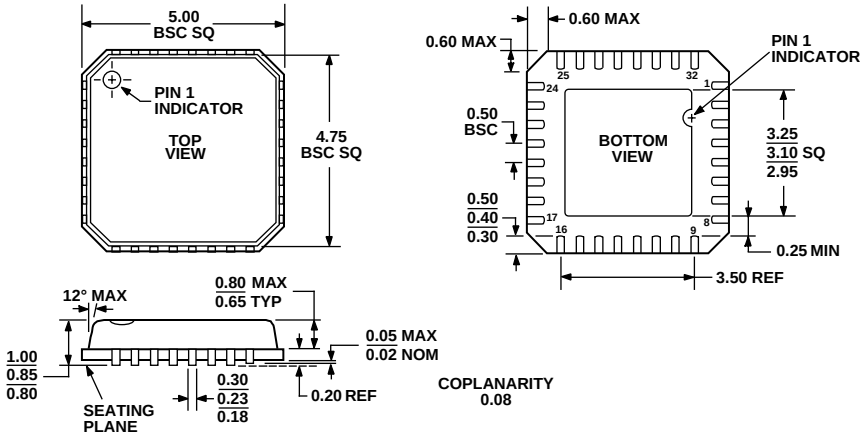


Figure 46. 32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32-2)
Dimensions shown in millimeters

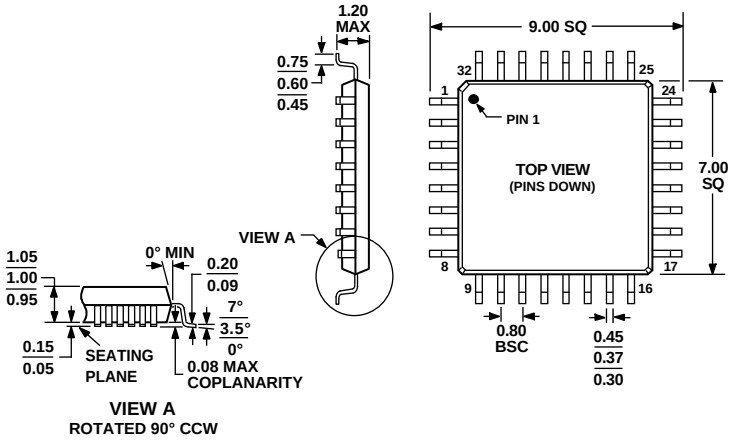


Figure 47. 32-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Descriptions	Package Option
AD7938BCP-6	–40°C to +85°C	±1	32-Lead LFCSP	CP-32-2
AD7938BCP-6REEL7	–40°C to +85°C	±1	32-Lead LFCSP	CP-32-2
AD7938BCPZ-6[2]	–40°C to +85°C	±1	32-Lead LFCSP	CP-32-2
AD7938BCPZ-6REEL7[2]	–40°C to +85°C	±1	32-Lead LFCSP	CP-32-2
AD7938BSU-6	–40°C to +85°C	±1	32-Lead TQFP	SU-32-2
AD7938BSU-6REEL	–40°C to +85°C	±1	32-Lead TQFP	SU-32-2
AD7938BSU-6REEL7	–40°C to +85°C	±1	32-Lead TQFP	SU-32-2
AD7938BSUZ-6[2]	–40°C to +85°C	±1	32-Lead TQFP	SU-32-2
AD7938BSUZ-6REEL7[2]	–40°C to +85°C	±1	32-Lead TQFP	SU-32-2
EVAL-AD7938-6CB[3]			Evaluation Board	
EVAL-CONTROL BRD2[4]			Controller Board	

[1] Linearity error here refers to integral linearity error.
[2] Z = Pb-free part.
[3] This can be used as a standalone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[4] Evaluation Board Controller. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. The following needs to be ordered to obtain a complete evaluation kit: the ADC Evaluation Board (e.g. EVAL-AD7938-6CB), the EVAL-CONTROL BRD2 and a 12 V ac transformer. See relevant evaluation board technical note for more details.

NOTES

NOTES

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