

# SLIC-E / TSLIC-E

Subscriber Line Interface Circuit Enhanced Feature Set

SLIC-E (PEF 4265), Version 2.1

SLIC-E2 (PEF 4265-2), Version 2.1

TSLIC-E (PEF 4365), Version 2.1

Preliminary  
**Data Sheet**

Revision 2.0

Communication Solutions



Never stop thinking

**Edition 2006-10-10**

**Published by  
Infineon Technologies AG  
81726 München, Germany**

**© Infineon Technologies AG 2006.  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

---

**SLIC-E / TSLIC-E Subscriber Line Interface Circuit Enhanced Feature Set**


---

**Revision History: 2006-10-10, Revision 2.0**
**Previous Version: Revision 1.0**

| Page           | Subjects (major changes since last revision)                                               |
|----------------|--------------------------------------------------------------------------------------------|
| all            | Package P-/PG-VQFN-48-4 changed to PG-VQFN-48-15                                           |
| all            | Package P-/PG-DSO-20-24 changed to PG-DSO-20-24                                            |
| all            | Package P-/PG-DSO-36-10 changed to PG-DSO-36-15                                            |
| <b>Page 36</b> | <b>"Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package" on Page 36</b> modified. |
|                |                                                                                            |
|                |                                                                                            |
|                |                                                                                            |
|                |                                                                                            |
|                |                                                                                            |
|                |                                                                                            |
|                |                                                                                            |

**Trademarks**

ABM®, ACE®, AOP®, Arcofi®, ASM®, ASP®, BlueMoon®, BlueNIX®, C166®, DuSLIC®, ELIC®, Epic®, FALC®, GEMINAX®, Idec®, INCA®, IOM®, Ipat®-2, IPVD®, Isac®, Itac®, IWE®, IWORX®, M-GOLD®, MUSAC®, MuSLIC®, OCTALFALC®, OCTAT®, POTSWIRE®, QUADFALC®, QUAT®, SCOUT®, SCT®, SEROCCO®, S-GOLD®, SICAT®, SICOFI®, SIDEC®, SIEGET®, SLICOFI®, SMARTI®, SOCRATES®, VDSLite®, VINETIC®, 10BaseS® are registered trademarks of Infineon Technologies AG.

ConverGate™, DIGITAPE™, DUALFALC™, EasyPort™, S-GOLDlite™, S-GOLD2™, S-GOLD3™, VINAX™, WildPass™, 10BaseV™, 10BaseVX™ are trademarks of Infineon Technologies AG.

Microsoft® and Visio® are registered trademarks of Microsoft Corporation. Linux® is a registered trademark of Linus Torvalds. FrameMaker® is a registered trademark of Adobe Systems Incorporated. APOXI® is a registered trademark of Comneon GmbH & Co. OHG. PrimeCell®, RealView®, ARM® are registered trademarks of ARM Limited. OakDSPCore®, TeakLite® DSP Core, OCEM® are registered trademarks of ParthusCeva Inc.

IndoorGPS™, GL-20000™, GL-LN-22™ are trademarks of Global Locate. ARM926EJ-S™, ADS™, Multi-ICE™ are trademarks of ARM Limited.

## Table of Contents

|          |                                                              |    |
|----------|--------------------------------------------------------------|----|
|          | <b>Table of Contents</b>                                     | 4  |
|          | <b>List of Figures</b>                                       | 5  |
|          | <b>List of Tables</b>                                        | 6  |
| <b>1</b> | <b>General Description</b>                                   | 7  |
| 1.1      | Version 2.1: Summary of Changes                              | 7  |
| 1.2      | Features                                                     | 8  |
| 1.3      | Logic Symbol                                                 | 9  |
| 1.4      | Pin Configuration                                            | 10 |
| 1.5      | Pin Definitions and Functions                                | 12 |
| 1.6      | Functional Block Diagram                                     | 14 |
| <b>2</b> | <b>Functional Description</b>                                | 15 |
| 2.1      | Operating Modes                                              | 16 |
| 2.2      | Current Limitation / Overtemperature Protection              | 17 |
| <b>3</b> | <b>Typical Application Circuit for DuSLIC® and VINETIC®</b>  | 18 |
| <b>4</b> | <b>Electrical Characteristics</b>                            | 21 |
| 4.1      | Absolute Maximum Ratings                                     | 21 |
| 4.2      | Foreign Line Voltages                                        | 21 |
| 4.3      | Operating Range                                              | 22 |
| 4.4      | Thermal Resistances                                          | 22 |
| 4.5      | Electrical Parameters                                        | 23 |
| 4.5.1    | Supply Currents and Power Dissipation                        | 23 |
| 4.5.2    | DC Characteristics                                           | 25 |
| 4.5.3    | AC Characteristics                                           | 27 |
| 4.5.3.1  | Frequency Dependence of PSRR                                 | 29 |
| <b>5</b> | <b>Test Figures</b>                                          | 31 |
| <b>6</b> | <b>Package Outlines</b>                                      | 35 |
| 6.1      | PG-DSO-20-24 Package                                         | 35 |
| 6.2      | PG-VQFN-48-15 Package                                        | 36 |
| 6.2.1    | Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package | 36 |
| 6.3      | PG-DSO-36-15 Package                                         | 37 |
| 6.3.1    | Recommended PCB Foot Print Pattern for PG-DSO-36-15 Package  | 38 |
|          | <b>References</b>                                            | 39 |

## List of Figures

|           |                                                                                           |    |
|-----------|-------------------------------------------------------------------------------------------|----|
| Figure 1  | Logic Symbol PEF 4265                                                                     | 9  |
| Figure 2  | Logic Symbol PEF 4365                                                                     | 9  |
| Figure 3  | Pin Configuration PG-DSO-20-24 Package (top view)                                         | 10 |
| Figure 4  | Pin Configuration PG-VQFN-48-15 Package (top view)                                        | 10 |
| Figure 5  | Pin Configuration PG-DSO-36-15 Package (dual channel)                                     | 11 |
| Figure 6  | Block Diagram                                                                             | 14 |
| Figure 7  | Transversal and Longitudinal Line Currents                                                | 15 |
| Figure 8  | Application Circuit DuSLIC®                                                               | 19 |
| Figure 9  | Application Circuit VINETIC®                                                              | 20 |
| Figure 10 | Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR                           | 27 |
| Figure 11 | Typical Frequency Dependence of PSRR VBATH/VTR                                            | 29 |
| Figure 12 | Typical Frequency Dependence of PSRR VBATH/VTR                                            | 29 |
| Figure 13 | Typical Frequency Dependence of PSRR VHR/VTR                                              | 30 |
| Figure 14 | Typical Frequency Dependence of PSRR VDD/VTR                                              | 30 |
| Figure 15 | Output Current Limit                                                                      | 31 |
| Figure 16 | Output Resistance PDRH, PDRHL                                                             | 31 |
| Figure 17 | Current Outputs IT, IL                                                                    | 32 |
| Figure 18 | Transmission Characteristics                                                              | 32 |
| Figure 19 | Longitudinal to Transversal Rejection                                                     | 33 |
| Figure 20 | Longitudinal to Transversal Rejection Loop                                                | 33 |
| Figure 21 | Transversal to Longitudinal Rejection                                                     | 34 |
| Figure 22 | Ring Amplitude                                                                            | 34 |
| Figure 23 | Package Outline for PG-DSO-20-24 (Plastic Green Dual Small Outline)                       | 35 |
| Figure 24 | Package Outline for PG-VQFN-48-15 (Plastic Green Very thin Profile Quad Flatpack No-lead) | 36 |
| Figure 25 | Package Outline for PG-DSO-36-15 (Plastic Green Dual Small Outline)                       | 37 |
| Figure 26 | Footprint for PG-DSO-36-15                                                                | 38 |

## List of Tables

|          |                                                                                    |    |
|----------|------------------------------------------------------------------------------------|----|
| Table 1  | Pin Definitions and Functions PG-DSO-20-24 and PG-VQFN-48-15                       | 12 |
| Table 2  | Pin Definitions and Functions PG-DSO-36-15                                         | 13 |
| Table 3  | SLIC-E Mode Table                                                                  | 16 |
| Table 4  | SLIC-E Modes and Supplies                                                          | 16 |
| Table 5  | External Components DuSLIC® / VINETIC® for 2 Channels                              | 18 |
| Table 6  | Absolute Maximum Ratings                                                           | 21 |
| Table 7  | Voltage Limits on Output Pins                                                      | 21 |
| Table 8  | Current Limits on Output Pins                                                      | 22 |
| Table 9  | Operating Range                                                                    | 22 |
| Table 10 | Thermal Resistances                                                                | 22 |
| Table 11 | Supply Currents, Power Dissipation ( $I_R = I_T = 0$ ; $V_{TR} = 0$ ; one channel) | 23 |
| Table 12 | Output Stage Power Dissipation                                                     | 24 |
| Table 13 | DC Characteristics ( $V_{ACP} = V_{ACN} = 1.5 \text{ V}$ )                         | 25 |
| Table 14 | AC Characteristics                                                                 | 27 |

## **1 General Description**

Infineon Technologies' new high voltage ringing Subscriber Line Interface Circuit SLIC-E (PEF 4265 **V2.1**) is the latest out of the well-known and broadly used SLIC-E family. It has been designed not only to cover all previous SLIC-E applications, but also for particular "ADSL friendliness" and thus enables the realization of highly cost optimized integrated voice data (IVD) systems. Special effort has been put on minimizing the influence of line voltage transients and distortions caused by mode transitions and the associated unavoidable impedance changes.

As SLIC-E V2.1 is pin compatible with its previous versions, it can be operated with all codec devices of the DuSLIC® or VINETIC® chip sets. The highly flexible device offers 3.3 V compatibility and integrated balanced ringing up to 85 V<sub>rms</sub>. Integrated supply switches allow the choice between two negative battery voltages for voice transmission, whereas in the ring mode an additional positive supply voltage is used.

To minimize the average system power dissipation, a power-down mode can be utilized; the transmission part is switched off completely and off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

SLIC-E V2.1 is available in a single (PEF 4265) channel version in either PG-DSO-20-24 or PG-VQFN-48-15 power packages, or in a dual channel version (PEF 4365), packaged in PG-DSO-36-15.

### **1.1 Version 2.1: Summary of Changes**

Compared with the previous version of SLIC-E, PEF 4265 V1.2, the new version V2.1 is characterized by the following changes:

- Improved high-frequency noise and distortion performance
- Optimized mode transitions to minimize influence on ADSL data in IVD systems
- Compatible with both 3.3 and 5 V VDD supplies
- High impedance DC inputs
- Fully differential receive path - VCMS pin not required
- Fast current limitation for improved overvoltage behaviour
- Application circuit:
  - 100 nF / 50 V capacitor at CEXT
  - Per channel series diode in VBATL supply mandatory (no shared diodes)



**Subscriber Line Interface Circuit Enhanced Feature Set**  
**SLIC-E**  
**SLIC-E2**  
**TSLIC-E**

**PEF 4265**  
**PEF 4265-2**  
**PEF 4365**

**Version 2.1**

**1.2 Features**

- “ADSL-friendly” high voltage SLIC with integrated ringing
- Compatible with both 3.3 and 5 V systems
- Available in single and dual-channel versions
- High-voltage line feed (long loop driving capability)
- Sensing of transversal and longitudinal line currents
- Two Battery voltages (–15 V ... –85 V)
- Positive ring supply voltage up to +85 V
- Total supply voltage up to 150 V
- Integrated balanced ringing up to 85 V<sub>rms</sub>
- High longitudinal balance performance with SLIC-E2 (PEF 4265-2)
- Power-saving active mode (ACTL) with reduced battery voltage
- Power Down mode with negligible power consumption
- Package options:
  - PG-DSO-20-24
  - PG-VQFN-48-15
  - PG-DSO-36-15 (dual channel)
- Reliable Smart Power Technology (SPT170)



PG-DSO-20-24



PG-VQFN-48-15



PG-DSO-36-15

| Product Name    | Product Type             | Package       |
|-----------------|--------------------------|---------------|
| SLIC-E, SLIC-E2 | PEF 4265 T, PEF 4265-2 T | PG-DSO-20-24  |
| SLIC-E, SLIC-E2 | PEF 4265 V, PEF 4265-2 V | PG-VQFN-48-15 |
| TSLIC-E         | PEF 4365 T               | PG-DSO-36-15  |



### 1.3 Logic Symbol

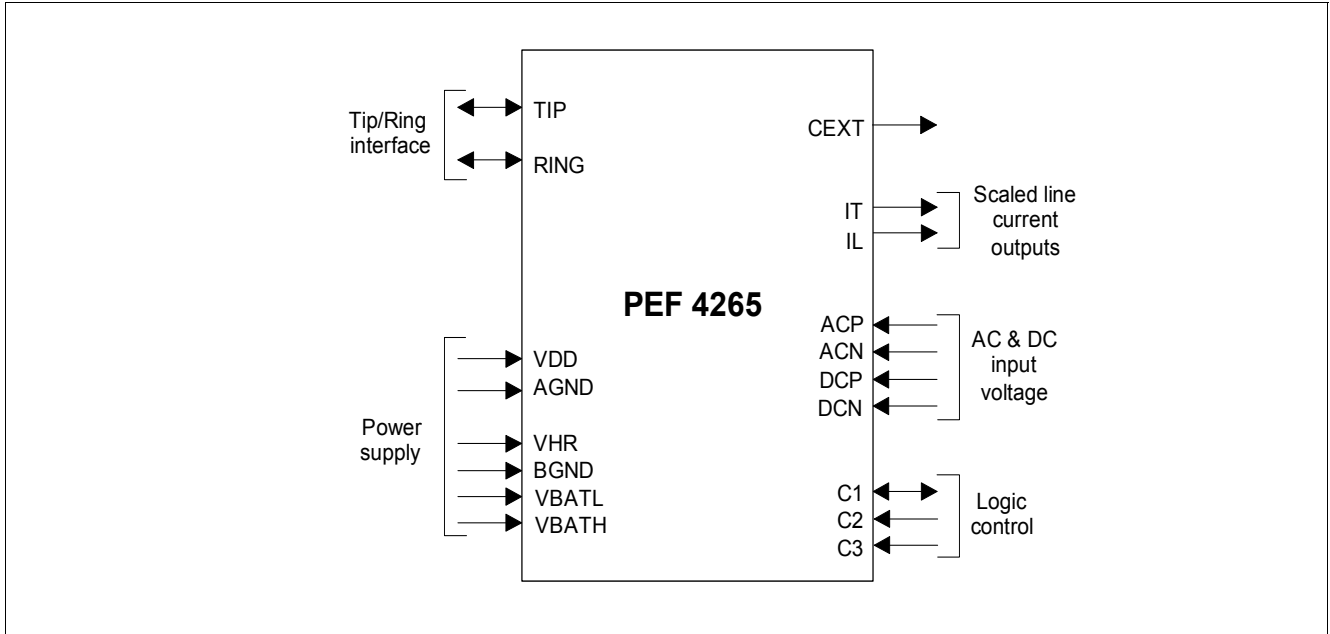


Figure 1 Logic Symbol PEF 4265

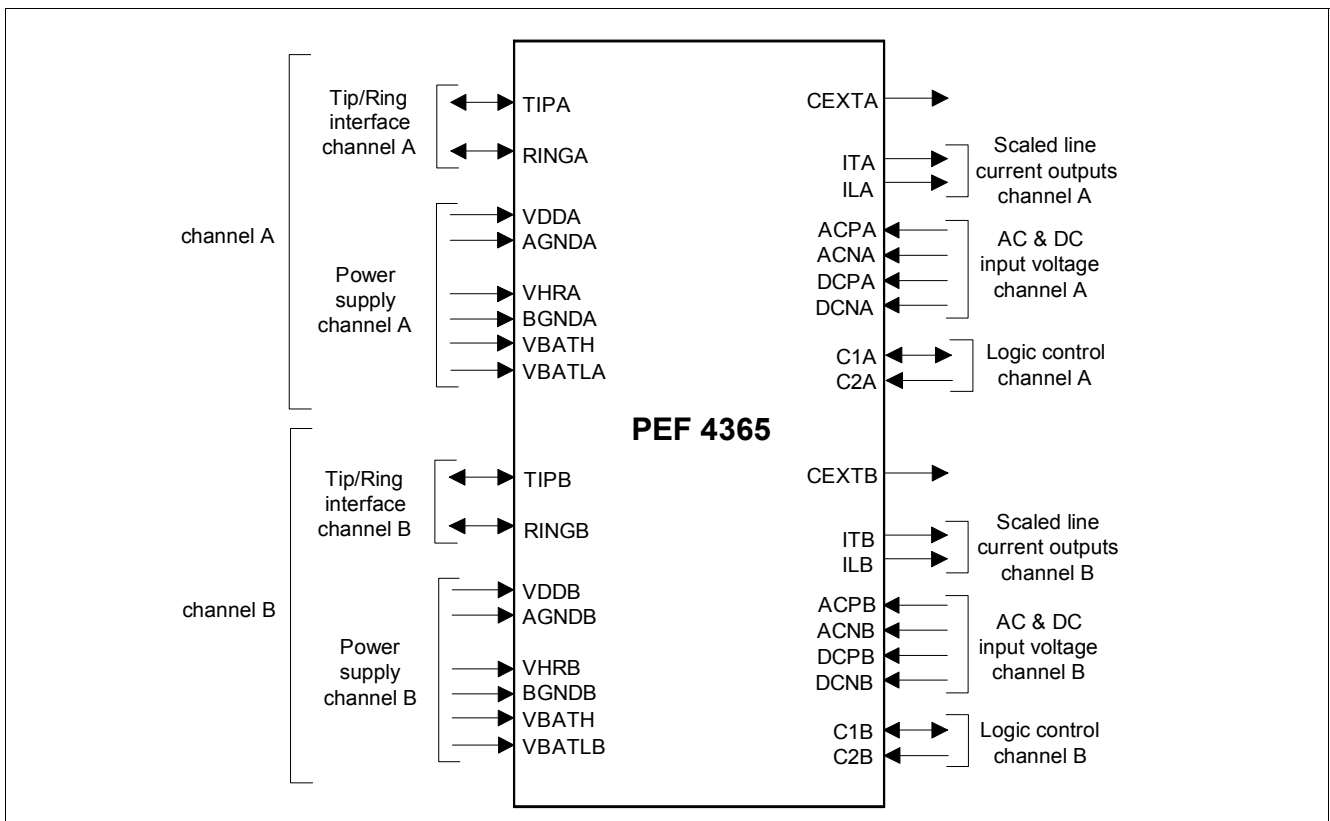


Figure 2 Logic Symbol PEF 4365

## 1.4 Pin Configuration

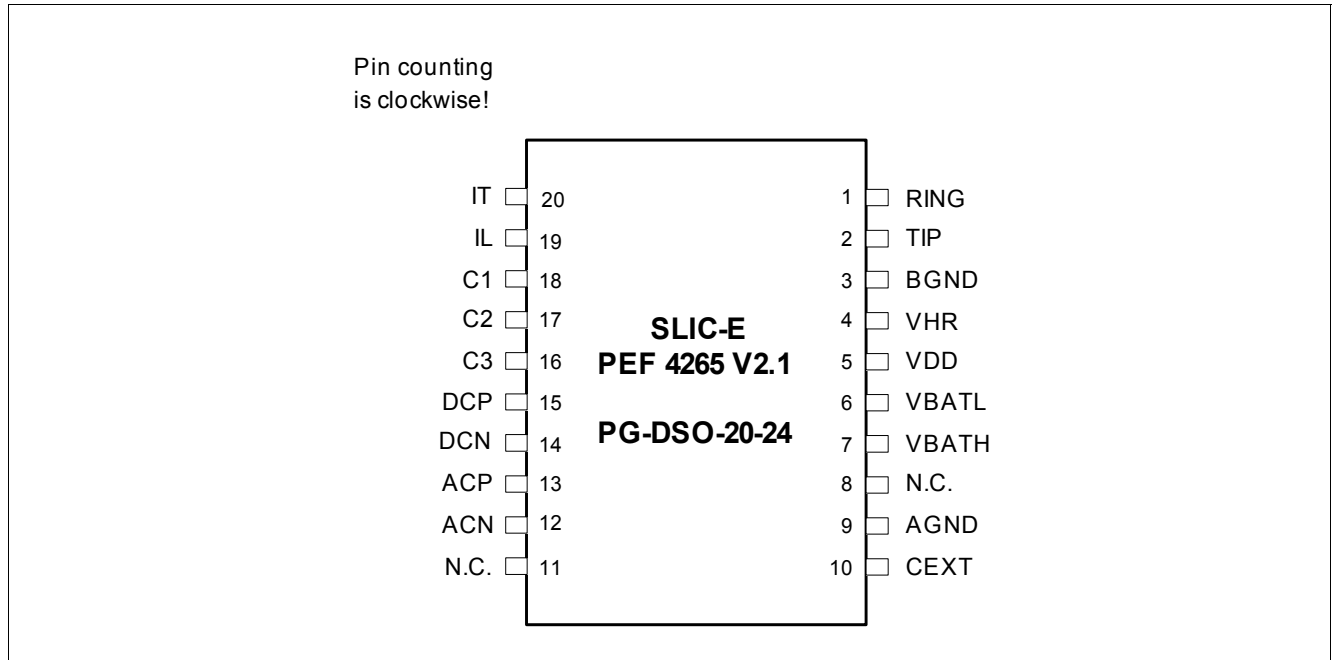


Figure 3 Pin Configuration PG-DSO-20-24 Package (top view)

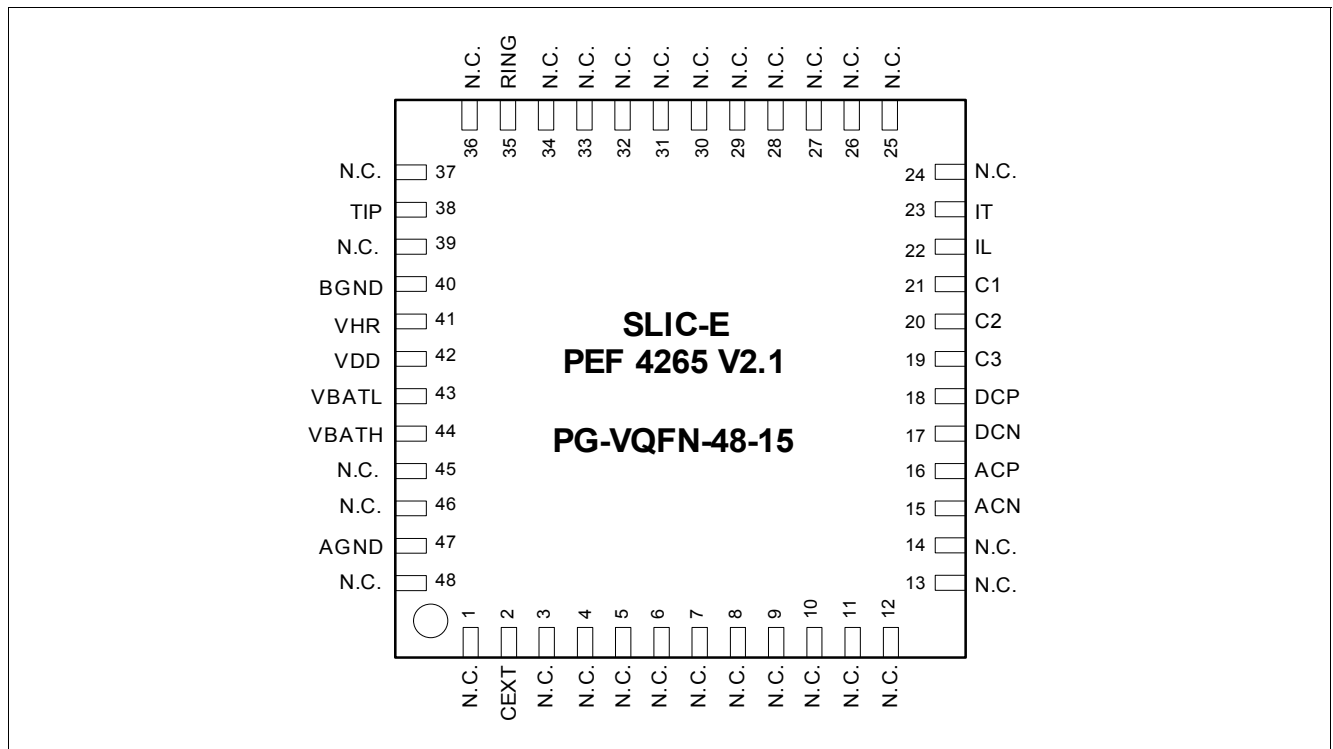


Figure 4 Pin Configuration PG-VQFN-48-15 Package (top view)

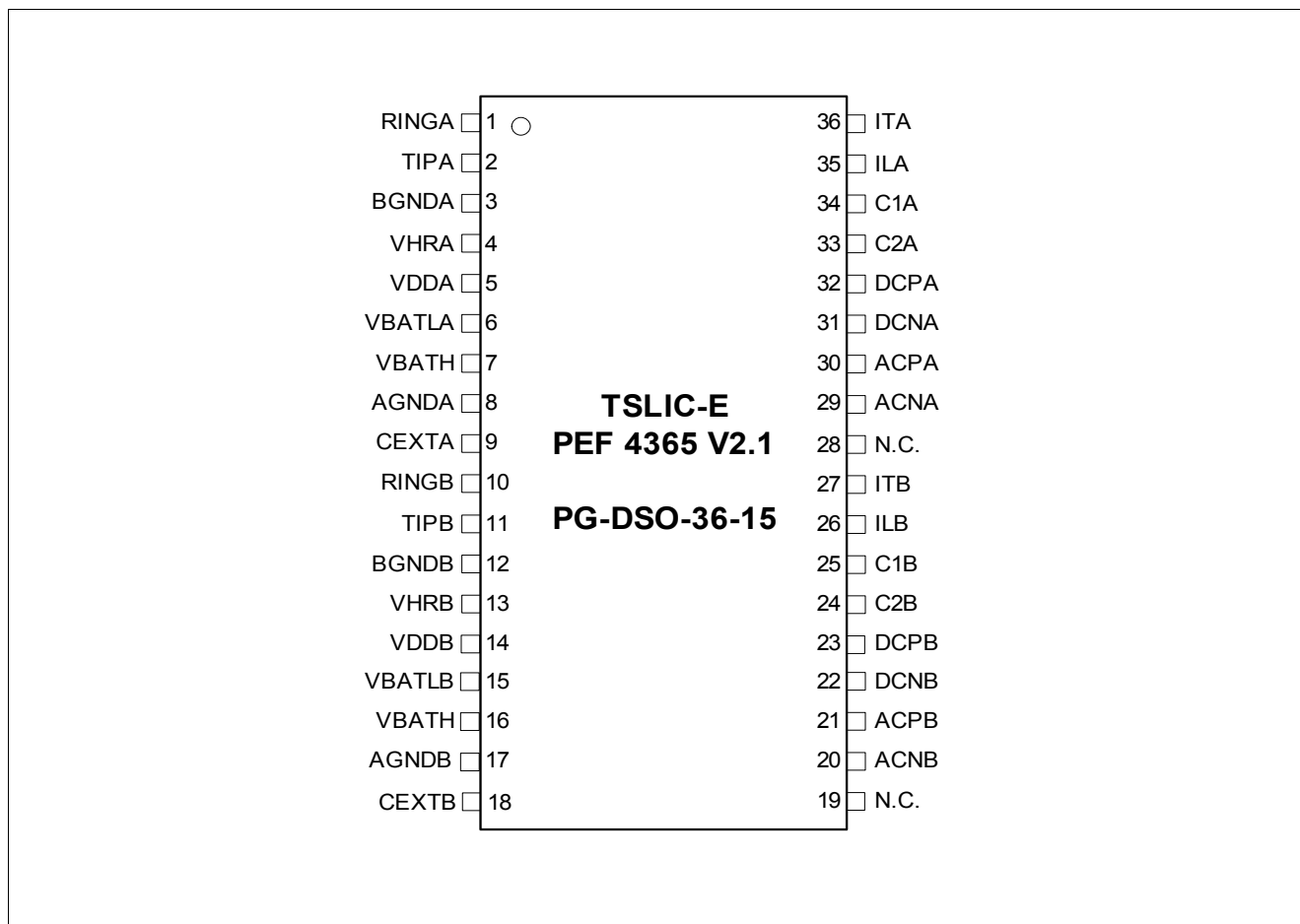


Figure 5 Pin Configuration PG-DSO-36-15 Package (dual channel)

## 1.5 Pin Definitions and Functions

**Table 1 Pin Definitions and Functions PG-DSO-20-24 and PG-VQFN-48-15**

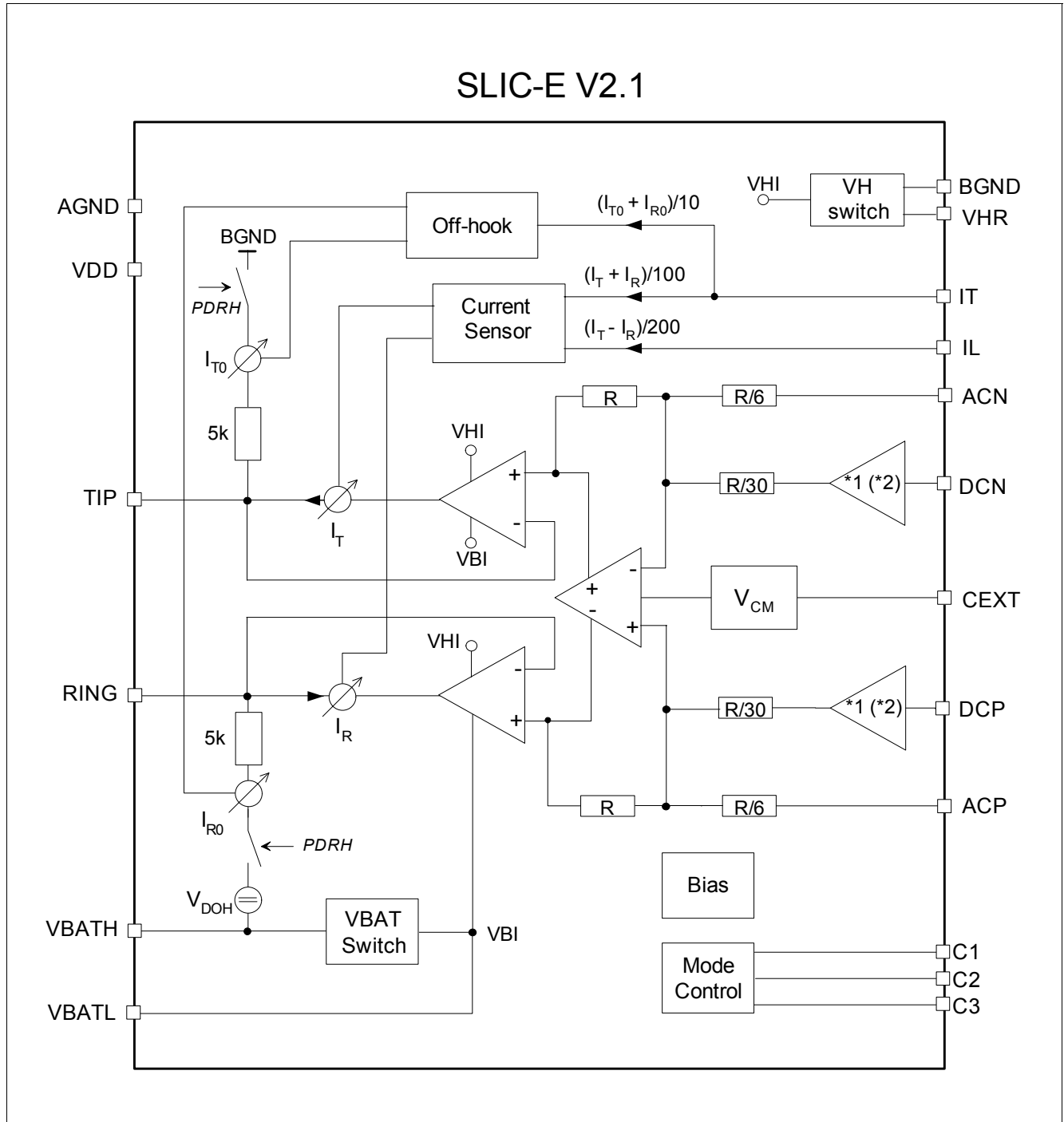
| Pin No.<br>DSO-20 | Pin No.<br>VQFN-48 | Name       | Pin<br>Type | Function                                                                                                                                                          |
|-------------------|--------------------|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                 | 35                 | RING       | I/O         | Subscriber loop connection RING                                                                                                                                   |
| 2                 | 38                 | TIP        | I/O         | Subscriber loop connection TIP                                                                                                                                    |
| 3                 | 40                 | BGND       | GND         | Battery ground: reference for TIP, RING, VBATH, VBATL and VHR                                                                                                     |
| 4                 | 41                 | VHR        | PWR         | Auxiliary positive battery supply voltage used in ringing mode<br>( $5\text{ V} \leq V_{\text{HR}} \leq 85\text{ V}$ )                                            |
| 5                 | 42                 | VDD        | PWR         | Positive supply voltage (+3.3 or +5 V), referred to AGND                                                                                                          |
| 6                 | 43                 | VBATL      | PWR         | Second negative battery supply voltage ( $-15\text{ V} \geq V_{\text{BATL}} \geq V_{\text{BATH}}$ )                                                               |
| 7                 | 44                 | VBATH      | PWR         | Most negative battery supply voltage; chip substrate potential<br>( $-20\text{ V} \geq V_{\text{BATH}} \geq -85\text{ V}$ )                                       |
| 9                 | 47                 | AGND       | GND         | Analog ground: reference for VDD and all signal and control pins except TIP and RING                                                                              |
| 10                | 2                  | CEXT       | O           | Common mode line potential with high output resistance (160 kΩ); an external capacitance allows supply voltage filtering                                          |
| 12<br>13          | 15<br>16           | ACN<br>ACP | I           | ACP - ACN: differential two-wire AC input voltage; at TIP/RING amplified by -6                                                                                    |
| 14<br>15          | 17<br>18           | DCN<br>DCP | I           | DCP - DCN: differential DC or ring input voltage; at TIP/RING amplified by -30 (ACTL, ACTH) and -60 (ACTR mode), respectively                                     |
| 16                | 19                 | C3         | I           | Ternary logic input, controlling the operation mode internal pull-down (C3 = L, if not connected)                                                                 |
| 17                | 20                 | C2         | I           | Ternary logic input, controlling the operation mode                                                                                                               |
| 18                | 21                 | C1         | I/O         | Ternary logic input, controlling the operation mode in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 μA. |
| 19                | 22                 | IL         | O           | Current output: longitudinal line current scaled down by a factor of 100                                                                                          |
| 20                | 23                 | IT         | O           | Current output: transversal line current scaled down by a factor of 50                                                                                            |
| 8, 11             | 1)                 | N.C.       |             | Not connected                                                                                                                                                     |

1) For the PG-VQFN-48-15 package the following pins are not connected:  
1,3,4,5,6,7,8,9,10,11,12,13,14,24,25,26,27,28,29,30,31,32,33,34,36,37,39,45,46,48

**Table 2 Pin Definitions and Functions PG-DSO-36-15**

| Pin No.          | Name                     | Pin Type | Function                                                                                                                                                                            |
|------------------|--------------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1<br>10          | RINGA<br>RINGB           | I/O      | Subscriber loop connection RING (Channel A)<br>Subscriber loop connection RING (Channel B)                                                                                          |
| 2<br>11          | TIPA<br>TIPB             | I/O      | Subscriber loop connection TIP                                                                                                                                                      |
| 3<br>12          | BGNDA<br>BGNDDB          | GND      | Battery ground: reference for TIP, RING, VBATH, VBATL and VHR                                                                                                                       |
| 4<br>13          | VHRA<br>VHRB             | PWR      | Auxiliary positive battery supply voltage used in ringing mode<br>( $5\text{ V} \leq V_{\text{HR}} \leq 85\text{ V}$ )                                                              |
| 5<br>14          | VDDA<br>VDDDB            | PWR      | Positive supply voltage (+3.3 or +5 V), referred to AGND                                                                                                                            |
| 6<br>15          | VBATLA<br>VBATLB         | PWR      | Second negative battery supply voltage ( $-15\text{ V} \geq V_{\text{BATL}} \geq V_{\text{BATH}}$ )                                                                                 |
| 7, 16            | VBATH                    | PWR      | Most negative battery supply voltage; chip substrate potential<br>( $-20\text{ V} \geq V_{\text{BATH}} \geq -85\text{ V}$ )                                                         |
| 8<br>17          | AGNDA<br>AGNDB           | GND      | Analog ground: reference for VDD and all signal and control pins except TIP and RING                                                                                                |
| 9<br>18          | CEXTA<br>CEXTB           | O        | Common mode line potential with high output resistance (160 k $\Omega$ );<br>an external capacitance allows supply voltage filtering                                                |
| 29, 30<br>20, 21 | ACNA, ACPA<br>ACNB, ACPB | I        | ACP - ACN: differential two-wire AC input voltage; at TIP/RING<br>amplified by -6                                                                                                   |
| 31, 32<br>22, 23 | DCNA, DCPA<br>DCNB, DCPB | I        | DCP - DCN: differential DC or ring input voltage; at TIP/RING amplified<br>by -30 (ACTL, ACTH) and -60 (ACTR mode), respectively                                                    |
| 33<br>24         | C2A<br>C2B               | I        | Ternary logic input, controlling the operation mode                                                                                                                                 |
| 34<br>25         | C1A<br>C1B               | I/O      | Ternary logic input, controlling the operation mode<br>in case of thermal overload (chip temperature exceeding 165 °C) this<br>pin sinks a current of typically 150 $\mu\text{A}$ . |
| 35<br>26         | ILA<br>ILB               | O        | Current output: longitudinal line current scaled down by a factor of 100                                                                                                            |
| 36<br>27         | ITA<br>ITB               | O        | Current output: transversal line current scaled down by a factor of 50                                                                                                              |
| 19, 28           | N.C.                     |          | Not connected                                                                                                                                                                       |

## 1.6 Functional Block Diagram



**Figure 6 Block Diagram**

Note: As in the dual channel version both channels "A" and "B" are identical, channel independent pin names (e.g. "TIP" instead of "TIPA / TIPB") are used throughout this document (with the exception of [Table 2](#))

## 2 Functional Description

A functional block diagram is shown in [Figure 6](#).

SLIC-E V2.1 supports AC and DC control loops based on feeding a voltage  $V_{TR}$  to the line and sensing the transversal line current  $I_{Trans}$  and the longitudinal current  $I_{Long}$ .

In receive direction, DC and AC voltages are handled separately with different gains. Both are applied differentially via the codec interface pins DCP / DCN and ACP / ACN, respectively, defining the transversal line voltage  $V_{TR}$  through

$$\begin{aligned} V_{TR} &= V_{TIP} - V_{RING} = V_{ab} = \\ &= 30 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN}) \text{ for modes ACTH, ACTL} \\ &= 60 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN}) \text{ for mode ACTR} \end{aligned}$$

As the ring signal is processed in the DC path, the DC gain is doubled in the ring mode ACTR to enable the full output voltage swing.

The common mode line voltage is always equal to the mean supply voltage,  $V_{CM} = (V_{HI} + V_{BI}) / 2$ , leading to symmetrical line potentials with respect to the supplies. Depending on the operation mode,  $V_{HI}$  is switched either to  $V_{HR}$  or to BGND via the VH switch, whereas  $V_{BI}$  is connected either to  $V_{BATH}$  via the VBAT switch or to  $V_{BATL}$  via an external diode.

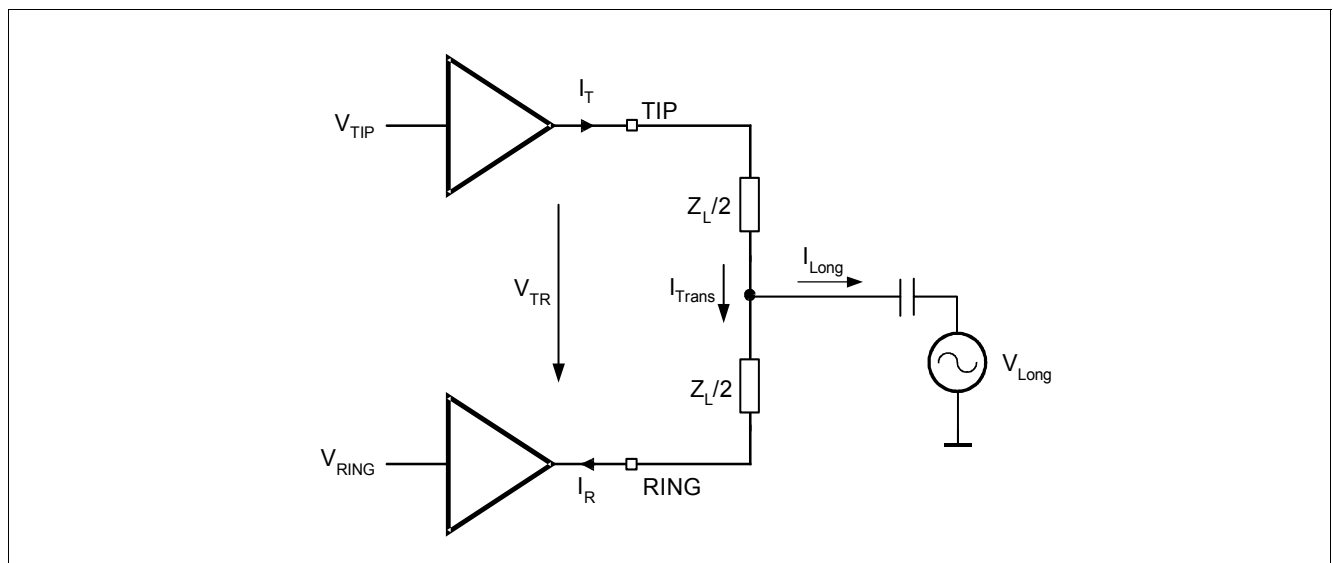
A reversed polarity of  $V_{TR}$  is easily obtained by changing the polarity of  $(V_{DCP} - V_{DCN})$ .

In transmit direction, the transversal and longitudinal line currents  $I_{Trans}$  and  $I_{Long}$  ([Figure 7](#)) are measured, and scaled images are provided at the IT and IL pins, respectively:

$$\begin{aligned} I_{IT} &= (I_T + I_R) / 100 = I_{Trans} / 50 & I_{IL} &= (I_T - I_R) / 200 = I_{Long} / 100 \\ I_{Trans} &= (I_T + I_R) / 2 & I_{Long} &= (I_T - I_R) / 2 \end{aligned}$$

For off-hook detection in PDRH mode, 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively. The currents through these resistors,  $I_{T0}$  and  $I_{R0}$ , are sensed, scaled and provided at IT:

$$I_{IT0} = (I_{T0} + I_{R0}) / 10 = I_{TRANS0} / 5$$



**Figure 7 Transversal and Longitudinal Line Currents**



## 2.1 Operating Modes

SLIC-E V2.1 operates in the following modes controlled by ternary logic signals at C1, C2 and a binary signal at C3 (PEF 4265 only)

**Table 3 SLIC-E Mode Table**

|    |                 | C2     |       |      |                         |                  |
|----|-----------------|--------|-------|------|-------------------------|------------------|
|    |                 | L      | M     | H    |                         |                  |
| C1 | L <sup>1)</sup> | PDH    | PDRHL | PDRH | L or N.C. <sup>2)</sup> | C3 <sup>3)</sup> |
|    |                 | HIRT   |       |      | H <sup>4)</sup>         |                  |
|    | M               | ACTL   | ACTH  | ACTR | L or N.C. <sup>2)</sup> |                  |
|    |                 |        |       |      | H <sup>4)</sup>         |                  |
|    | H               | HIRT   | HIT   | HIR  | L or N.C. <sup>2)</sup> |                  |
|    |                 | ACTH-R |       |      | H <sup>4)</sup>         |                  |

1) No 'Overtemp' signaling possible via pin C1 if C1 is low.

2) Register setting (VINETIC®): SEL-SLIC = (0001)hex

3) Not connected in dual-channel version PEF 4365

4) Register setting (VINETIC®): SEL-SLIC = (0100)hex

**Table 4 SLIC-E Modes and Supplies**

| Mode          | Mode Description               | Internal Supply Voltages $V_{BI}$ , $V_{HI}$ |
|---------------|--------------------------------|----------------------------------------------|
| <b>PDH</b>    | Power Down High Impedance      | VBATH, VH switch open                        |
| <b>PDRH</b>   | Power Down Resistive High      | VBATH, VH switch open                        |
| <b>PDRHL</b>  | Power Down Resistive High Load | VBATH, VH switch open                        |
| <b>ACTL</b>   | Active Low                     | VBATL, BGND                                  |
| <b>ACTH</b>   | Active High                    | VBATH, BGND                                  |
| <b>ACTH-R</b> | Active High Resistive          | VBATH, BGND                                  |
| <b>ACTR</b>   | Active Ring                    | VBATH, VHR                                   |
| <b>HIRT</b>   | High Impedance on RING and TIP | VBATH, VHR                                   |
| <b>HIT</b>    | High Impedance on TIP          | VBATH, VHR                                   |
| <b>HIR</b>    | High Impedance on RING         | VBATH, VHR                                   |

### Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

### Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 kΩ each from TIP to BGND and RING to VBATH, respectively, while the output buffers show high impedance (see [Figure 6](#)). The current through these resistors is sensed, scaled by 1/5 and transferred to the IT pin for off-hook supervision.

### Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state from Power Down to Active modes (automatically initiated during a mode change). It causes fast preloading of CEXT in order to suppress line voltage transients.

**Active Low (ACTL), Active High (ACTH)**

These are the regular transmission modes for voiceband. The line-driving section is operated between BGND and VBATL (ACTL) or VBATH (ACTH).

**Active High Resistive (ACTH-R)**

The SLIC is operated in Active High state together with the 5 k $\Omega$  resistors from TIP to BGND and from RING to VBATH. This mode is intended to be used for line testing.

**Active Ring (ACTR)**

Utilizing an additional positive battery voltage  $V_{HR}$ , this mode allows balanced ringing of up to 85 Vrms or feeding of very long telephone lines. In ACTR mode the DC voltage gain is doubled to 60.

**High Impedance (HIR, HIT, HIRT)**

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer is still sensed. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

## 2.2 Current Limitation / Overtemperature Protection

In any operating mode the total current delivered by the output drivers is limited to typically 85 mA.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current  $I_{therm}$ .

### 3 Typical Application Circuit for DuSLIC® and VINETIC®

**Figure 8** to **Figure 9** show one channel of application circuits including SLIC-E / TSLIC-E V2.1 and SLICOFI®-2/-2S or VINETIC® codec (please refer to the latest DuSLIC® or VINETIC® Data Sheet).

In **Table 5** the recommended external components for a dual channel DuSLIC® or VINETIC® system and their typical values are listed.

**Table 5 External Components DuSLIC® / VINETIC® for 2 Channels**

| No. | Symbol              | Value                                           | Unit       | Relat. Tol.       | Rating         | DuSLIC® Systems | VINETIC® Systems |
|-----|---------------------|-------------------------------------------------|------------|-------------------|----------------|-----------------|------------------|
| 2   | $R_{IT1}$           | 470                                             | $\Omega$   | 1 %               | —              | x               | —                |
| 2   | $R_{IT1}$           | 510                                             | $\Omega$   | 1 %               | —              | —               | x                |
| 2   | $R_{IT2}$           | 680                                             | $\Omega$   | 1 %               | —              | x               | x                |
| 2   | $R_{IL}$            | 1.6                                             | k $\Omega$ | 1 %               | —              | x               | x                |
| 4   | $R_{STAB}$          | 30                                              | $\Omega$   | 1 % <sup>1)</sup> | —              | x               | x                |
| 4   | $C_{STAB}$          | 15 (POTS)<br>22 (IVD)                           | nF<br>nF   | 10 %<br>10 %      | 100 V<br>100 V | x<br>x          | x<br>x           |
| 2   | $C_{DC}$            | 120                                             | nF         | 10 %              | 10 V           | x               | —                |
| 2   | $C_{DC}$            | 220                                             | nF         | 10 %              | 10 V           | —               | x <sup>2)</sup>  |
| 2   | $C_{ITAC}$          | 680                                             | nF         | 10 %              | 10 V           | x               | —                |
| 2   | $C_{ITAC}$          | 1                                               | $\mu$ F    | 10 %              | 10 V           | —               | x                |
| 1   | $C_{PRE}$           | 18                                              | nF         | 5 %               | 10 V           | —               | x                |
| 2   | $C_{VCMIT}$         | 680                                             | nF         | 10 %              | 10 V           | x               | —                |
| 1   | $C_{REF}$           | 68                                              | nF         | 20 %              | 10 V           | x               | x                |
| 2   | $C_{EXT}$           | 100                                             | nF         | 20 %              | 50 V           | x               | x                |
| 6   | $C_1$               | 100                                             | nF         | 10 %              | 10 V           | x               | —                |
| 13  | $C_1$               | 100                                             | nF         | 10 %              | 10 V           | —               | x                |
| 6   | $C_2$               | 100                                             | nF         | 10 %              | 100 V          | x               | x                |
| 1   | $C_3$               | 4.7                                             | $\mu$ F    | 20 %              | 10 V, Tantal   | x               | —                |
| 4   | $D_1, D_2$          | BAS 21                                          | —          | —                 | —              | x               | x                |
| 2   | $D_3$ <sup>3)</sup> | BAS 21                                          | —          | —                 | —              | x               | x                |
| 2   | OVP <sup>4)</sup>   | Overvoltage Protection<br>(e.g. thyristor)      | —          | —                 | —              | x               | x                |
| 4   | OCP <sup>4)</sup>   | Overcurrent Protection<br>(e.g. LFR, fuse, PTC) | —          | —                 | —              | x               | x                |

1) Matching tolerance depends on longitudinal balance requirements (for details see [2]).

2) With VINETIC®-2CPE this capacitance is substituted by 100 nF between DCN and DCP.

3) Due to the changed battery switch concept (see **Figure 6**), the VBATL series diode must not be shared between different channels; one diode per channel is mandatory (also for applications with TSLIC).

4) See [1]

The C3 pin of SLIC-E V2.1 can be either

- Not connected (or connected to AGND) to be compatible with previous SLIC-E/-E2 versions or
- Connected to IO0x (IO2x) of VINETIC® (SLICOFI®-2/-2S) to offer an additional test mode ACTH-R.

Typical Application Circuit for DuSLIC® and VINETIC®

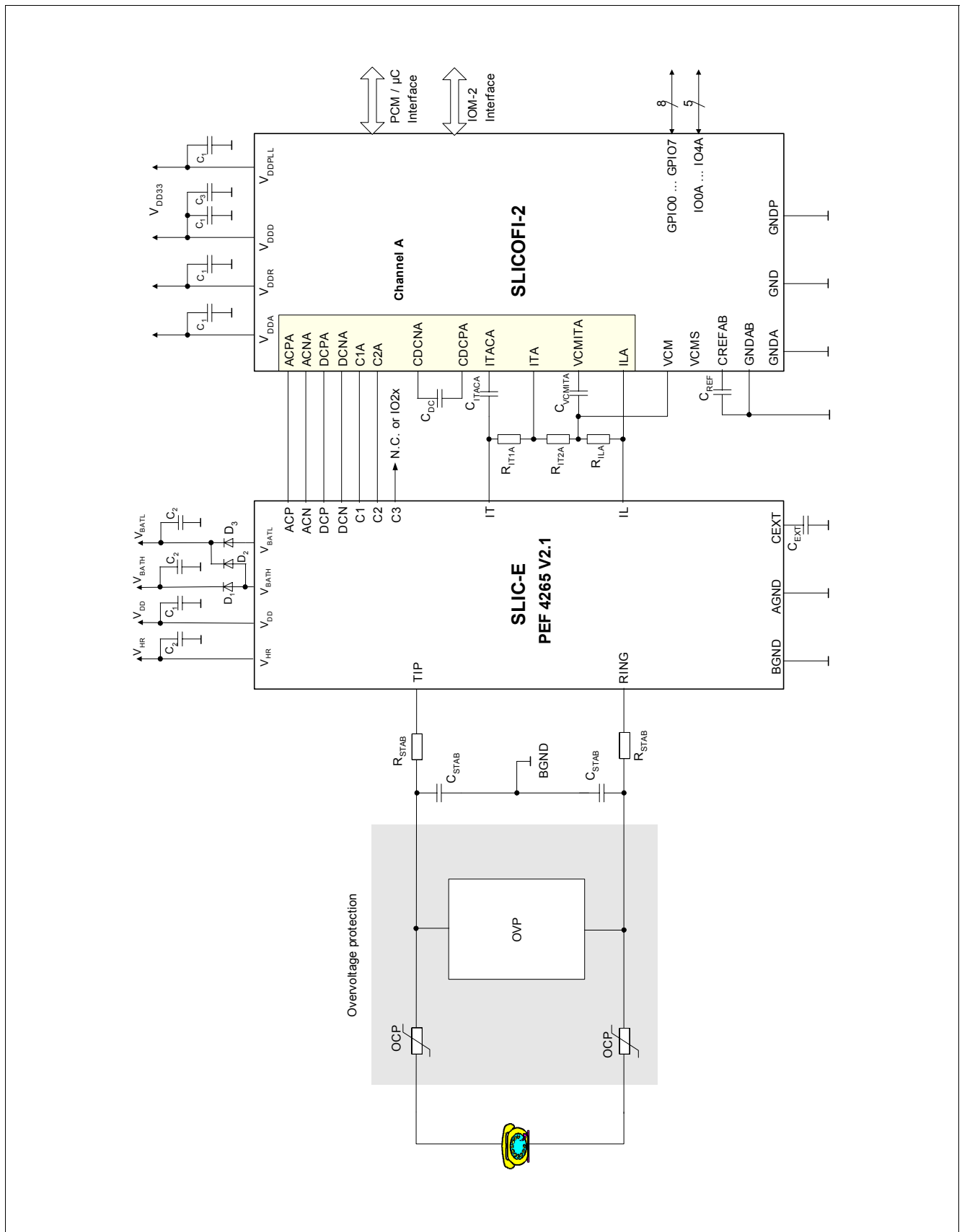


Figure 8 Application Circuit DuSLIC®

Typical Application Circuit for DuSLIC® and VINETIC®

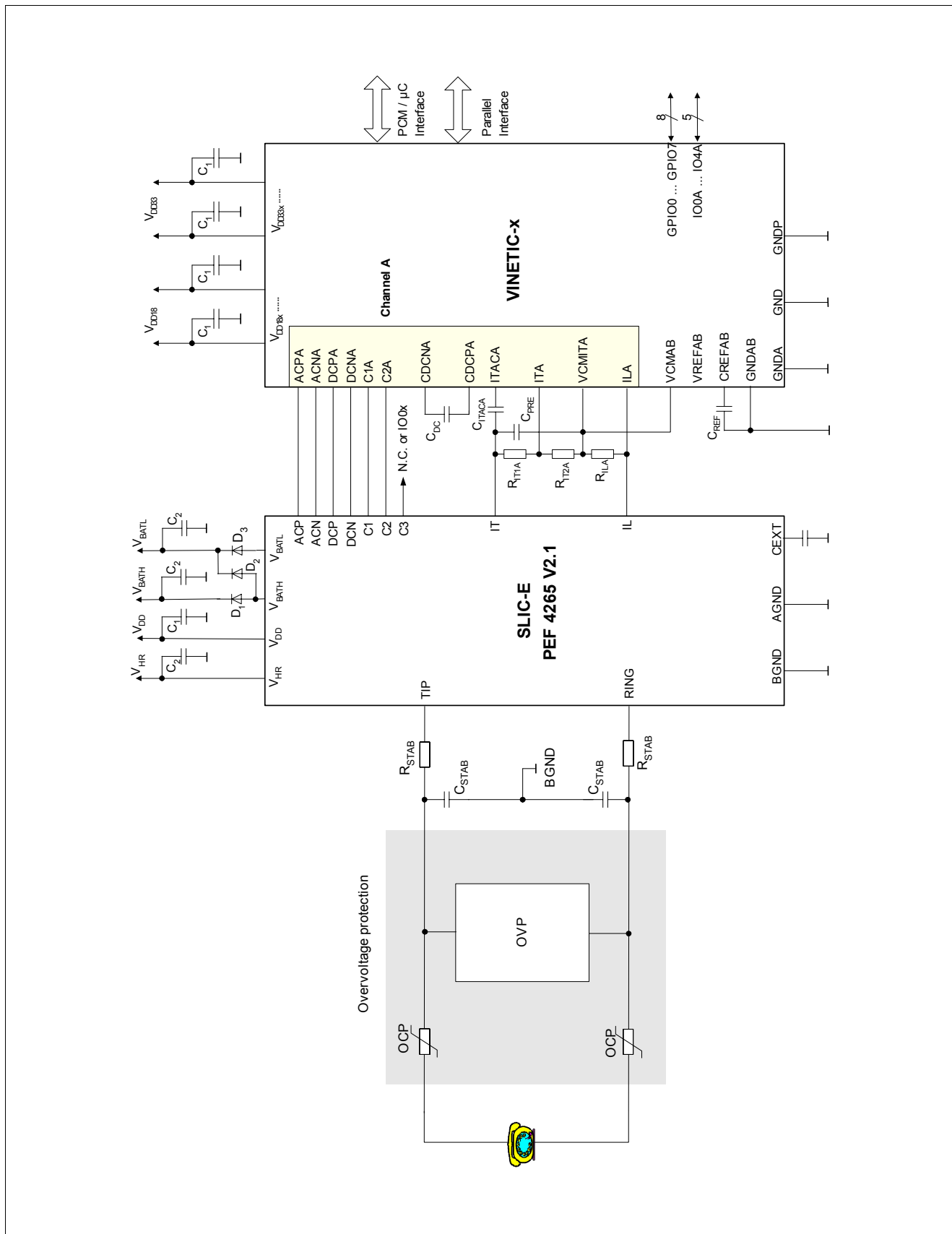


Figure 9 Application Circuit VINETIC®

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

**Table 6 Absolute Maximum Ratings**

| Parameter                                | Symbol                                                       | Values |      |                | Unit | Note / Test Condition                     |
|------------------------------------------|--------------------------------------------------------------|--------|------|----------------|------|-------------------------------------------|
|                                          |                                                              | Min.   | Typ. | Max.           |      |                                           |
| Battery voltage low                      | $V_{BATL}$                                                   | -85    | –    | 0.4            | V    | Referred to BGND                          |
| Battery voltage high                     | $V_{BATH}$                                                   | -90    | –    | 0.4            | V    | Referred to BGND                          |
| Battery voltage difference               | $V_{BATL} - V_{BATH}$                                        | -0.4   | –    | –              | V    | –                                         |
| Auxiliary supply voltage                 | $V_{HR}$                                                     | -0.4   | –    | 90             | V    | Referred to BGND                          |
| Total battery supply voltage, continuous | $V_{HR} - V_{BATH}$                                          | -0.4   | –    | 160            | V    | –                                         |
| $V_{DD}$ supply voltage                  | $V_{DD}$                                                     | -0.4   | –    | 7              | V    | Referred to AGND                          |
| Ground voltage difference                | $V_{BGND} - V_{AGND}$                                        | -0.4   | –    | 0.4            | V    | –                                         |
| Input voltages                           | $V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}, V_{C3}$ | -0.4   | –    | $V_{DD} + 0.4$ | V    | Referred to AGND                          |
| Junction temperature                     | $T_j$                                                        | –      | –    | 150            | °C   | –                                         |
| ESD voltage, all pins                    | –                                                            | –      | –    | 1              | kV   | SDM (Socketed Device Model) <sup>1)</sup> |
|                                          | –                                                            | –      | –    | 1              | kV   | HBM (Human Body Model) <sup>1)</sup>      |

1) EOS/ESD Assn. Standard DS5.3-1993.

**Attention: Stresses exceeding the max. values listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

### 4.2 Foreign Line Voltages

External voltages applied at the line outputs may cause large currents in the SLIC. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, if the overtemperature protection cannot react sufficiently fast due to high local power density. The safe power dissipation values are strongly dependent on duration. They can be expressed in terms of voltage and current limits directly at the TIP and RING pins (see [Table 7](#) and [Table 8](#)).

**Table 7 Voltage Limits on Output Pins**

| Voltage Duration | Pins      | Min. Voltage [V] | Max. Voltage [V] |
|------------------|-----------|------------------|------------------|
| Continuous       | TIP, RING | $V_{BATH} - 0.4$ | $V_{HR} + 5$     |
| < 10 ms          | TIP, RING | $V_{BATH} - 5$   | $V_{HR} + 10$    |
| < 100 $\mu$ s    | TIP, RING | $V_{BATH} - 10$  | $V_{HR} + 20$    |
| < 1 $\mu$ s      | TIP, RING | $V_{BATH} - 15$  | $V_{HR} + 40$    |

**Table 8 Current Limits on Output Pins**

| Current Duration | Pins      | Min. current [A] | Max. current [A] |
|------------------|-----------|------------------|------------------|
| Continuous       | TIP, RING | – 0.1            | 0.1              |
| < 10 ms          | TIP, RING | – 0.5            | 0.5              |
| < 100 µs         | TIP, RING | – 1.0            | 1.0              |
| < 1 µs           | TIP, RING | – 1.5            | 1.5              |

The above limitations have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see [1]).

### 4.3 Operating Range

**Table 9 Operating Range**

| Parameter                                        | Symbol                | Values   |      |                   | Unit | Note / Test Condition |
|--------------------------------------------------|-----------------------|----------|------|-------------------|------|-----------------------|
|                                                  |                       | Min.     | Typ. | Max.              |      |                       |
| Battery voltage L <sup>1)</sup>                  | $V_{BATL}$            | –80      | –    | –15               | V    | Referred to BGND      |
| Battery voltage H <sup>1)</sup>                  | $V_{BATH}$            | –85      | –    | –20               | V    | Referred to BGND      |
| Auxiliary supply voltage                         | $V_{HR}$              | $V_{DD}$ | –    | 85                | V    | Referred to BGND      |
| Total battery supply voltage                     | $V_{HR} - V_{BATH}$   | –        | –    | 150               | V    | –                     |
| $V_{DD}$ supply voltage                          | $V_{DD}$              | 3.15     | –    | 5.5               | V    | Referred to AGND      |
| Ground voltage difference                        | $V_{BGND} - V_{AGND}$ | –0.4     | –    | 0.4               | V    | –                     |
| Voltage at pins IT, IL                           | $V_{IT}, V_{IL}$      | –0.4     | –    | $V_{DD} - 0.6$    | V    | Referred to AGND      |
| Input range $V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}$ |                       | 0        | –    | 3.3               | V    | Referred to AGND      |
| Ambient temperature                              | $T_{amb}$             | –40      | –    | 85                | °C   | –                     |
| Junction temperature                             | $T_J$                 | –        | –    | 125 <sup>2)</sup> | °C   | –                     |

1) If the battery switch is not used, VBATL has to be connected with VBATH

2) Operation up to  $T_J = 150$  °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

### 4.4 Thermal Resistances

**Table 10 Thermal Resistances**

| Parameter           | Symbol       | Values |      |      | Unit | Note / Test Condition                                                                                                                           |
|---------------------|--------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
|                     |              | Min.   | Typ. | Max. |      |                                                                                                                                                 |
| Junction to case    | $R_{th, jC}$ | –      | 2    | –    | K/W  | All packages                                                                                                                                    |
| Junction to ambient | $R_{th, jA}$ | –      | 50   | –    | K/W  | PG-DSO-20-24 without heatsink                                                                                                                   |
|                     |              | –      | 20   | –    | K/W  | PG-DSO-20-24 with heatsink<br>PG-DSO-36-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see <a href="#">Chapter 6.3.1</a> ) |
| Junction to ambient | $R_{th, jA}$ | –      | 25   | –    | K/W  | PG-VQFN-48-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see <a href="#">Chapter 6.2.1</a> )                              |

## 4.5 Electrical Parameters

Unless otherwise stated, minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at  $V_{BATH} = -48\text{ V}$ ,  $V_{BATL} = -24\text{ V}$ ,  $V_{HR} = +32\text{ V}$  and  $V_{DD} = +3.3\text{ V}$ .

Functionality and performance is guaranteed for  $T_A = 0$  to  $70\text{ °C}$  by production testing. Extended temperature range operation at  $-40\text{ °C} < T_A < 85\text{ °C}$  is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

### 4.5.1 Supply Currents and Power Dissipation

**Table 11** Supply Currents, Power Dissipation ( $I_R = I_T = 0$ ;  $V_{TR} = 0$ ; one channel)

| Parameter                                            | Symbol            | Values |      |      | Unit | Note /<br>Test Condition | No. |
|------------------------------------------------------|-------------------|--------|------|------|------|--------------------------|-----|
|                                                      |                   | Min.   | Typ. | Max. |      |                          |     |
| Power Down High Impedance, Power Down Resistive High |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 250  | 350  | μA   | –                        | 1   |
| $V_{\text{BATH}}$ current                            | $I_{\text{BATH}}$ | –      | 40   | 80   | μA   | –                        | 2   |
| $V_{\text{BATL}}$ current                            | $I_{\text{BATL}}$ | –      | 0    | 10   | μA   | –                        | 3   |
| $V_{\text{HR}}$ current                              | $I_{\text{HR}}$   | –      | 0    | 10   | μA   | –                        | 4   |
| Active Low                                           |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 2.2  | 2.8  | mA   | –                        | 5   |
| $V_{\text{BATH}}$ current                            | $I_{\text{BATH}}$ | –      | 40   | 80   | μA   | –                        | 6   |
| $V_{\text{BATL}}$ current <sup>1)</sup>              | $I_{\text{BATL}}$ | –      | 3.3  | 4    | mA   | –                        | 7   |
| $V_{\text{HR}}$ current                              | $I_{\text{HR}}$   | –      | 0    | 10   | μA   | –                        | 8   |
| Active High                                          |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 2.6  | 3.2  | mA   | –                        | 9   |
| $V_{\text{BATH}}$ current <sup>2)</sup>              | $I_{\text{BATH}}$ | –      | 3.8  | 4.5  | mA   | –                        | 10  |
| $V_{\text{BATL}}$ current                            | $I_{\text{BATL}}$ | –      | 0    | 10   | μA   | –                        | 11  |
| $V_{\text{HR}}$ current                              | $I_{\text{HR}}$   | –      | 0    | 10   | μA   | –                        | 12  |
| Active Ring                                          |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 1.5  | 2    | mA   | –                        | 13  |
| $V_{\text{BATH}}$ current <sup>3)</sup>              | $I_{\text{BATH}}$ | –      | 3.5  | 4.3  | mA   | –                        | 14  |
| $V_{\text{BATL}}$ current                            | $I_{\text{BATL}}$ | –      | 0    | 10   | μA   | –                        | 15  |
| $V_{\text{HR}}$ current <sup>4)</sup>                | $I_{\text{HR}}$   | –      | 1.8  | 2.3  | mA   | –                        | 16  |
| High Impedance on TIP or RING (HIR, HIT)             |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 1.5  | 2    | mA   | –                        | 17  |
| $V_{\text{BATH}}$ current                            | $I_{\text{BATH}}$ | –      | 2.9  | 3.6  | mA   | –                        | 18  |
| $V_{\text{BATL}}$ current                            | $I_{\text{BATL}}$ | –      | 0    | 10   | μA   | –                        | 19  |
| $V_{\text{HR}}$ current                              | $I_{\text{HR}}$   | –      | 1.3  | 1.7  | mA   | –                        | 20  |
| High Impedance on TIP and RING (HIRT)                |                   |        |      |      |      |                          |     |
| $V_{\text{DD}}$ current                              | $I_{\text{DD}}$   | –      | 1.4  | 1.8  | mA   | –                        | 21  |
| $V_{\text{BATH}}$ current                            | $I_{\text{BATH}}$ | –      | 2.2  | 2.8  | mA   | –                        | 22  |



## Electrical Characteristics

**Table 11 Supply Currents, Power Dissipation** ( $I_R = I_T = 0$ ;  $V_{TR} = 0$ ; one channel) (cont'd)

| Parameter          | Symbol     | Values |      |      | Unit    | Note / Test Condition | No. |
|--------------------|------------|--------|------|------|---------|-----------------------|-----|
|                    |            | Min.   | Typ. | Max. |         |                       |     |
| $V_{BATL}$ current | $I_{BATL}$ | –      | 0    | 10   | $\mu A$ | –                     | 23  |
| $V_{HR}$ current   | $I_{HR}$   | –      | 0.8  | 1.1  | mA      | –                     | 24  |

1) Current depending on supply voltage:  $I_{BATL}(V_{BATL}) = I_{BATL}(-24V) + (-V_{BATL} - 24) / 40k\Omega$ 

2) Current depending on supply voltage:  $I_{BATH}(V_{BATH}) = I_{BATH}(-48V) + (-V_{BATH} - 48) / 40k\Omega$ 

3) Current depending on line voltage:  $I_{BATH}(V_{TR}) = I_{BATH}(0) + |V_{TR}| / 40k\Omega$ 

4) Current depending on line voltage:  $I_{HR}(V_{TR}) = I_{HR}(0) + |V_{TR}| / 60k\Omega$ 

The total power dissipated in the SLIC consists of the quiescent power  $P_Q$  due to the supply currents and the output stage power  $P_O$  caused by any line current  $I_{Trans}$  (see [Table 12](#)).

$$P_{tot} = P_Q + P_O$$

$$\text{with } P_Q = V_{DD} * I_{DD} + |V_{BATH}| * I_{BATH} + |V_{BATL}| * I_{BATL} + V_{HR} * I_{HR}$$

**Table 12 Output Stage Power Dissipation**

| Operating Mode | Equation for $P_O$ Calculation                                                                                                                       | Comment                                                                         |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| ACTL           | $P_O = (1.05 *  V_{BATL}  - V_{TR}) * I_{Trans}$                                                                                                     | –                                                                               |
| ACTH           | $P_O = (1.05 *  V_{BATH}  - V_{TR}) * I_{Trans}$                                                                                                     | –                                                                               |
| ACTR           | $P_O = (1.02 * V_{HR} + 1.05 *  V_{BATH}  - V_{TR}) * I_{Trans}$<br>$P_O = [4 * (V_H +  V_{BATH} ) - \pi * V_P * \cos \phi] * V_P / (2 * \pi * Z_L)$ | Ohmic load<br>complex load $Z = Z_L e^{i\phi}$ ,<br>$V_P$ ... peak ring voltage |

For the dual channel version, the power values of each channel have to be added to yield the total power dissipation.

## 4.5.2 DC Characteristics

**Table 13 DC Characteristics** ( $V_{ACP} = V_{ACN} = 1.5 \text{ V}$ )

| Parameter                                               | Symbol                             | Values |      |       | Unit | Note / Test Condition                                                                                           | No. |
|---------------------------------------------------------|------------------------------------|--------|------|-------|------|-----------------------------------------------------------------------------------------------------------------|-----|
|                                                         |                                    | Min.   | Typ. | Max.  |      |                                                                                                                 |     |
| Line Termination TIP, RING                              |                                    |        |      |       |      |                                                                                                                 |     |
| Differential DC line voltage                            | $V_{TR, DC}$                       | -0.4   | 0    | 0.4   | V    | $V_{DCP} = V_{DCN} = 1.5\text{ V}$<br>Modes: ACTx                                                               | 25  |
|                                                         |                                    | 23.5   | 24   | 24.5  | V    | $V_{DCP} - V_{DCN} = 0.8\text{ V}$<br>Mode: ACTH                                                                | 26  |
|                                                         |                                    | -24.5  | -24  | -23.5 | V    | $V_{DCP} - V_{DCN} = -0.8\text{ V}$<br>Mode: ACTH                                                               | 27  |
| Common mode DC line voltage                             | $V_{TIP, DC} = V_{RING, DC}$       | -13    | -12  | -11   | V    | Mode: ACTL                                                                                                      | 28  |
|                                                         |                                    | -25    | -24  | -23   | V    | Mode: ACTH                                                                                                      | 29  |
|                                                         |                                    | -10    | -9   | -8    | V    | Mode: ACTR                                                                                                      | 30  |
| DC line voltage drop (see Figure 10)                    | $-V_{BATH} - V_{TR, max}$          | -      | 2.5  | 3     | V    | $I_{Trans, DC} = 20\text{ mA}$<br>$V_{DCP} - V_{DCN} = 2.5\text{ V}$<br>Temp = 25°C <sup>1)</sup><br>Mode: ACTH | 31  |
| Output current limit (see Figure 15)                    | $ I_{R, max} ,  I_{T, max} $       | 70     | 85   | 100   | mA   | $V_T, V_R = 0$ (sinking)                                                                                        | 32  |
|                                                         |                                    | 80     | 100  | 120   | mA   | $V_T, V_R = V_{BATx}$ (sourcing)<br>Temp = 25°C <sup>2)</sup>                                                   | 33  |
| Open loop resistance TIP to $V_{BGND}$ (see Figure 16)  | $R_{TG}$                           | 4.2    | 5    | 5.8   | kΩ   | Temp = 25°C <sup>3)</sup><br>Mode: PDRH                                                                         | 34  |
| Open loop resistance RING to $V_{BATH}$ (see Figure 16) | $R_{RB}$                           | 4.2    | 5    | 5.8   | kΩ   | Temp = 25°C <sup>3)</sup><br>Mode: PDRH                                                                         | 35  |
| Power down open loop line voltage                       | $V_{TR, PD} = -V_{BATH} - V_{DOH}$ | 42     | 44   | 47    | V    | Mode: PDRH                                                                                                      | 36  |
| Power down output leakage current                       | $I_{Leak, R}$                      | -10    | -    | 10    | μA   | $V_{BATH} < V_{T/R} < 0$                                                                                        | 37  |
|                                                         | $I_{Leak, T}$                      | -10    | -    | 10    | μA   | Mode: PDH                                                                                                       | 38  |
| High impedance output leakage current                   | $I_{Leak, R}$                      | -10    | -    | 10    | μA   | $V_{BATH} < V_R < V_{HR}$<br>Mode: HIR, HIRT                                                                    | 39  |
|                                                         | $I_{Leak, T}$                      | -10    | -    | 10    | μA   | $V_{BATH} < V_T < V_{HR}$<br>Mode: HIT, HIRT                                                                    | 40  |
| Inputs DCP, DCN, ACP, ACN, Output C <sub>EXT</sub>      |                                    |        |      |       |      |                                                                                                                 |     |
| Input current DCP, DCN                                  | $I_{DC}$                           | -      | 0.1  | -     | μA   | -                                                                                                               | 41  |
| Differential AC input resistance ACP, ACN               | $R_{AC}$                           | -      | 20   | -     | kΩ   | -                                                                                                               | 42  |
| Output resistance on C <sub>EXT</sub>                   | -                                  | -      | 100  | -     | kΩ   | -                                                                                                               | 43  |
| Current Outputs IT, IL                                  |                                    |        |      |       |      |                                                                                                                 |     |
| IT output current                                       | $I_{IT}$                           | -15    | 0    | 15    | μA   | $I_R = I_T = 0\text{ mA}$                                                                                       | 44  |
| IT output current normal polarity                       | $I_{IT}$                           | 380    | 400  | 420   | μA   | $I_R = I_T = 20\text{ mA}$                                                                                      | 45  |

## Electrical Characteristics

**Table 13 DC Characteristics** ( $V_{ACP} = V_{ACN} = 1.5 \text{ V}$ ) (cont'd)

| Parameter                                               | Symbol        | Values |      |      | Unit          | Note / Test Condition                                         | No. |
|---------------------------------------------------------|---------------|--------|------|------|---------------|---------------------------------------------------------------|-----|
|                                                         |               | Min.   | Typ. | Max. |               |                                                               |     |
| IT output current reverse polarity <sup>4)</sup>        | $I_{IT}$      | -420   | -400 | -380 | $\mu\text{A}$ | $I_R = I_T = -20 \text{ mA}$                                  | 46  |
| Transversal current ratio (see Figure 18) <sup>5)</sup> | $I/G_{IT,DC}$ | 49.5   | 50   | 50.5 | —             | $I_R = I_T = 20 \text{ mA}$ ,<br>$I_R = I_T = -20 \text{ mA}$ | 47  |
| Off-hook output current on IT                           | —             | 800    | 950  | 1100 | $\mu\text{A}$ | TIP/RING shorted,<br>Temp = 25 °C <sup>6)</sup><br>Mode: PDRH | 48  |
| IL output current (see Figure 18)                       | $I_{IL}$      | -20    | 0    | 20   | $\mu\text{A}$ | $I_R = I_T = 20 \text{ mA}$                                   | 49  |
|                                                         |               | 30     | 50   | 70   | $\mu\text{A}$ | $I_R = 15 \text{ mA}$ , $I_T = 25 \text{ mA}$                 | 50  |
|                                                         |               | -160   | -125 | -90  | $\mu\text{A}$ | $I_R = 50 \text{ mA}$ , $I_T = 25 \text{ mA}$                 | 51  |

**Control Inputs C1, C2, C3**

|                                        |             |      |     |                |               |                           |    |
|----------------------------------------|-------------|------|-----|----------------|---------------|---------------------------|----|
| H-input voltage                        | $V_{IH}$    | 2.7  | —   | $V_{DD} + 0.3$ | V             | —                         | 52 |
| M-input voltage                        | $V_{IM}$    | 1.2  | —   | 2.1            | V             | C1, C2 only               | 53 |
| L-input voltage                        | $V_{IL}$    | -0.3 | —   | 0.6            | V             | —                         | 54 |
| Input pull down current                | $I_{in}$    | 0    | 2   | 10             | $\mu\text{A}$ | C1, C2, C3                | 55 |
| Thermal overload current C1            | $I_{therm}$ | 120  | 150 | 250            | $\mu\text{A}$ | $V_{C1} = 1.20 \text{ V}$ | 56 |
| Thermal overload threshold temperature | $T_{jLIM}$  | —    | 165 | —              | °C            | Mode: ACTx, Hlx           | 57 |

- 1) The systematic temperature dependence is appr. + 7 mV / °C
- 2) The systematic temperature dependence is appr. -0.3 % / °C
- 3) The systematic temperature dependence is appr. +0.1 % / °C
- 4) With **VDD = 3.3 V**, the IT output current **in reverse polarity** is limited to typically 700  $\mu\text{A}$ ; thus, the DC current regulation loop operates correctly only up to the corresponding line current value of 35 mA. In all other cases, IT is linear within the full line current range
- 5) The offset ( $I_R = I_T = 0 \text{ mA}$ ) has to be taken into account.
- 6) The systematic temperature dependence is appr. -0.1 % / °C

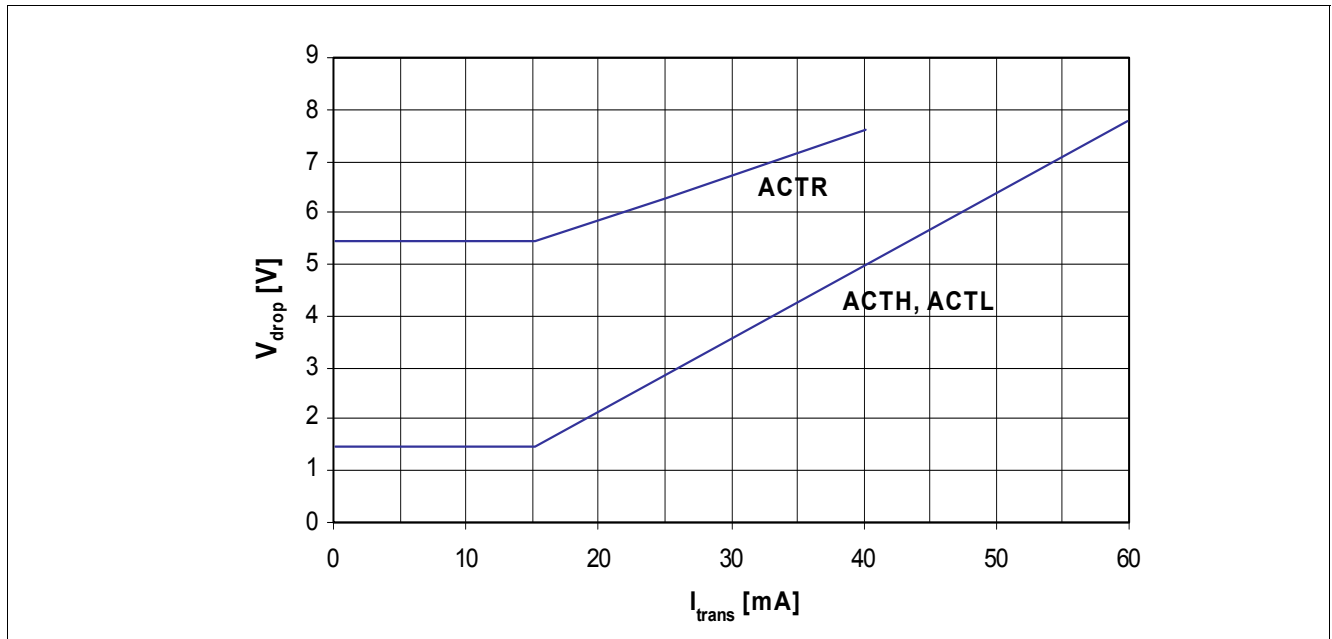


Figure 10 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR

### 4.5.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 14 AC Characteristics

| Parameter                                                                                                                                       | Symbol               | Values |      |       | Unit | Note / Test Condition                                                                                                               | No. |
|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------|------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------|-----|
|                                                                                                                                                 |                      | Min.   | Typ. | Max.  |      |                                                                                                                                     |     |
| Line Termination TIP, RING                                                                                                                      |                      |        |      |       |      |                                                                                                                                     |     |
| Receive gain (see <a href="#">Figure 18</a> )                                                                                                   | $G_r$                | 5.925  | 6.0  | 6.075 | –    | $V_{ACP} - V_{ACN} = 640 \text{ mV}_{\text{rms}}$ ,<br>$f = 1015 \text{ Hz}$                                                        | 58  |
| Total harmonic distortion $V_{\text{TR}}$<br>(see <a href="#">Figure 18</a> )                                                                   | $THD$                | –      | 0.01 | –     | %    | $V_{ACP} - V_{ACN} = 640 \text{ mV}_{\text{rms}}$ ,<br>$f = 1015 \text{ Hz}$                                                        | 59  |
| Teletax distortion                                                                                                                              | $THD_{TTX}$          | –      | 0.1  | –     | %    | $V_{\text{TR,AC}} = 5 \text{ V}_{\text{rms}}$ , $f = 16 \text{ kHz}$ ,<br>$R_L = 200 \Omega$                                        | 60  |
|                                                                                                                                                 |                      | –      | 0.2  | –     | %    | $V_{\text{TR,AC}} = 5 \text{ V}_{\text{rms}}$ , $f = 16 \text{ kHz}$ ,<br>$R_L = 200 \Omega$ , $I_{\text{Trans,DC}} = 0 \text{ mA}$ | 61  |
| Psophometric noise<br>(see <a href="#">Figure 18</a> )                                                                                          | $N_{\text{pVTR}}$    | –      | –82  | –78   | dBmp | –                                                                                                                                   | 62  |
| Longitudinal to transversal<br>rejection ratio $V_{\text{long}}/V_{\text{TR}}$<br>(see <a href="#">Figure 19</a> )                              | $LTRR$               | –      | 80   | –     | dB   | $V_{\text{long}} = 3 \text{ V}_{\text{rms}}$ ,<br>$300 \text{ Hz} < f < 3.4 \text{ kHz}$                                            | 63  |
| Longitudinal to transversal<br>rejection ratio $V_{\text{long}}/V_{\text{TR}}$ (loop)<br>PEF 4265, PEF 4365<br>(see <a href="#">Figure 19</a> ) | $LTRR_{\text{loop}}$ | 54     | 58   | –     | dB   | $V_{\text{long}} = 3 \text{ V}_{\text{rms}}$<br>$300 \text{ Hz} < f < 1\text{kHz}$                                                  | 64  |
|                                                                                                                                                 |                      | 52     | 56   | –     | dB   | $f = 3.4 \text{ kHz}$                                                                                                               | 65  |

**Electrical Characteristics**
**Table 14 AC Characteristics (cont'd)**

| Parameter                                                                                                                                               | Symbol                 | Values |      |      | Unit | Note / Test Condition                                                                                        | No. |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|--------|------|------|------|--------------------------------------------------------------------------------------------------------------|-----|
|                                                                                                                                                         |                        | Min.   | Typ. | Max. |      |                                                                                                              |     |
| Longitudinal to transversal rejection ratio $V_{\text{long}}/V_{\text{TR}}$ (loop)<br>PEF 4265-2<br>(see <a href="#">Figure 19</a> )                    | $LTRR-2_{\text{loop}}$ | 61     | 65   | –    | dB   | $V_{\text{long}} = 3 V_{\text{rms}}$<br>$300 \text{ Hz} < f < 1 \text{ kHz}$                                 | 66  |
|                                                                                                                                                         |                        | 56     | 60   | –    | dB   | $f = 3.4 \text{ kHz}$                                                                                        | 67  |
| Transversal to longitudinal rejection ratio $V_{\text{TR}}/V_{\text{long}}$ (see <a href="#">Figure 21</a> )                                            | $TLRR$                 | 48     | 60   | –    | dB   | $V_{\text{ACP}} - V_{\text{ACN}} = 1920 \text{ mV}_{\text{rms}}$ ,<br>$300 \text{ Hz} < f < 3.4 \text{ kHz}$ | 68  |
| Power supply rejection ratio<br>(see <a href="#">Figure 11</a> , <a href="#">Figure 12</a> ,<br><a href="#">Figure 14</a> , <a href="#">Figure 14</a> ) | $PSRR$                 |        |      |      |      | $V_{\text{SupplyAC}} = 100 \text{ mV}_p$ ,<br>$300 \text{ Hz} < f < 3.4 \text{ kHz}$                         |     |
| $V_{\text{BATL}}/V_{\text{TR}}$                                                                                                                         |                        | 40     | 60   | –    | dB   |                                                                                                              | 69  |
| $V_{\text{BATH}}/V_{\text{TR}}$                                                                                                                         |                        | 40     | 60   | –    | dB   |                                                                                                              | 70  |
| $V_{\text{HR}}/V_{\text{TR}}$                                                                                                                           |                        | 33     | 50   | –    | dB   |                                                                                                              | 71  |
| $V_{\text{DD}}/V_{\text{TR}}$                                                                                                                           |                        | 33     | 50   | –    | dB   |                                                                                                              | 72  |
| Interchannel crosstalk <sup>1)</sup>                                                                                                                    |                        |        | -80  | –    | dB   | $300 \text{ Hz} < f < 3.4 \text{ kHz}$<br>both channels active                                               | 73  |
|                                                                                                                                                         |                        |        | -80  | –    | dB   | One channel active,<br>one channel power down                                                                | 74  |
| Ringing amplitude TIP/RING                                                                                                                              | $V_{\text{RNG0}}$      | –      | 85   | –    | Vrms | $V_{\text{DCP}} - V_{\text{DCN}} = 0.15 \text{ V (DC)}$<br>$+ 1.42 V_{\text{rms}}$ (sine wave,<br>20Hz)      | 75  |
| Ringing distortion (see <a href="#">Figure 22</a> )                                                                                                     | RD                     | –      | 0.1  | –    | %    | $R_R = 450 \Omega$ , $C_R = 3.4 \mu\text{F}$ ,<br>Mode: ACTR                                                 | 76  |

**Transversal Current IT<sup>2)</sup>**

|                                                                                                                                |                   |      |      |      |      |                                                                                            |    |
|--------------------------------------------------------------------------------------------------------------------------------|-------------------|------|------|------|------|--------------------------------------------------------------------------------------------|----|
| Transversal current ratio<br>(see <a href="#">Figure 18</a> )                                                                  | $I/G_{\text{it}}$ |      |      |      |      | $V_{\text{ACP}} - V_{\text{ACN}} = 640 \text{ mV}_{\text{rms}}$ ,<br>$f = 1015 \text{ Hz}$ |    |
|                                                                                                                                |                   | 49.5 | 50   | 50.5 |      | $I_{\text{Trans,DC}} = 25 \text{ mA}$                                                      | 77 |
|                                                                                                                                |                   | 49   | 50   | 51   |      | $I_{\text{Trans,DC}} = -25 \text{ mA}$                                                     | 78 |
| Total harmonic distortion $V_{\text{IT}}$                                                                                      | $THD_{\text{IT}}$ | –    | 0.02 | 0.3  | %    | $V_{\text{ACP}} - V_{\text{ACN}} = 640 \text{ mV}_{\text{rms}}$ ,<br>$f = 1015 \text{ Hz}$ | 79 |
| Psophometric noise<br>(see <a href="#">Figure 18</a> )                                                                         | $N_{\text{pVIT}}$ | –    | -110 | -105 | dBmp | –                                                                                          | 80 |
| Longitudinal to transversal current output rejection ratio<br>$V_{\text{long}}/V_{\text{IT}}$ (see <a href="#">Figure 19</a> ) | $LITRR$           | –    | 85   | –    | dB   | $V_{\text{long}} = 3 V_{\text{rms}}$ ,<br>$300 \text{ Hz} < f < 3.4 \text{ kHz}$           | 81 |
| Power supply rejection ratio                                                                                                   | $PSRR$            |      |      |      |      | $V_{\text{SupplyAC}} = 100 \text{ mV}_p$ ,<br>$300 \text{ Hz} < f < 3.4 \text{ kHz}$       |    |
| $V_{\text{BATL}}/V_{\text{IT}}$                                                                                                |                   | 50   | 70   | –    | dB   |                                                                                            | 82 |
| $V_{\text{BATH}}/V_{\text{IT}}$                                                                                                |                   | 50   | 70   | –    | dB   |                                                                                            | 83 |
| $V_{\text{HR}}/V_{\text{IT}}$                                                                                                  |                   | 50   | 70   | –    | dB   |                                                                                            | 84 |
| $V_{\text{DD}}/V_{\text{IT}}$                                                                                                  |                   | 50   | 70   | –    | dB   |                                                                                            | 85 |

1) Dual channel version PEF 4365 only

2) Unless otherwise specified, characteristics are valid for both DC line current directions (normal and reverse polarity)

#### 4.5.3.1 Frequency Dependence of PSRR

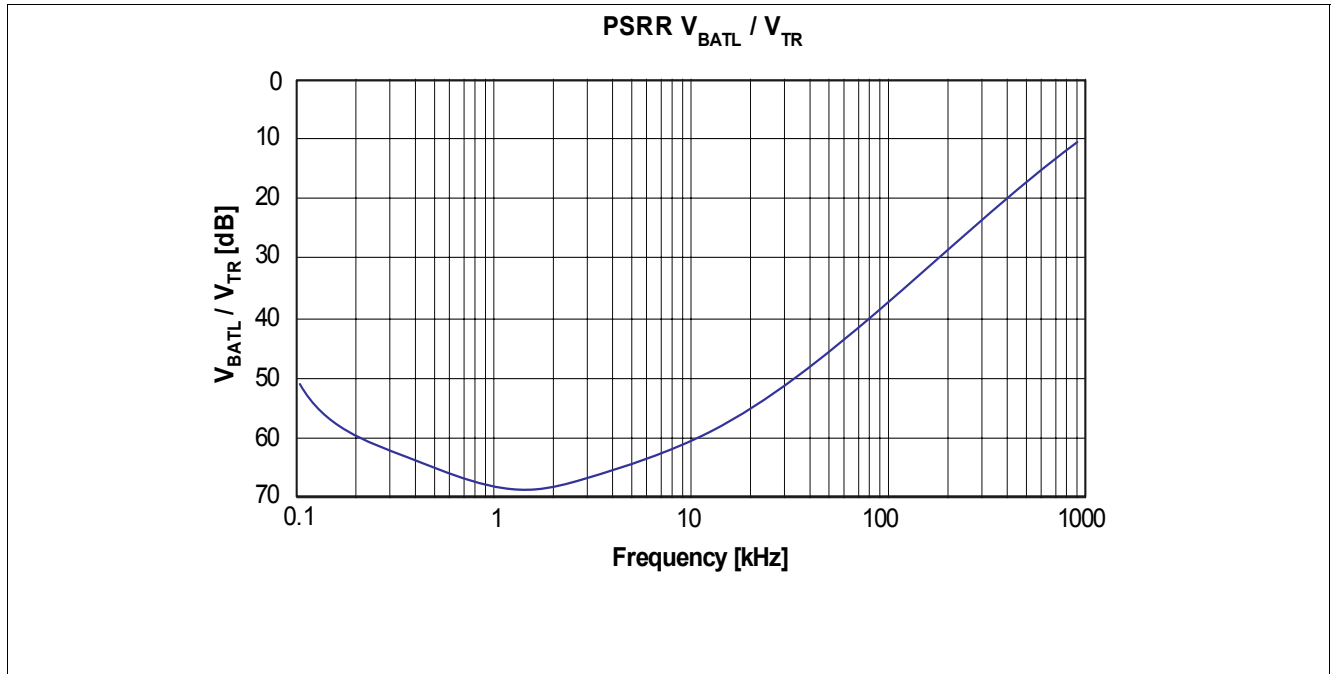


Figure 11 Typical Frequency Dependence of PSRR  $V_{BATL}/V_{TR}$

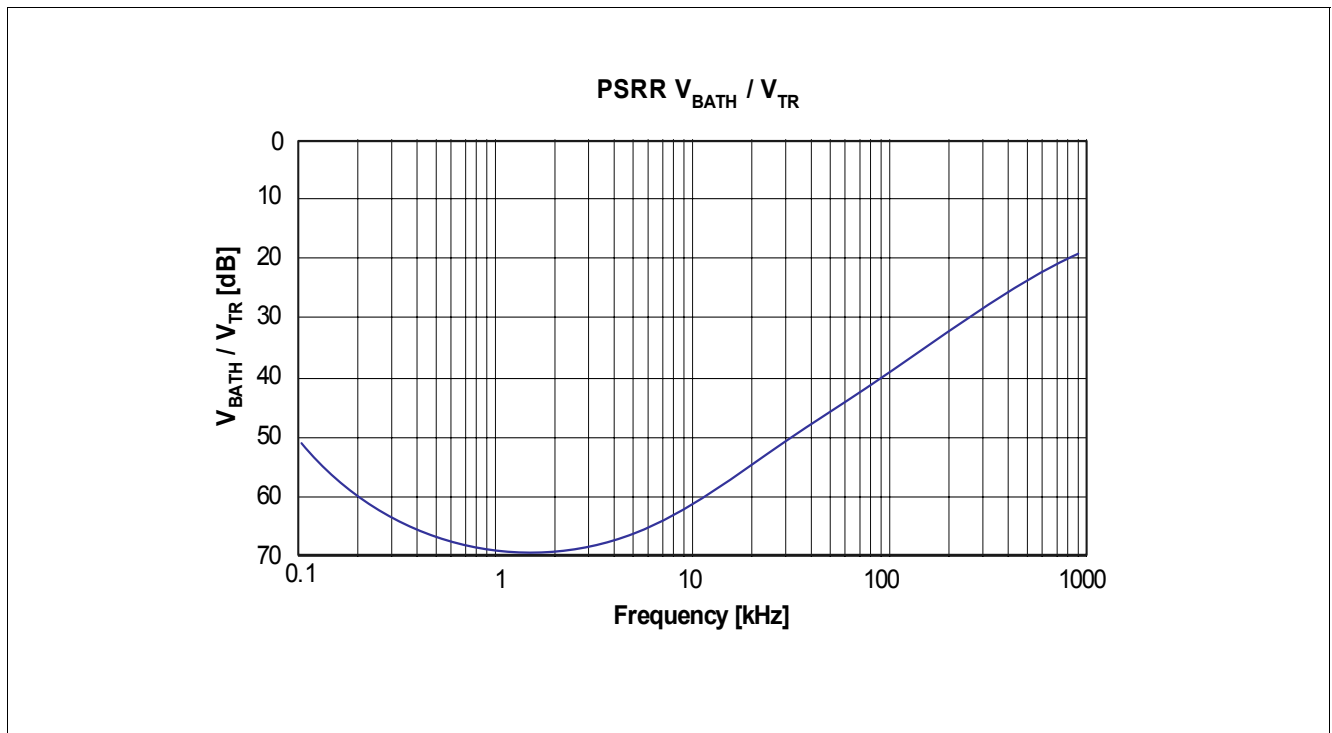


Figure 12 Typical Frequency Dependence of PSRR  $V_{BATH}/V_{TR}$

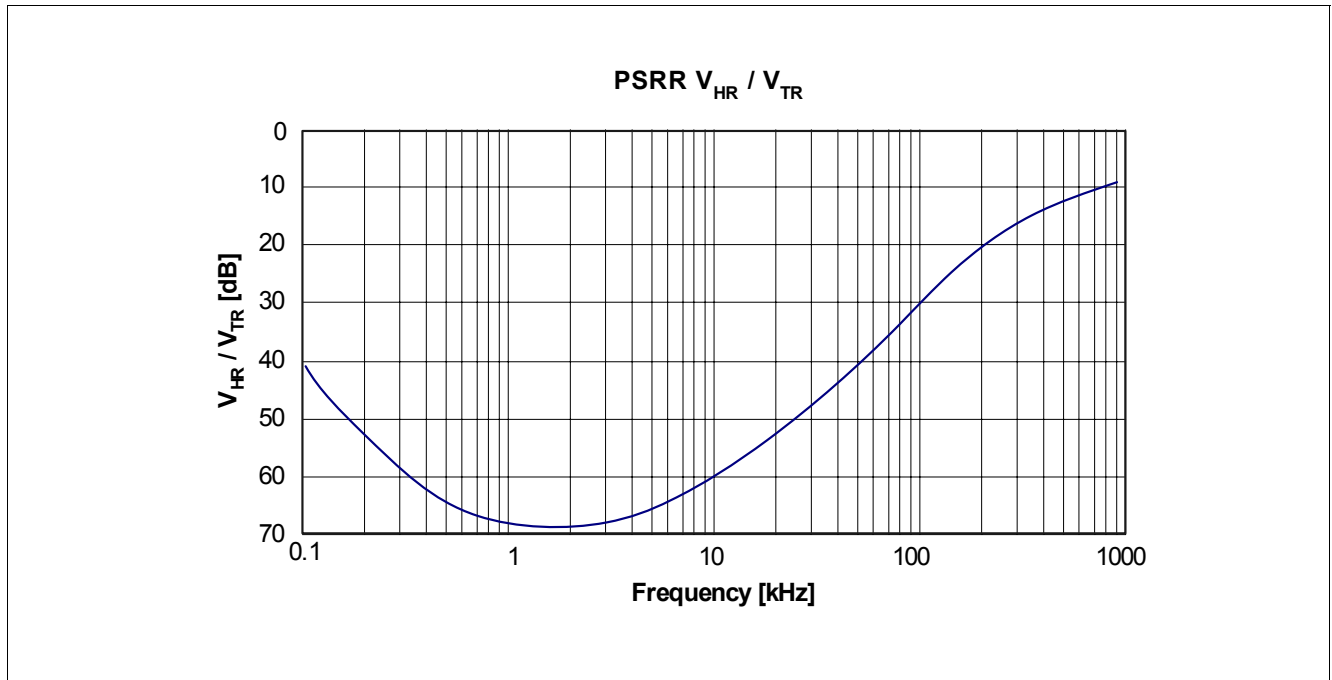


Figure 13 Typical Frequency Dependence of PSRR VHR/VTR

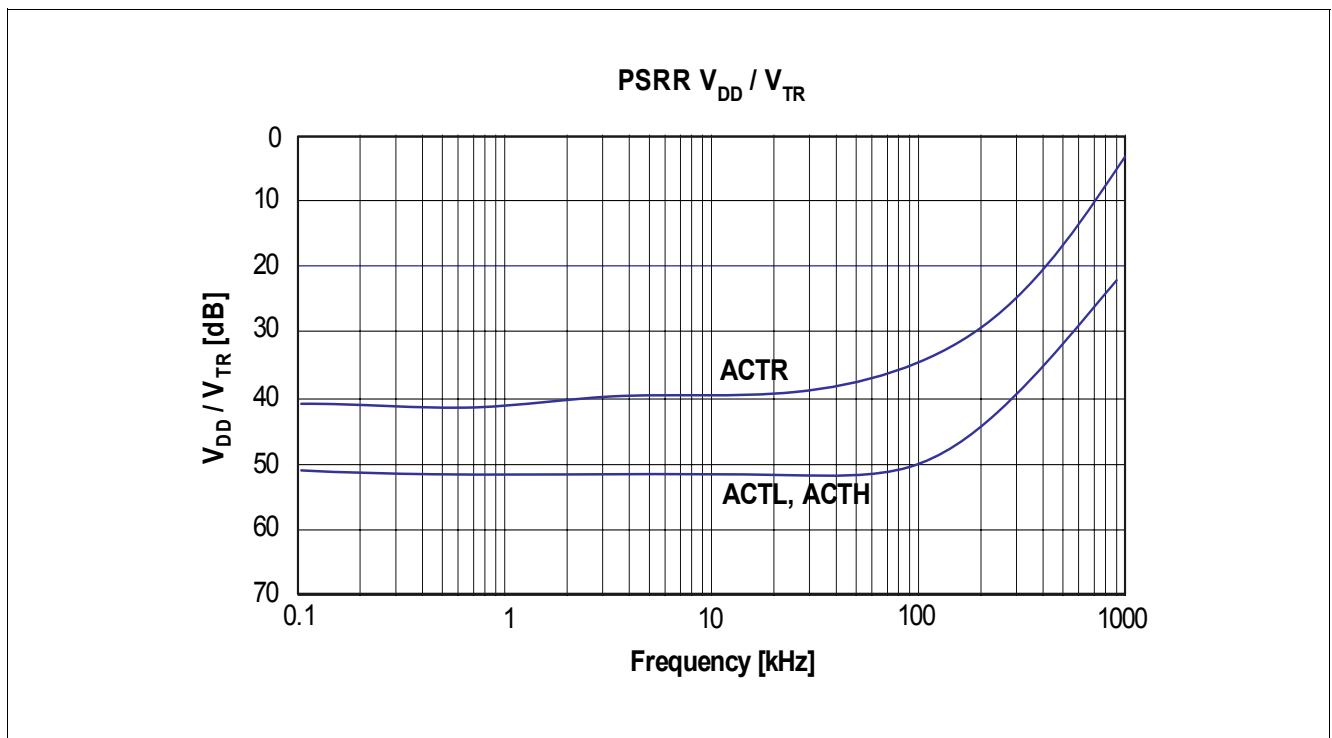


Figure 14 Typical Frequency Dependence of PSRR VDD/VTR

## 5 Test Figures

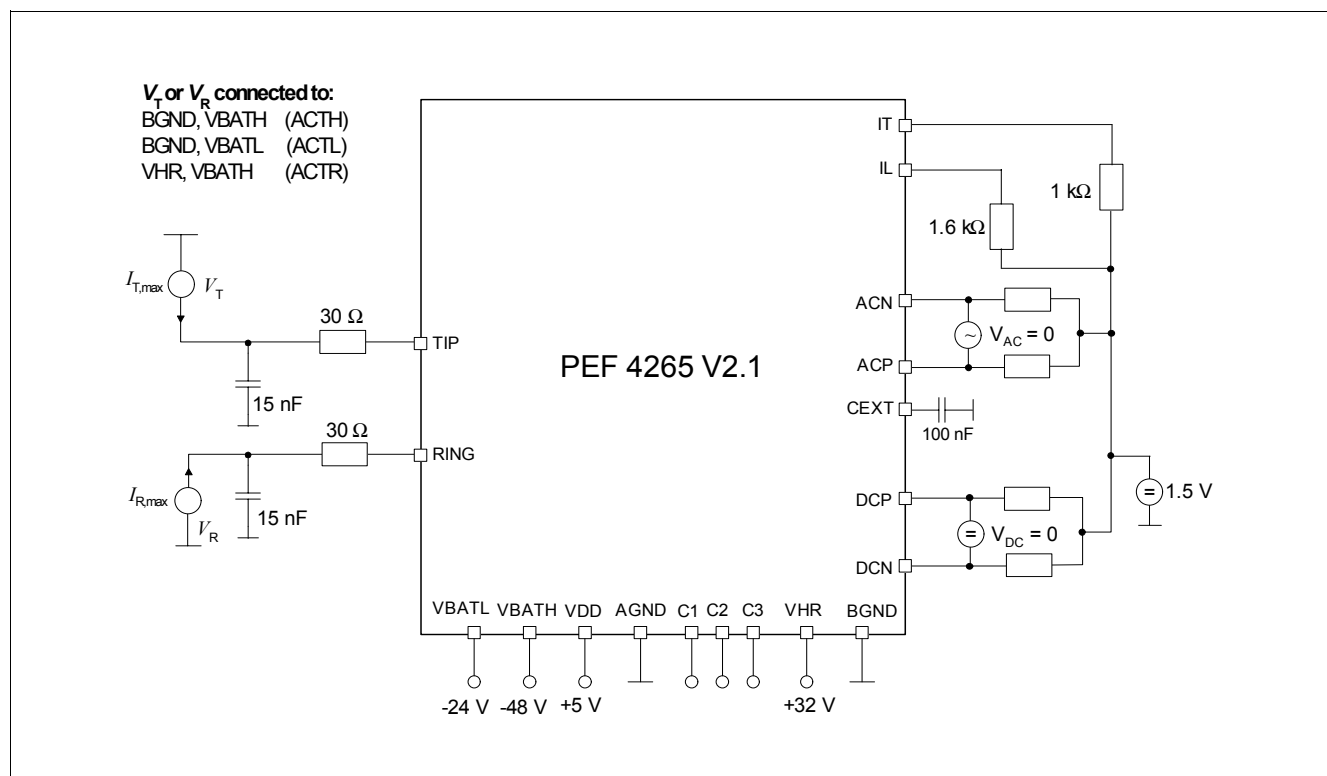


Figure 15 Output Current Limit

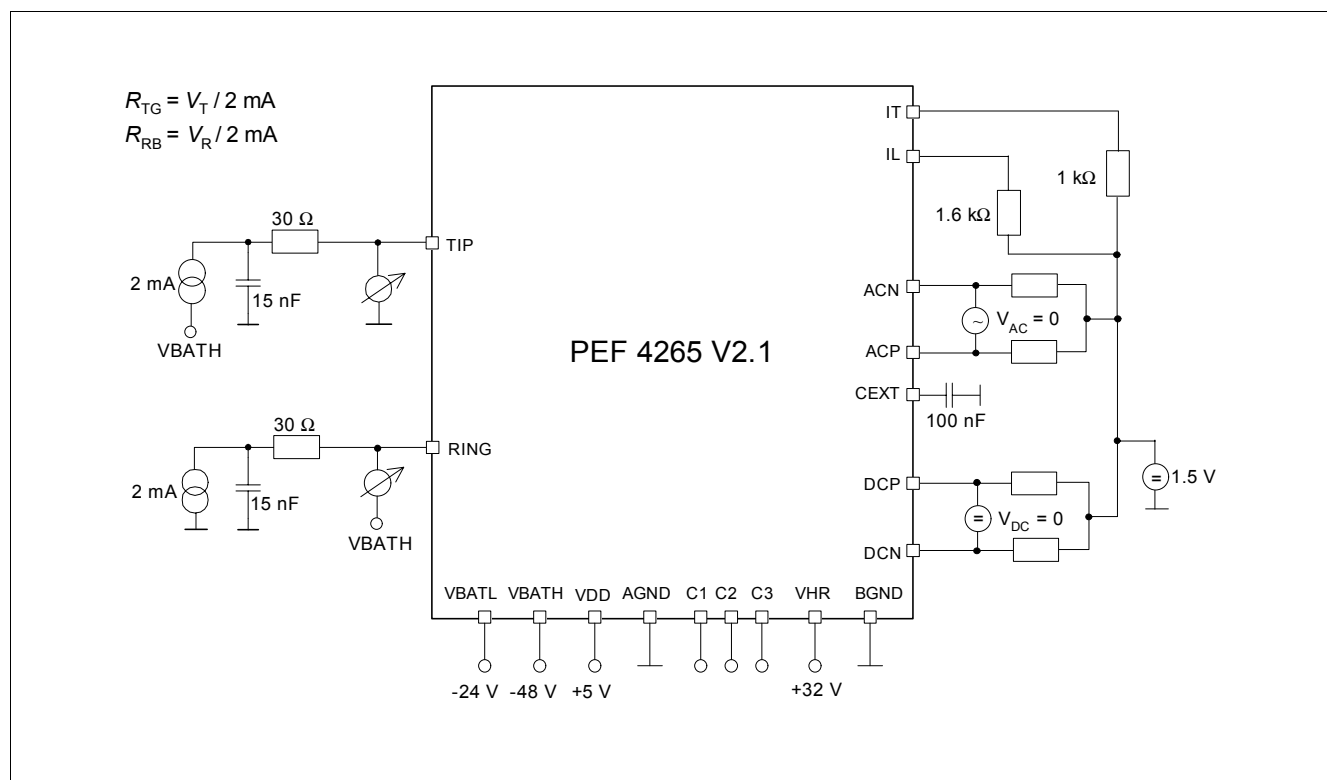


Figure 16 Output Resistance PDRH, PDRHL



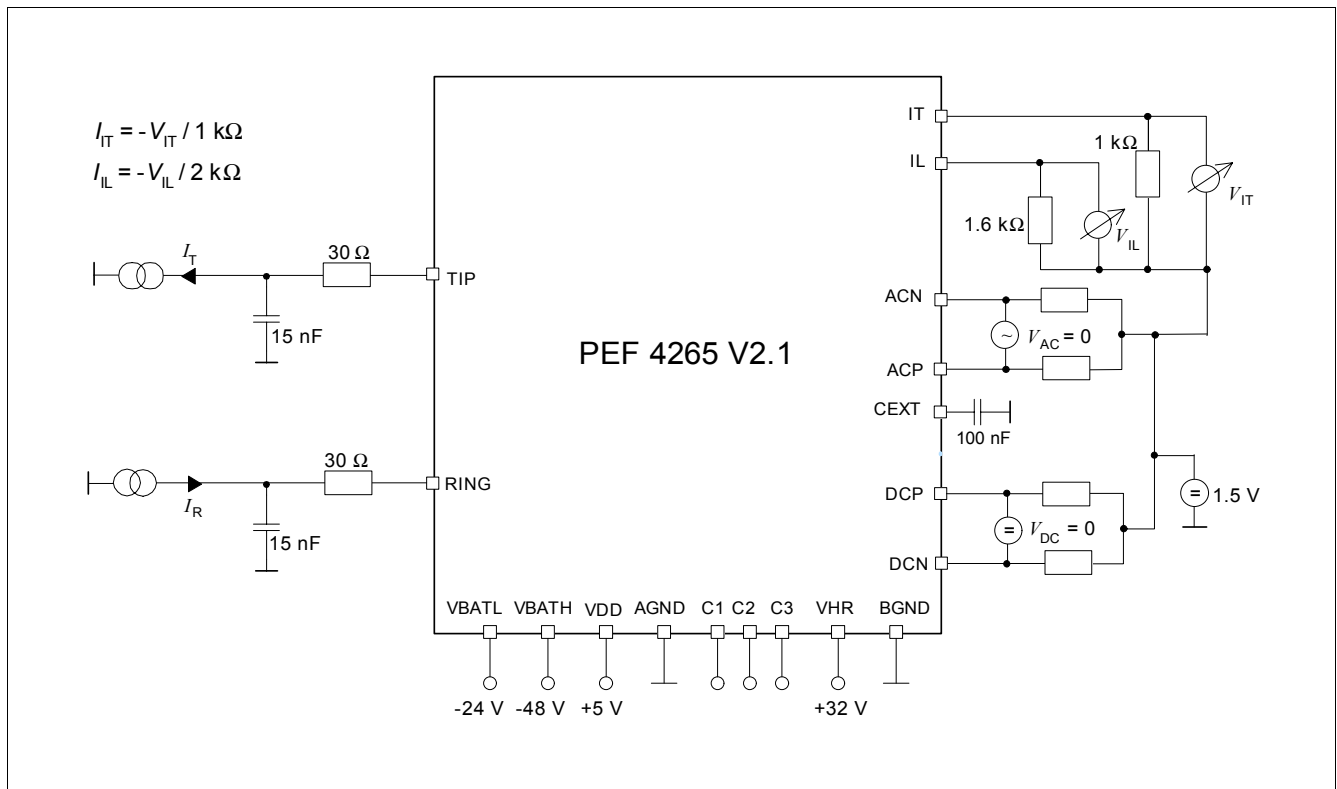


Figure 17 Current Outputs IT, IL

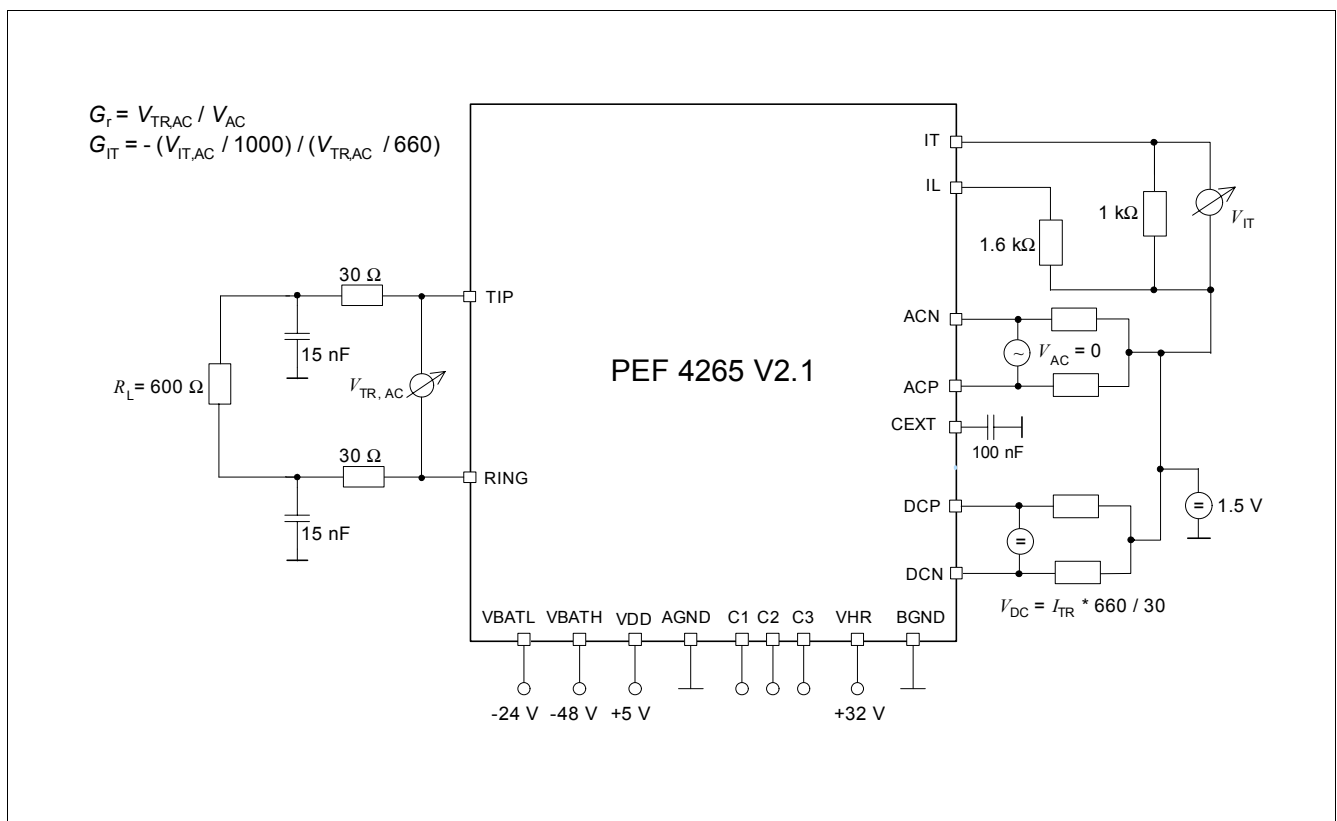


Figure 18 Transmission Characteristics

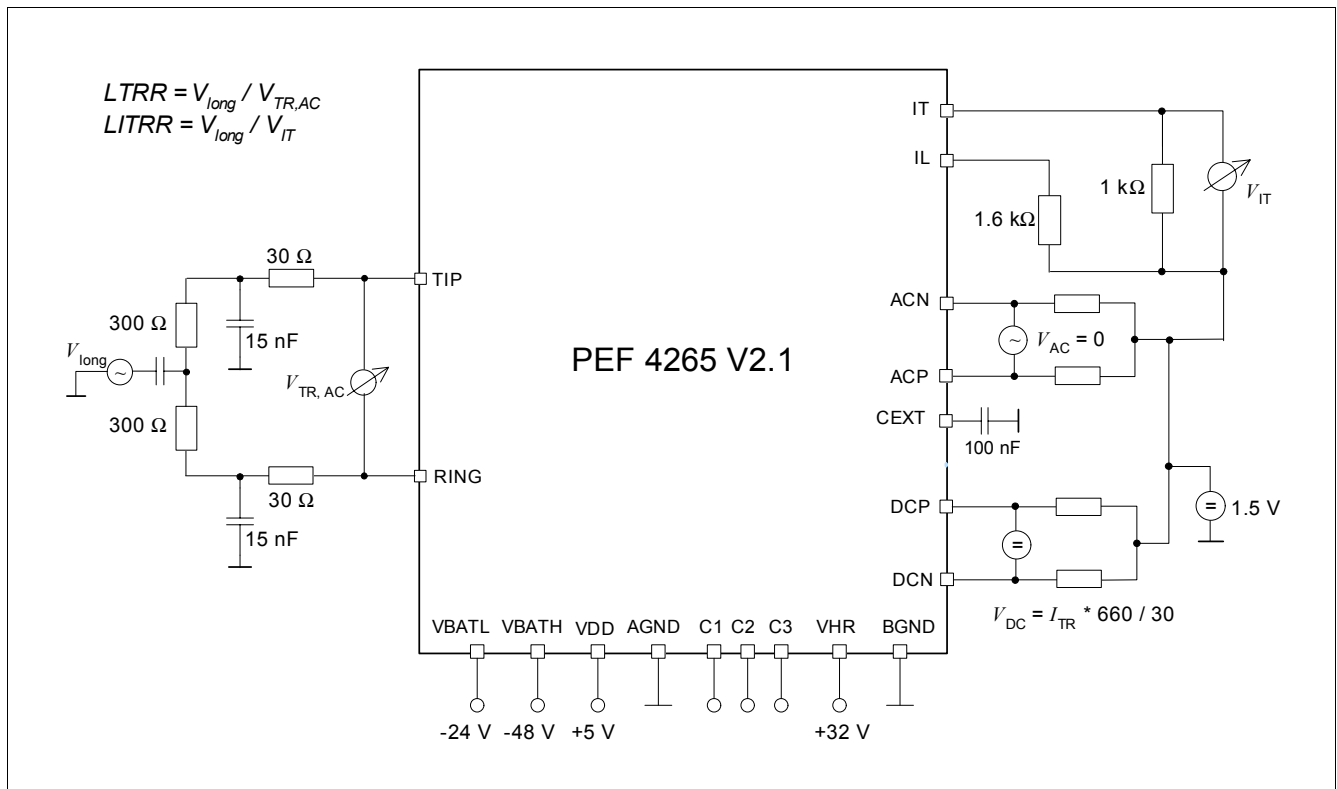


Figure 19 Longitudinal to Transversal Rejection

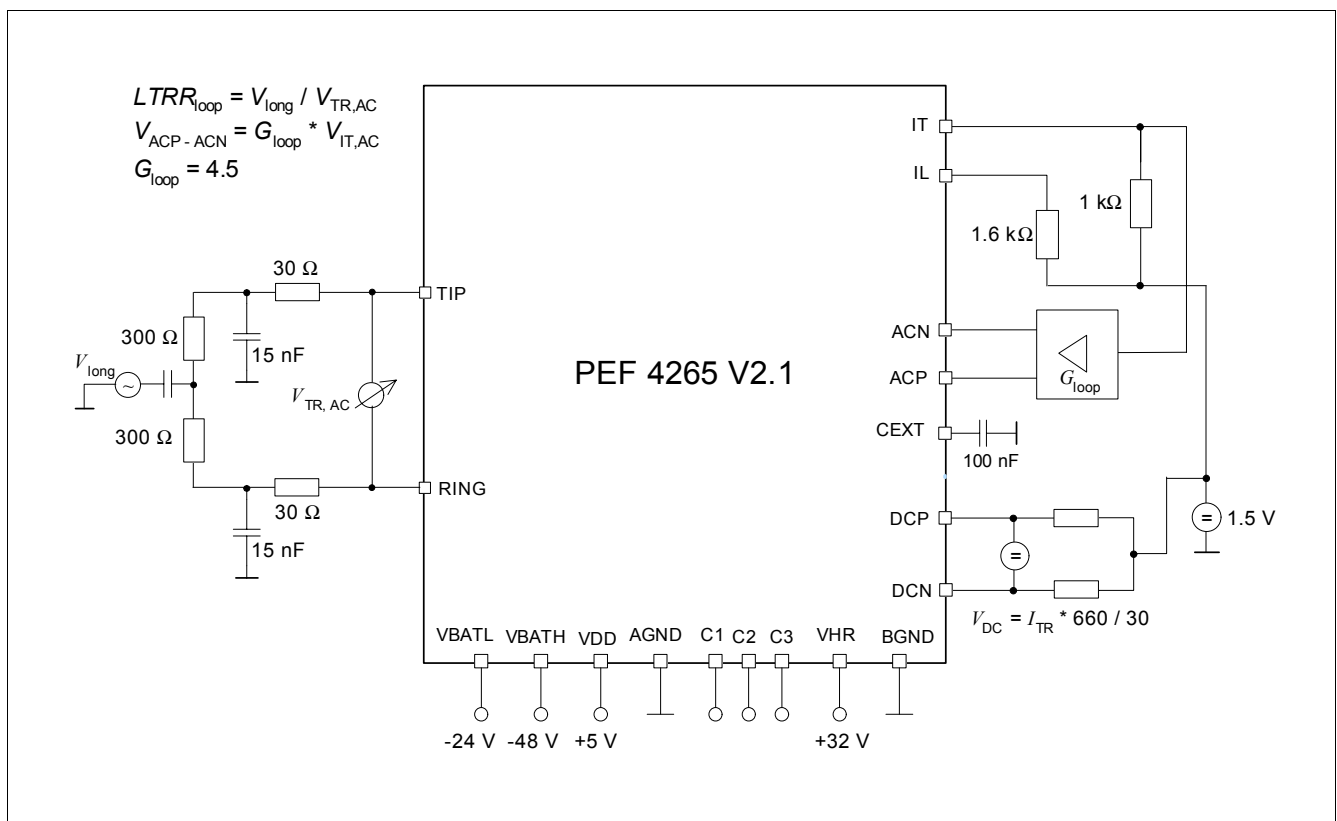


Figure 20 Longitudinal to Transversal Rejection Loop

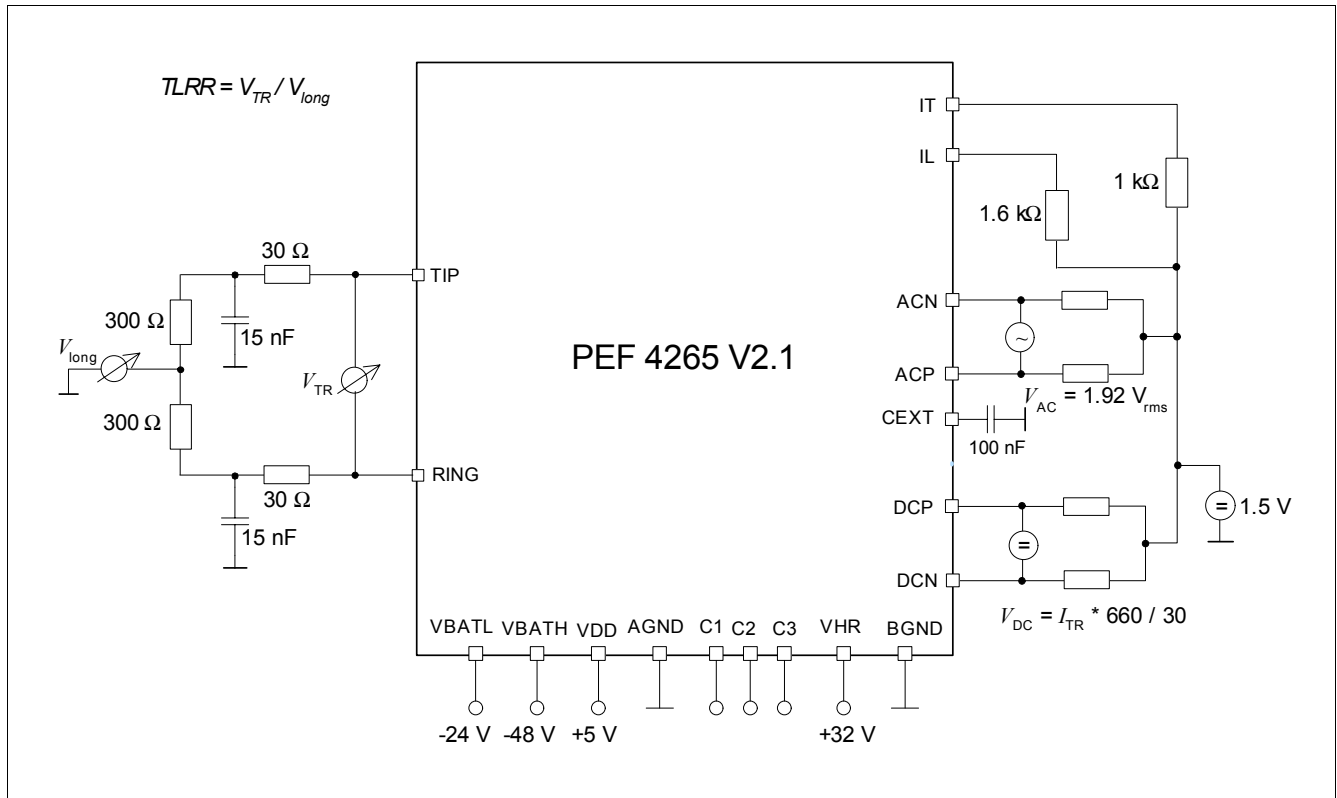


Figure 21 Transversal to Longitudinal Rejection

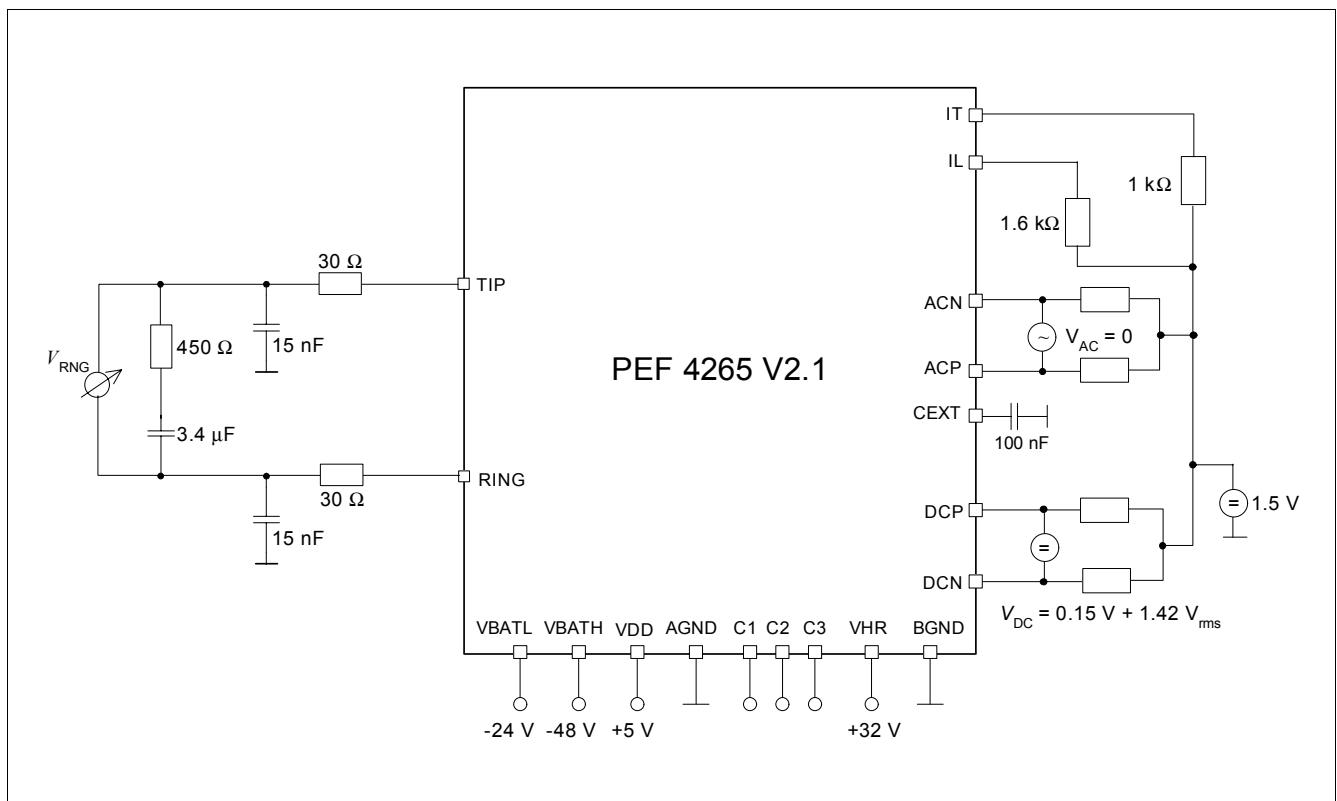
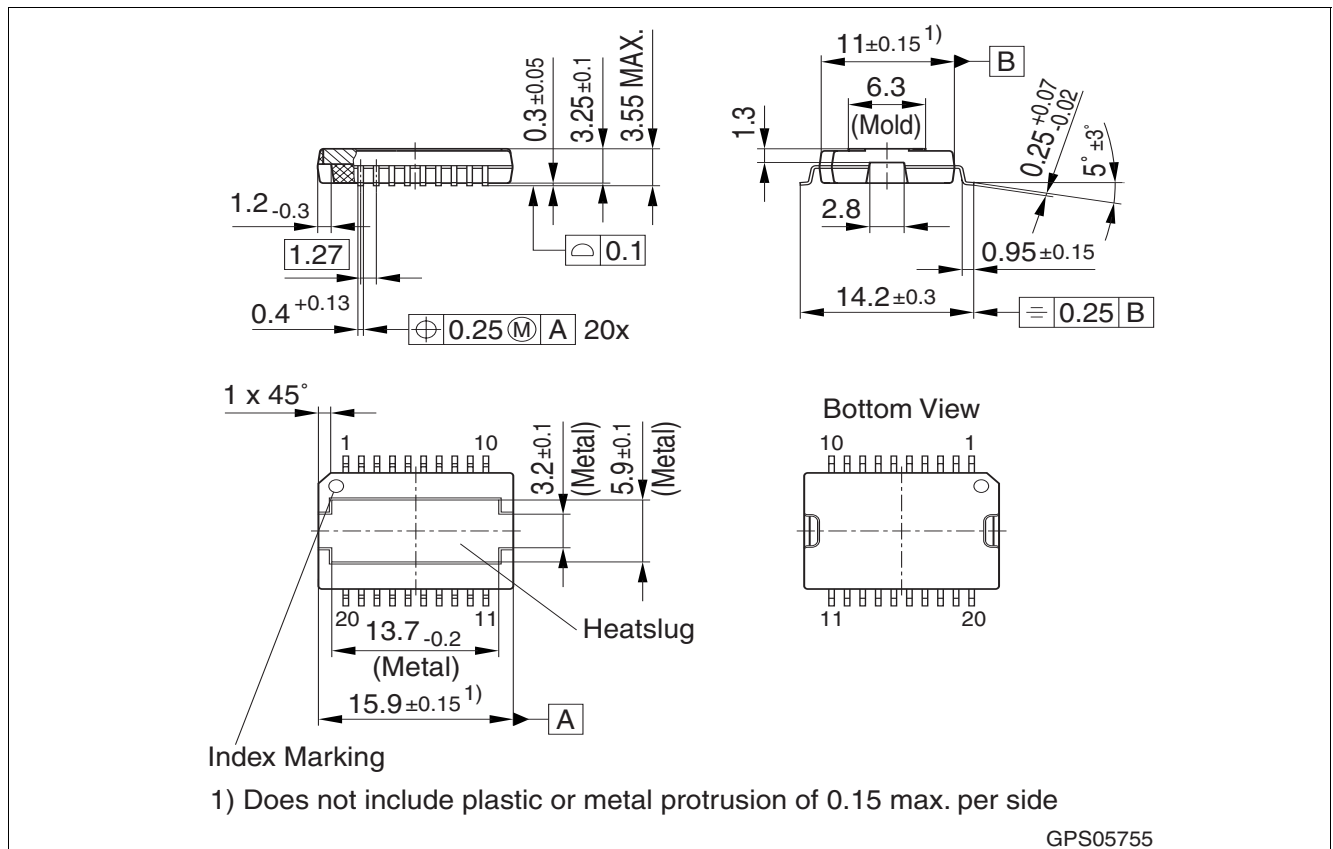


Figure 22 Ring Amplitude

## 6 Package Outlines

### 6.1 PG-DSO-20-24 Package



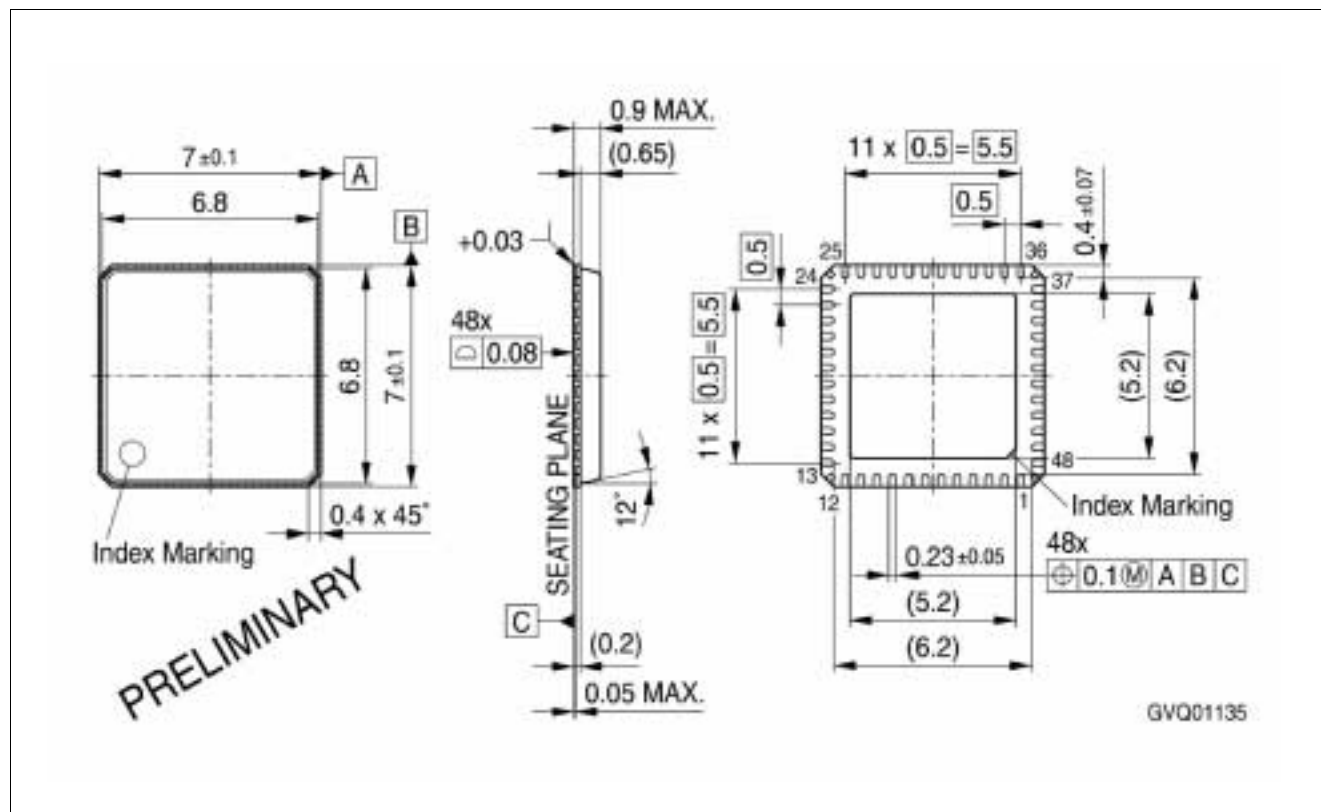
**Figure 23** Package Outline for PG-DSO-20-24 (Plastic Green Dual Small Outline)

#### Notes

1. Heatsink on top - pin counting clockwise (top view)
2. Dimensions in mm

**Attention:** The heatsink is connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

## 6.2 PG-VQFN-48-15 Package



**Figure 24** Package Outline for PG-VQFN-48-15 (Plastic Green Very thin Profile Quad Flatpack No-lead)

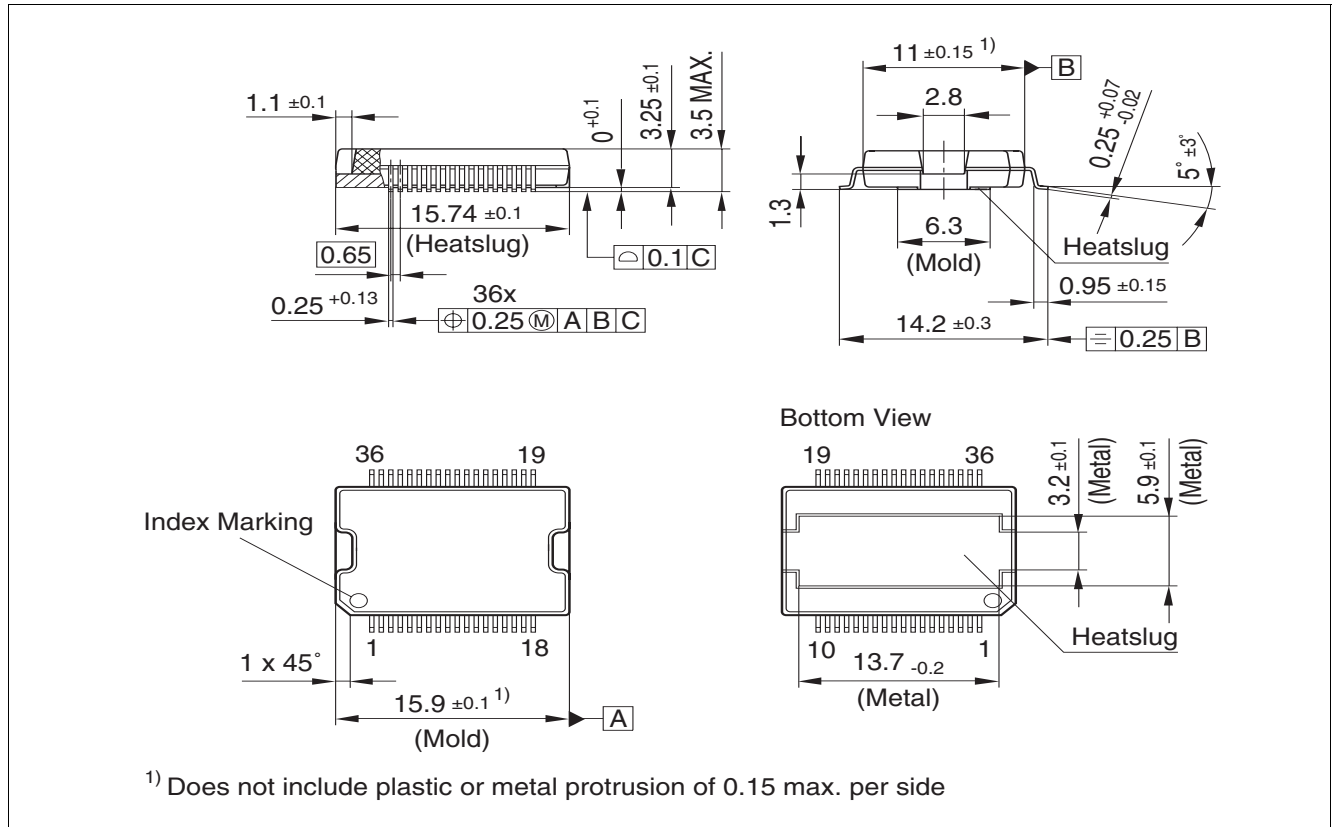
Note: Dimensions in mm

**Attention:** The exposed die pad and the die pad edges are connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the die pad or any attached conducting part can be hazardous.

### 6.2.1 Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package

For detailed information on PCB related thermal and soldering issues of the PG-VQFN-48-15 package see [3], chapter 3 and 4.

### 6.3 PG-DSO-36-15 Package



**Figure 25** Package Outline for PG-DSO-36-15 (Plastic Green Dual Small Outline)

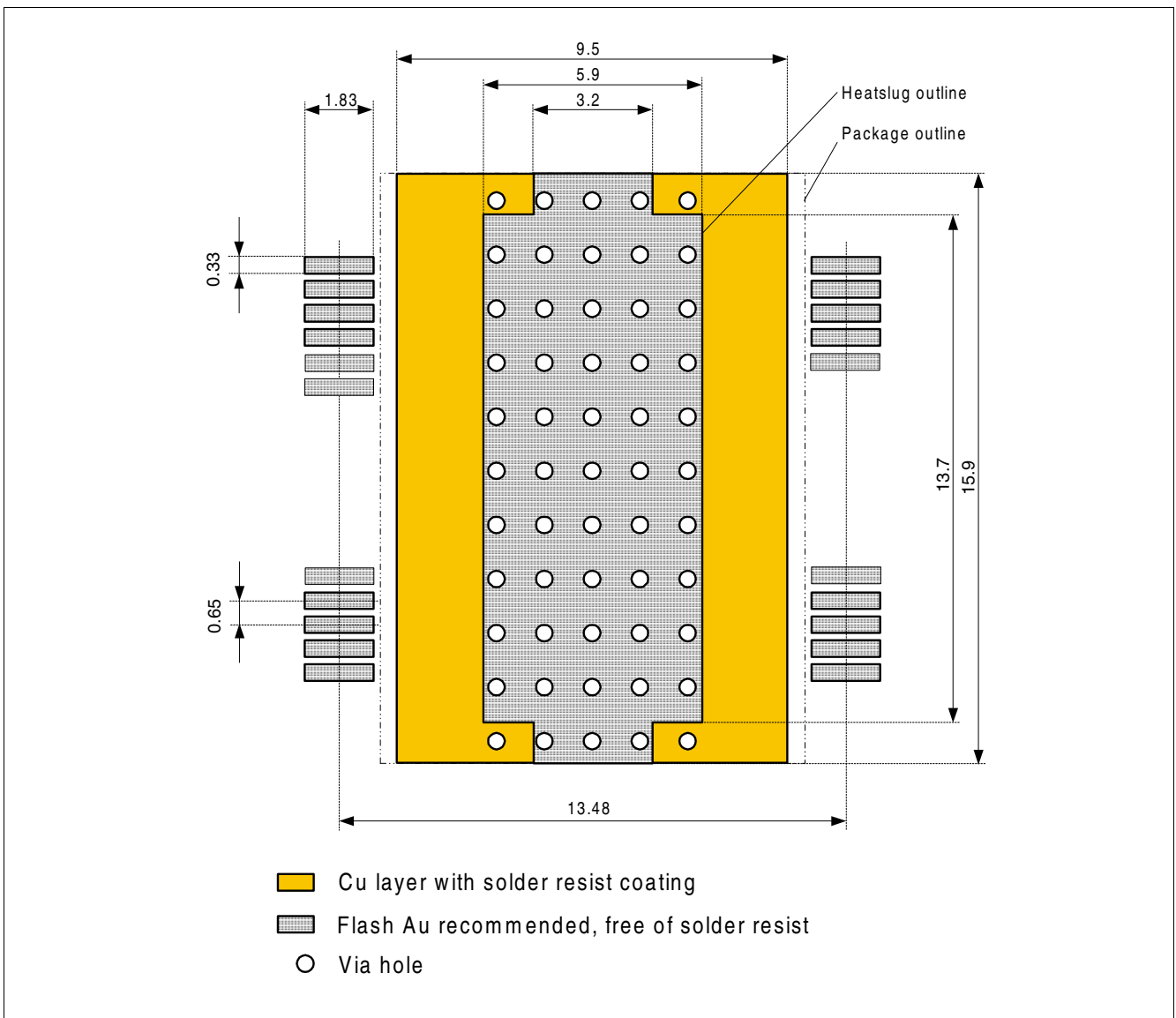
#### Notes

1. Heatslug down version - pin counting counterclockwise (top view)
2. Dimensions in mm

**Attention:** The heatslug is connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

### 6.3.1 Recommended PCB Foot Print Pattern for PG-DSO-36-15 Package

The heatslug is soldered to the PCB according to [Figure 25](#). For improved thermal behaviour the utilization of another PCB metal layer as an additional cooling area is recommended. These copper areas should be both electrically separated from each other and floating, i. e. they must not be connected with any other metallic part on the PCB.



**Figure 26** Footprint for PG-DSO-36-15

## **References**

- [1] SLIC-E/-E2 / TSLIC-E (PEB 4265/-2 / PEB 4365) Application Note "Protection for SLIC-E / -E2 against Overvoltages and Overcurrents according to ITU-T K. 20/K.21/K.45" Rev. 1.0, 2004-06-29
- [2] VINETIC® Version 1.4 Prel. Application Note External Components Rev. 2.0, 2005-09-06
- [3] Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages, Application Support, DS3, 2006-03-03



[www.infineon.com](http://www.infineon.com)