



# STP20NF06 STF20NF06

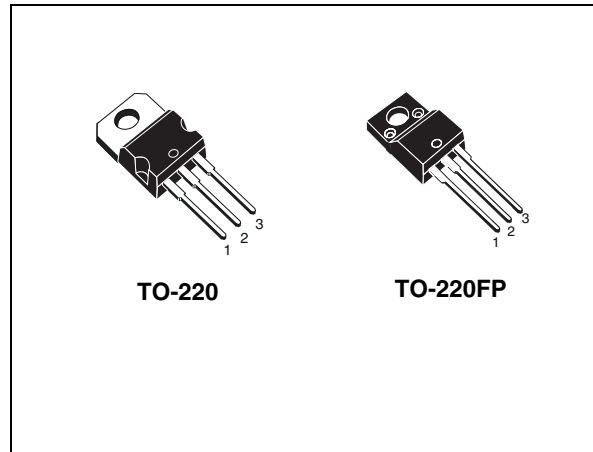
N-channel 60V - 0.06Ω - 20A - TO-220/TO-220FP  
STripFET™ II Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP20NF06	60V	<0.07Ω	20A
STF20NF06	60V	<0.07Ω	20A <sup>(1)</sup>

1. Refer to soa for the max allowable current value on FP-type due to R<sub>th</sub> value

- Avalanche rugged technology
- 100% avalanche tested
- 175°C operating temperature
- High dv/dt capability
- Application oriented characterization



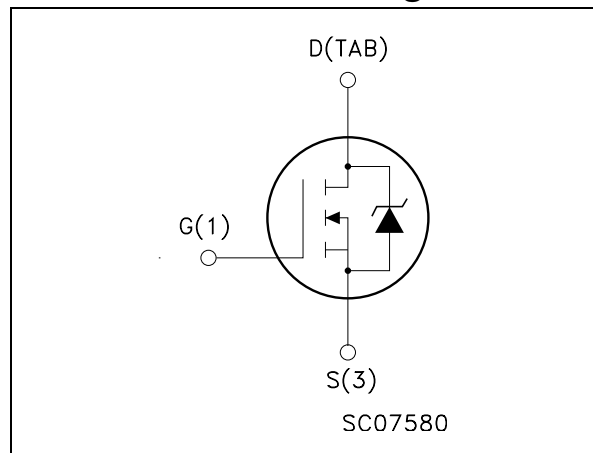
## Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

## Application

- Switching applications

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP20NF06	P20NF06	TO-220	Tube
STF20NF06	F20NF06	TO-220FP	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60		V
$V_{GS}$	Gate- source voltage	$\pm 20$		V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	20 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	14	14 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80	80 <sup>(1)</sup>	A
$P_{tot}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	28	W
	Derating factor	0.4	0.18	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	9		V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	120		mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1s; T_C=25^\circ\text{C}$ )	--	2500	V
$T_{stg}$	Storage temperature	-55 to 175		°C
$T_j$	Max. operating junction temperature			

1. Refer to SOA for the max allowable current value on FP-type due to  $R_{th}$  value

2. Pulse width limited by safe operating area.

3.  $I_{SD} \leq 20\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$

4. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 10\text{A}$ ,  $V_{DD} = 30\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	TO-220	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.5	5.35	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		°C/W
$T_J$	Maximum lead temperature for soldering purpose	300		°C

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max ratings}$ $V_{DS} = \text{max ratings}$ , $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 10\text{A}$		0.06	0.07	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 8\text{A}$		10		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		400 100 40		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30\text{V}$ , $I_D = 10\text{A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{V}$ (see <a href="#">Figure 15</a> )		5 15 15 5		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 30\text{V}$ , $I_D = 20\text{A}$ , $V_{GS} = 10\text{V}$ (see <a href="#">Figure 16</a> )		14 3 5.5	18	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				20 80	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A$ , $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A$ , $di/dt = 100A/\mu s$ , $V_{DD} = 20V$ , $T_j = 150^\circ C$ (see <a href="#">Figure 17</a> )		50 88 3.2		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

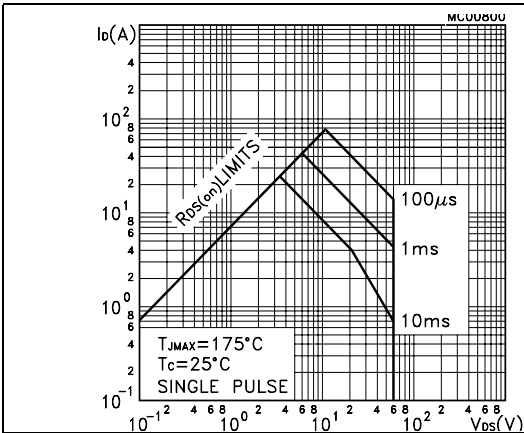


Figure 2. Thermal impedance for TO-220

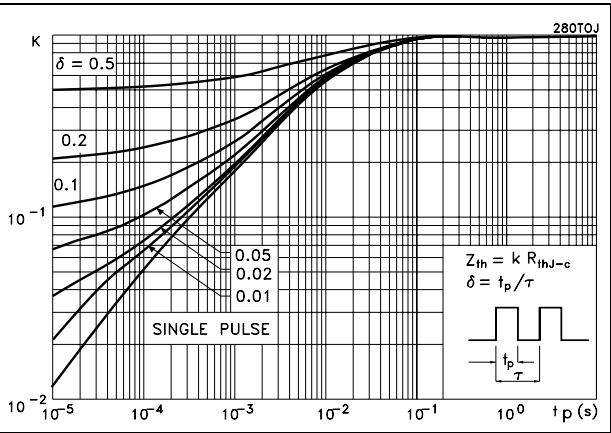


Figure 3. Safe operating area for TO-220FP

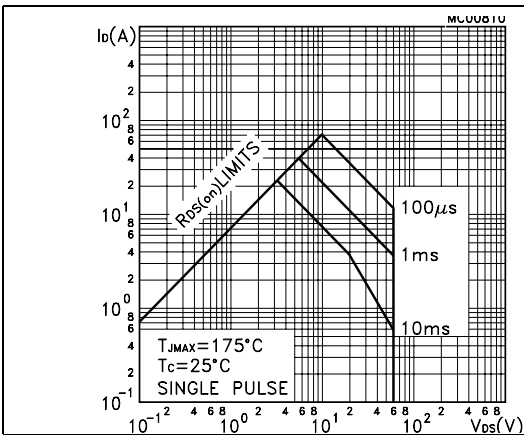


Figure 4. Thermal impedance for TO-220FP

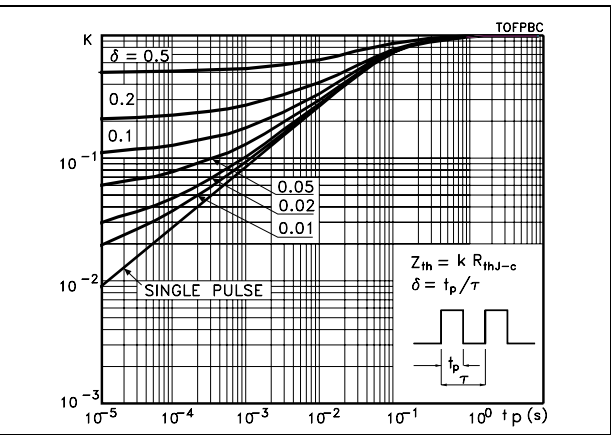


Figure 5. Output characteristics

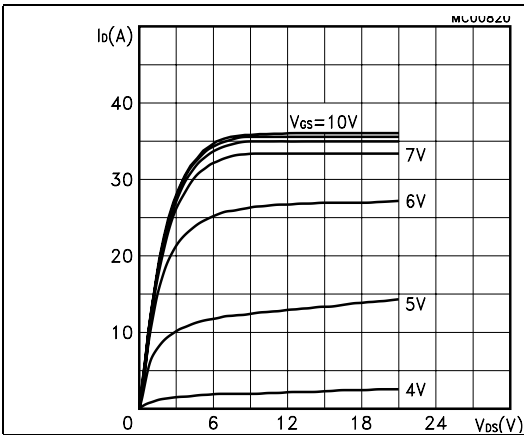


Figure 6. Transfer characteristics

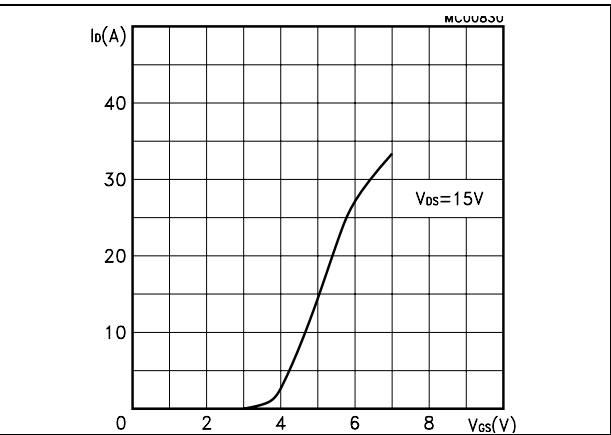


Figure 7. Transconductance

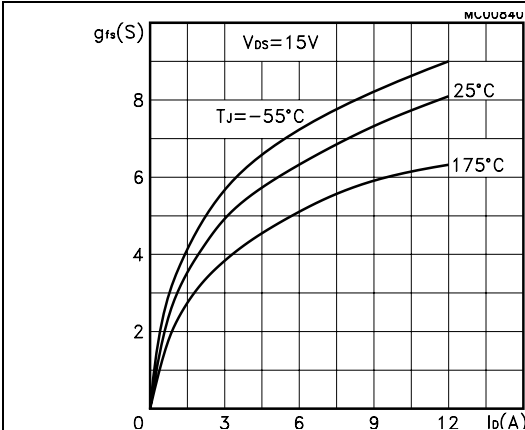


Figure 8. Static drain-source on resistance

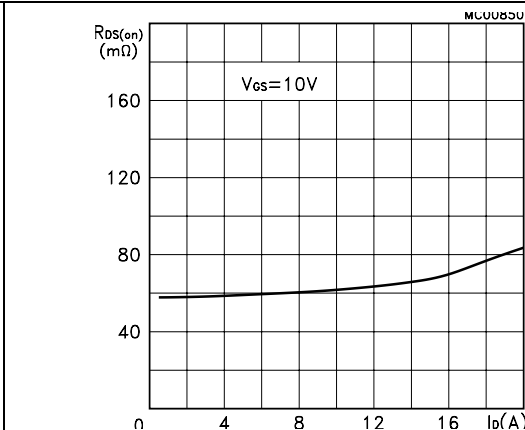


Figure 9. Gate charge vs. gate-source voltage

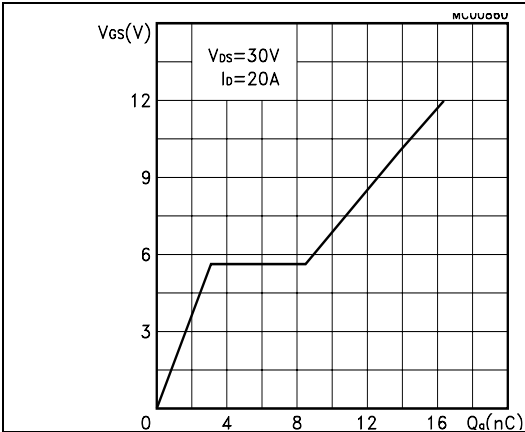


Figure 10. Capacitance variations

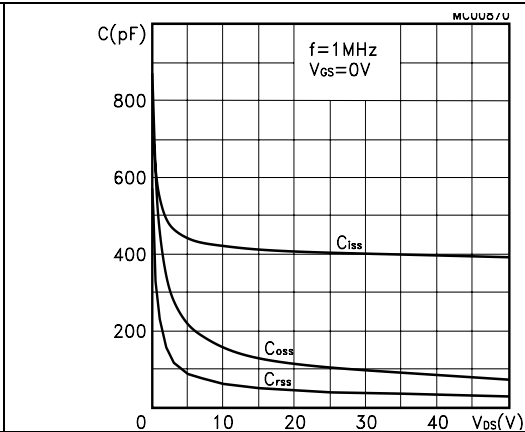


Figure 11. Normalized gate threshold voltage vs. temperature

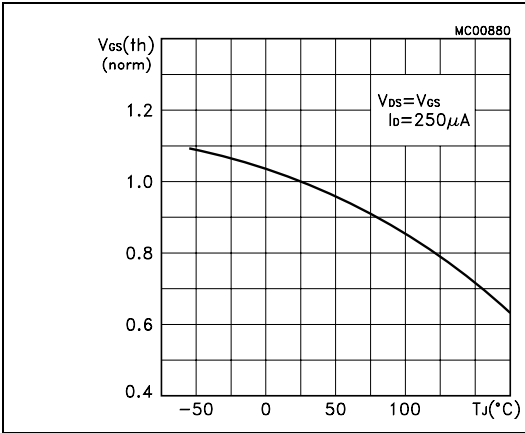


Figure 12. Normalized on resistance vs. temperature

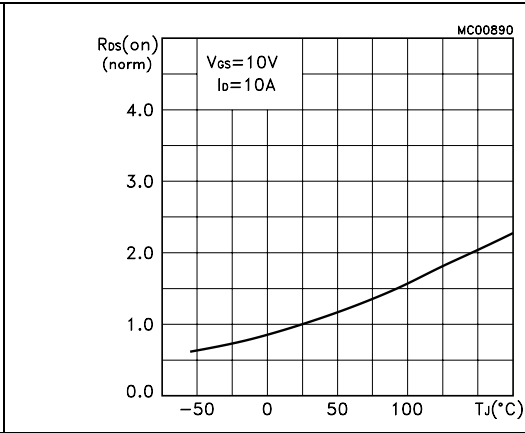


Figure 13. Source-drain diode forward characteristics

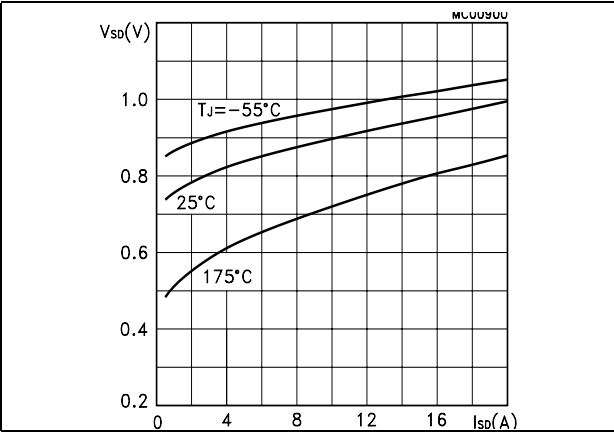
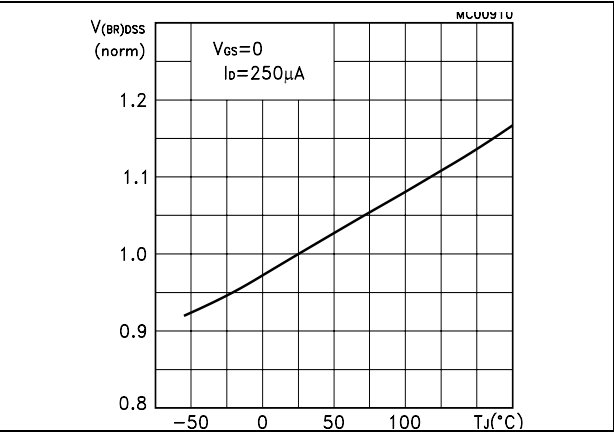


Figure 14. Normalized  $B_{V_{DSS}}$  vs. temperature





### 3 Test circuit

Figure 15. Switching times test circuit for resistive load

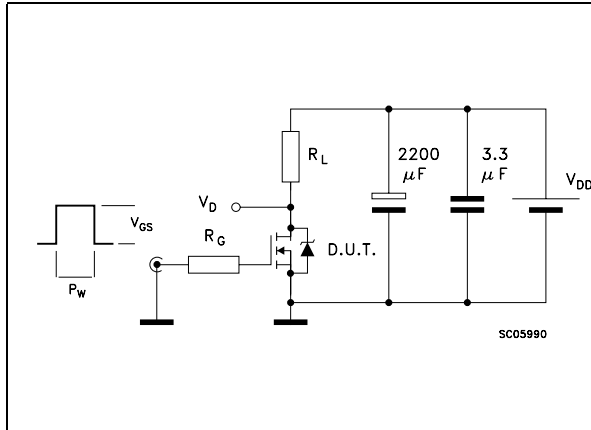


Figure 16. Gate charge test circuit

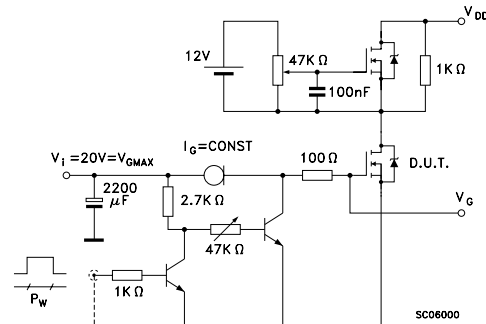


Figure 17. Test circuit for inductive load switching and diode recovery times

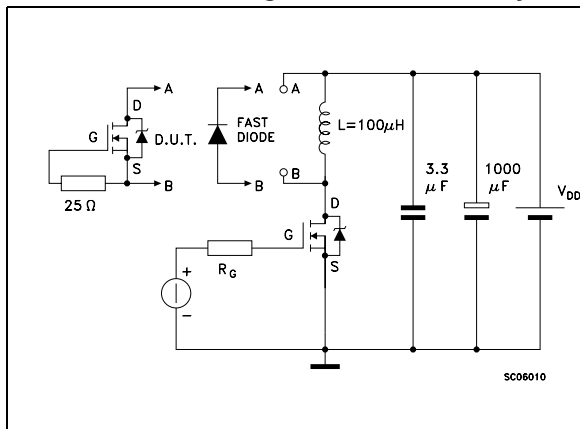


Figure 18. Unclamped Inductive load test circuit

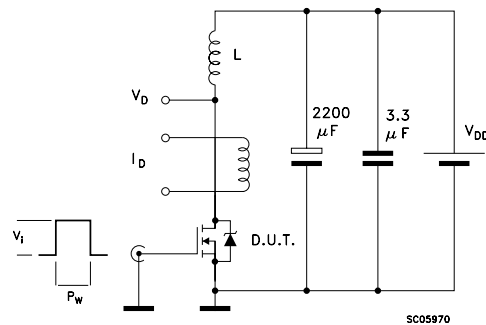


Figure 19. Unclamped inductive waveform

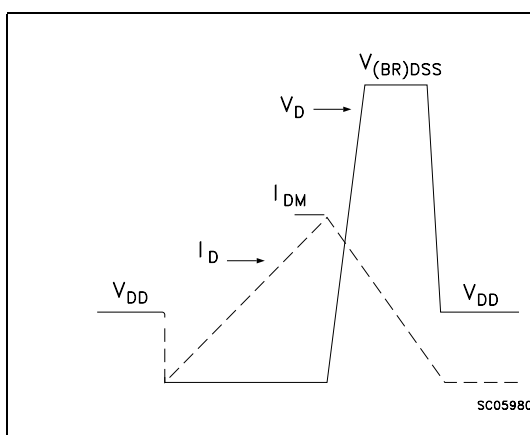
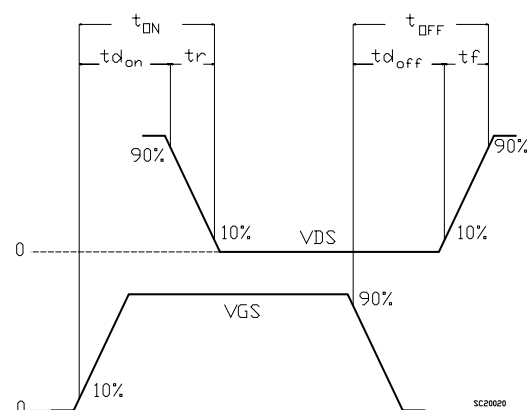


Figure 20. Switching time waveform

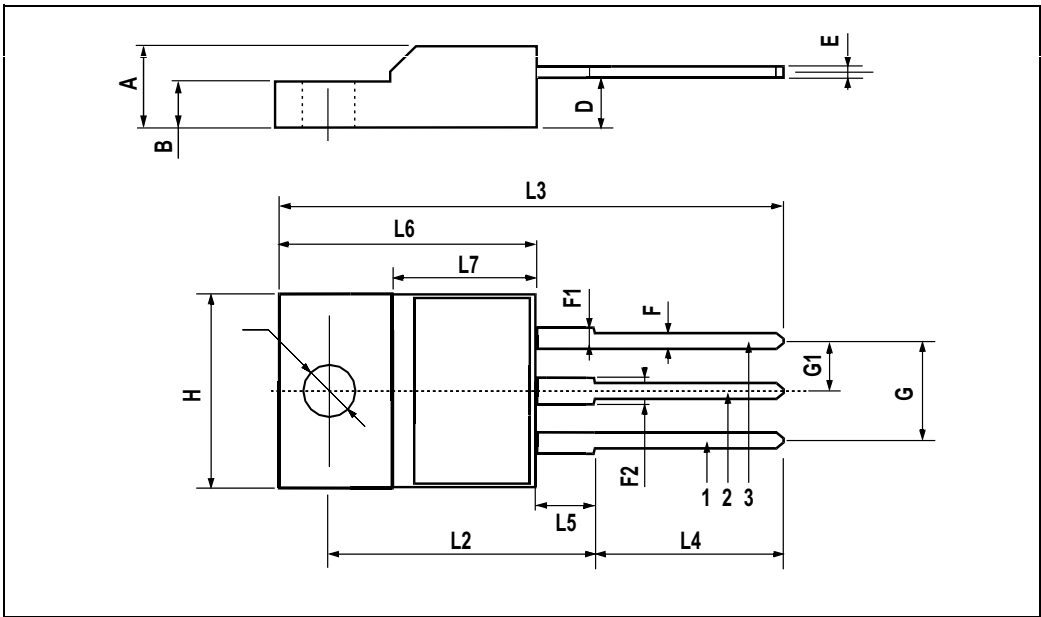


## 4 Package mechanical data

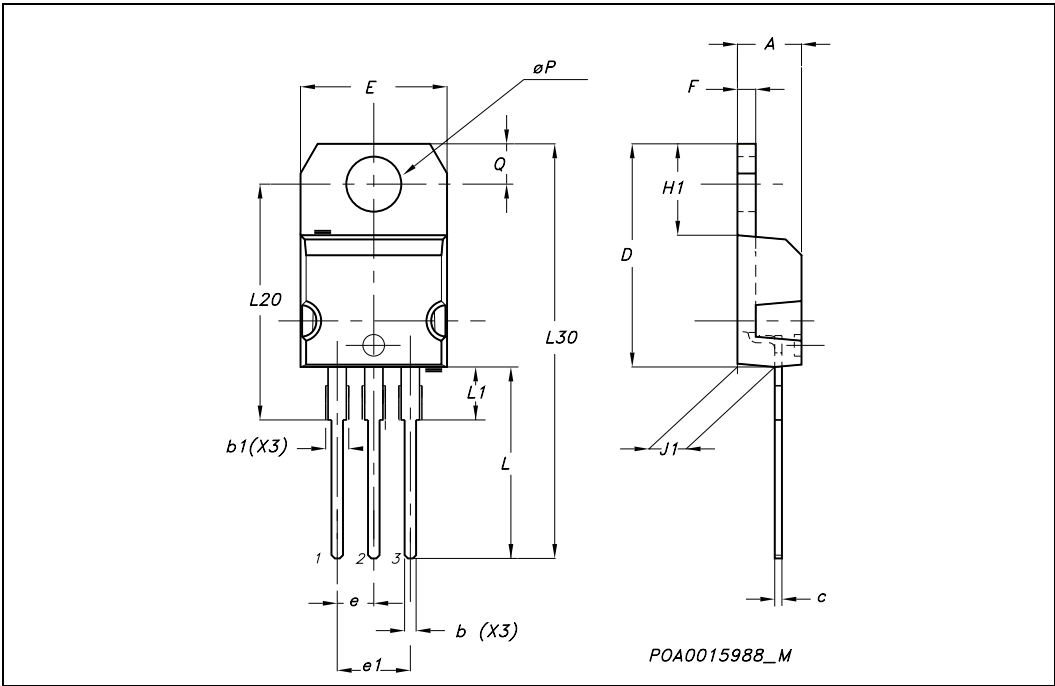
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 6. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
07-Dec-2004	1	First version
09-Aug-2006	2	The document has been reformatted
30-May-2007	3	Modified part number

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