

Field Effect Transistor - N-Channel, Logic Level, Enhancement Mode

NDS355AN

General Description

SuperSOT™-3 N-Channel logic level enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.7 A, 30 V
 - $R_{DS(on)} = 0.125 \Omega @ V_{GS} = 4.5 V$
 - $R_{DS(on)} = 0.085 \Omega @ V_{GS} = 10 V$
- Industry Standard Outline SOT-23 Surface Mount Package Using Proprietary SUPERSOT-3 Design for Superior Thermal and Electrical Capabilities
- High Density Cell Design for Extremely Low $R_{DS(on)}$
- Exceptional On-Resistance and Maximum DC Current Capability
- Compact Industry Standard SOT-23 Surface Mount Package
- This is a Pb-Free Device

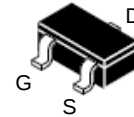
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Maximum Drain Current - Continuous (Note 1a) - Pulsed	1.7 10	A
P_D	Power Dissipation (Note 1a) (Note 1b)	0.5 0.46	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

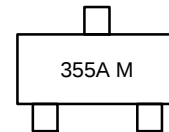
THERMAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ C/W$

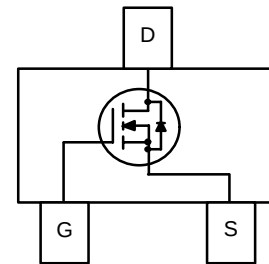


SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9
CASE 527AG

MARKING DIAGRAM



355A = Specific Device Code
M = Date Code



N-Channel

ORDERING INFORMATION

Device	Package	Shipping†
NDS355AN	SOT-23-3/ SUPERSOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NDS355AN

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 125°C	–	–	10	
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.6	2	V
		V _{DS} = V _{GS} , I _D = 250 μA, T _J = 125°C	0.5	1.2	1.5	
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 1.7 A	–	0.105	0.125	Ω
		V _{GS} = 4.5 V, I _D = 1.7 A, T _J = 125°C	–	0.16	0.23	
		V _{GS} = 10 V, I _D = 1.9 A	–	0.065	0.085	
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	6	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 1.7 A	–	3.5	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	195	–	pF
C _{oss}	Output Capacitance		–	135	–	pF
C _{rss}	Reverse Transfer Capacitance		–	48	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	10	20	ns
t _r	Turn–On Rise Time		–	13	25	ns
t _{d(off)}	Turn–Off Delay Time		–	13	25	ns
t _f	Turn–Off Fall Time		–	4	10	ns
t _{d(on)}	Turn–On Delay Time	V _{DD} = 5 V, I _D = 1 A, V _{GS} = 4.5V, R _{GEN} = 6 Ω	–	10	20	ns
t _r	Turn–On Rise Time		–	32	60	ns
t _{d(off)}	Turn–Off Delay Time		–	10	20	ns
t _f	Turn–Off Fall Time		–	5	10	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 1.7 A, V _{GS} = 5 V	–	3.5	5	nC
Q _{gs}	Gate–Source Charge		–	0.8	–	nC
Q _{gd}	Gate–Drain Charge		–	1.7	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.42	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	10	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.42 A (Note 2)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical R_{θJA} using the board layouts shown below on 4.5"x 5" FR–4 PCB in a still air environment:



a) 250°C/W when mounted on a 0.02 in² pad of 2oz copper.



b) 270°C/W when mounted on a 0.001 in² pad of 2oz copper.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

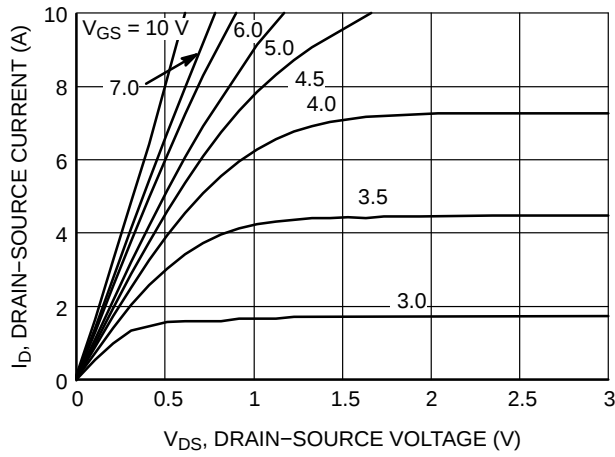


Figure 1. On-Region Characteristics

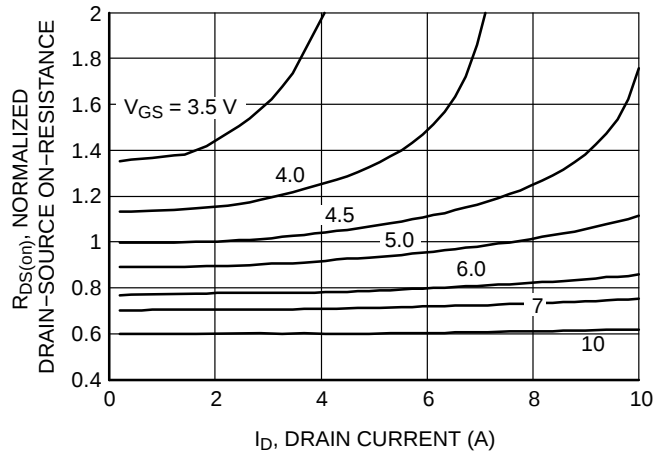


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

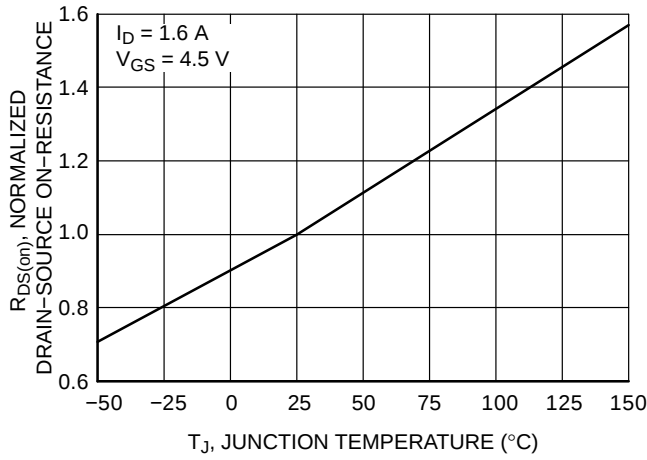


Figure 3. On-Resistance Variation with Temperature

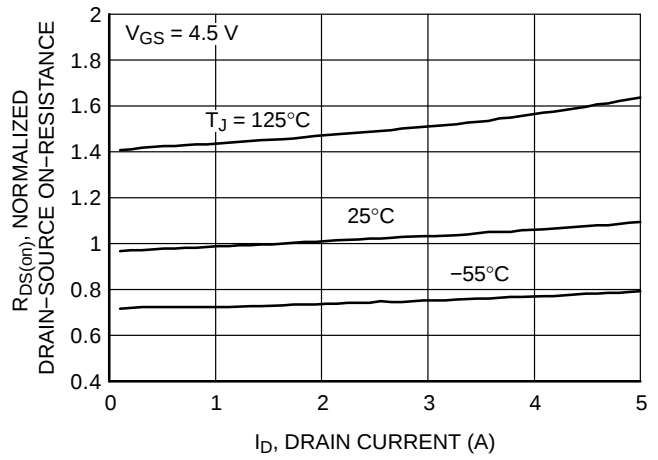


Figure 4. On-Resistance Variation with Drain Current and Temperature

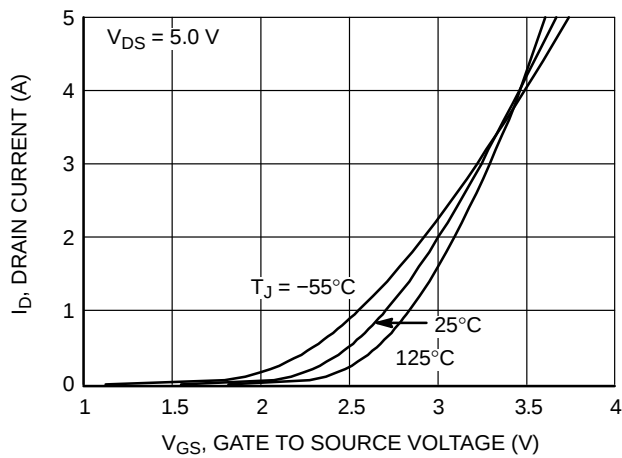


Figure 5. Transfer Characteristics

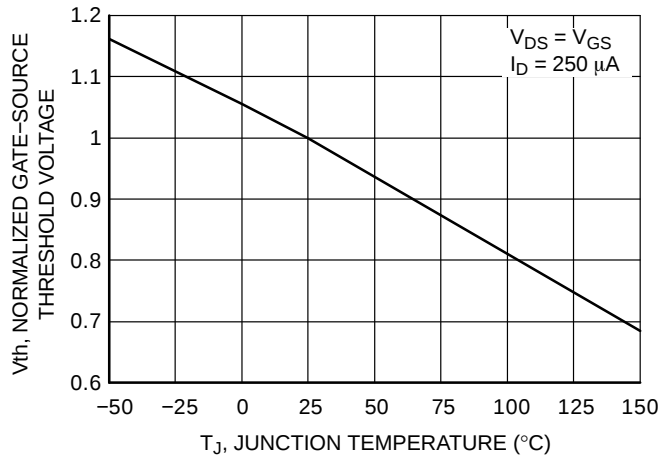


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (CONTINUED)

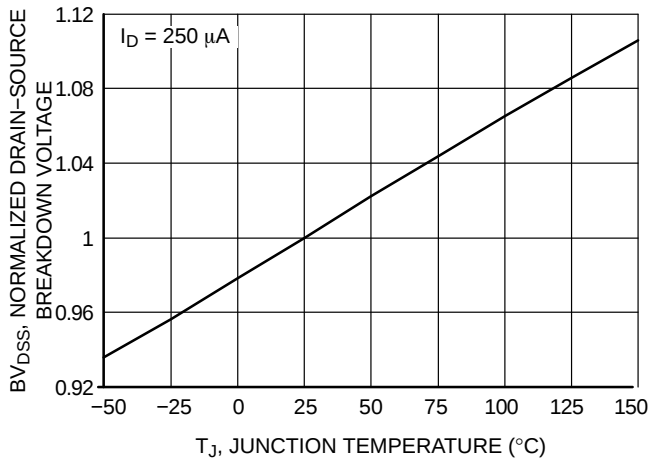


Figure 7. Breakdown Voltage Variation with Temperature

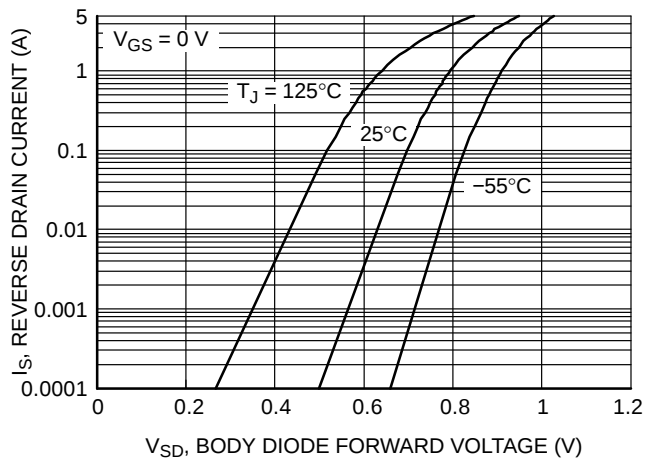


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

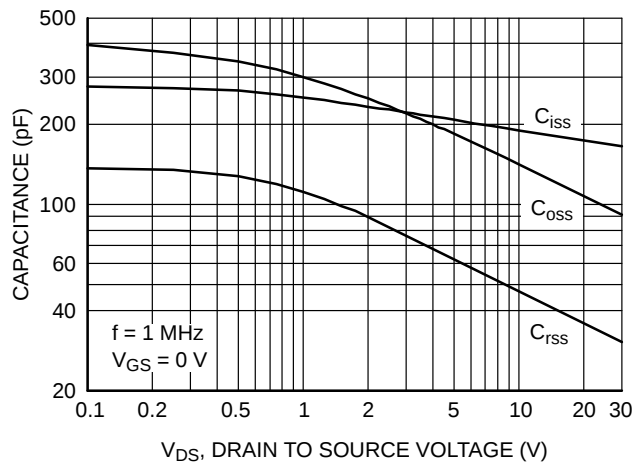


Figure 9. Capacitance Characteristics

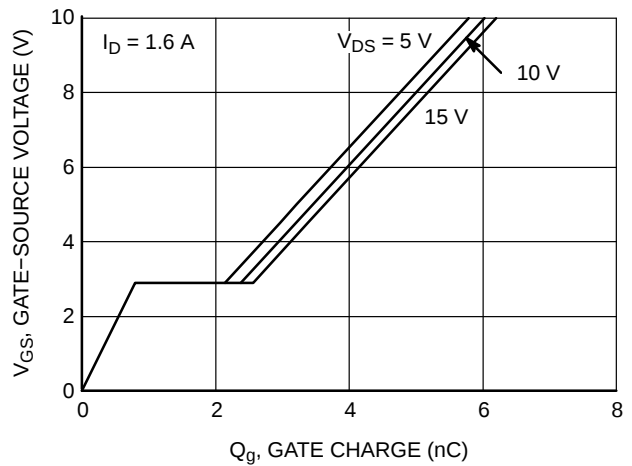


Figure 10. Gate Charge Characteristics

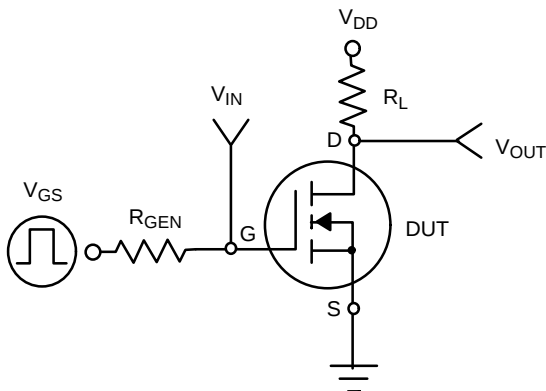


Figure 11. Switching Test Circuit

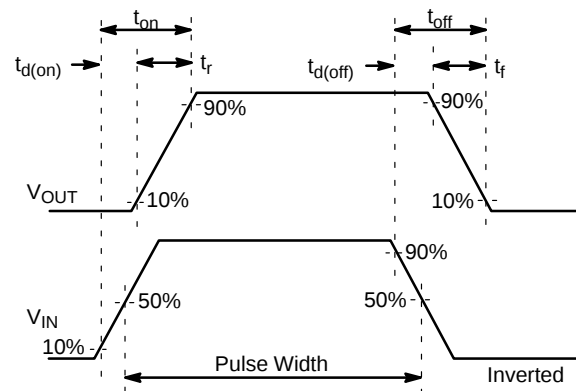


Figure 12. Switching Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS (CONTINUED)

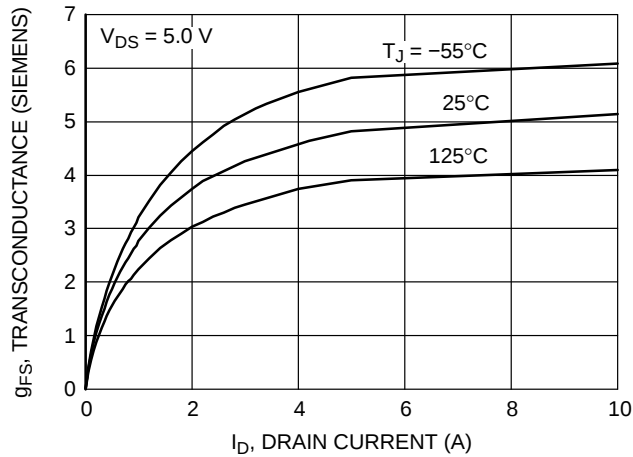


Figure 13. Transconductance Variation with Drain Current and Temperature

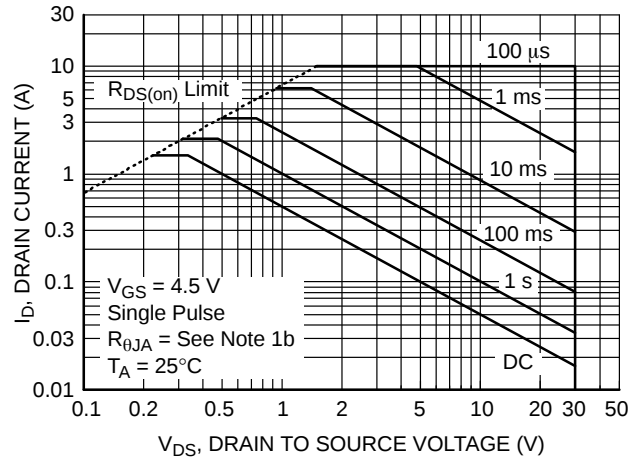


Figure 14. Maximum Safe Operating Area

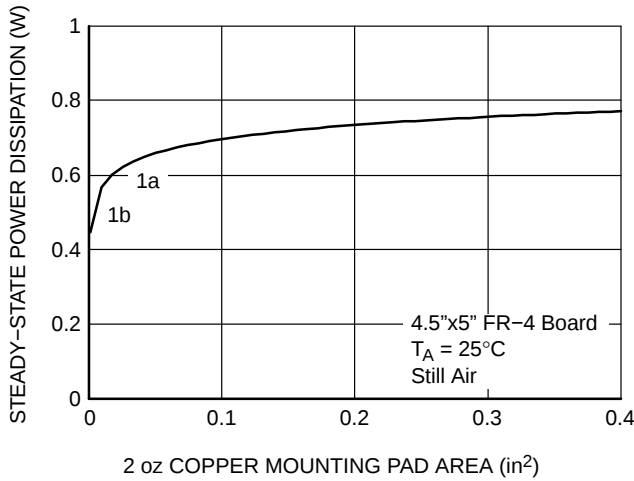


Figure 15. SUPERSOT-3 Maximum Steady-State Power Dissipation vs. Copper Mounting Pad Area

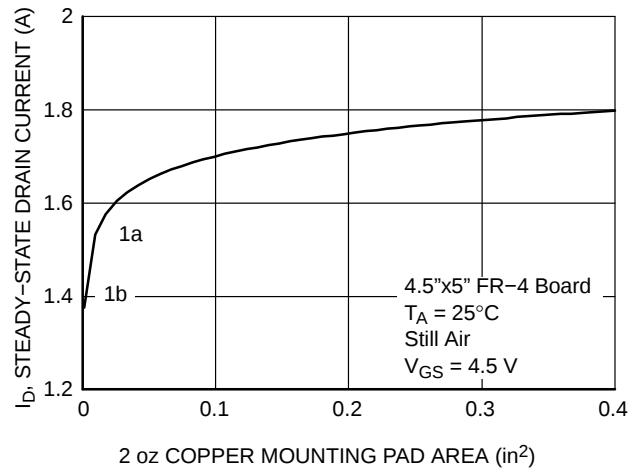


Figure 16. Maximum Steady-State Drain Current vs. Copper Mounting Pad Area

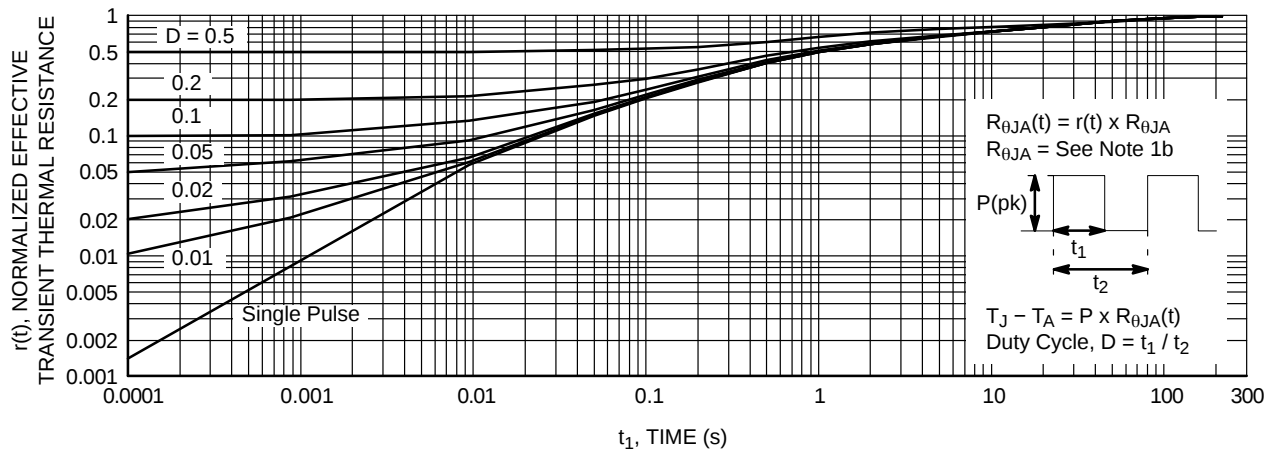


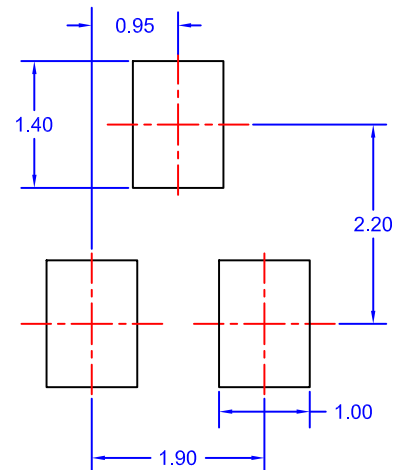
Figure 17. Transient Thermal Response Curve

NOTE: Characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

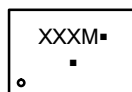
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SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019


LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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