

# 74HCT540D,74HCT541D

## 1. Functional Description

- Octal Bus Buffer

74HCT540D: INVERTING, 3-STATE OUTPUTS

74HCT541D: NON-INVERTING, 3-STATE OUTPUTS

## 2. General

The 74HCT540D/74HCT541D are high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HCT540D is an inverting type, and the 74HCT541D is a non-inverting type.

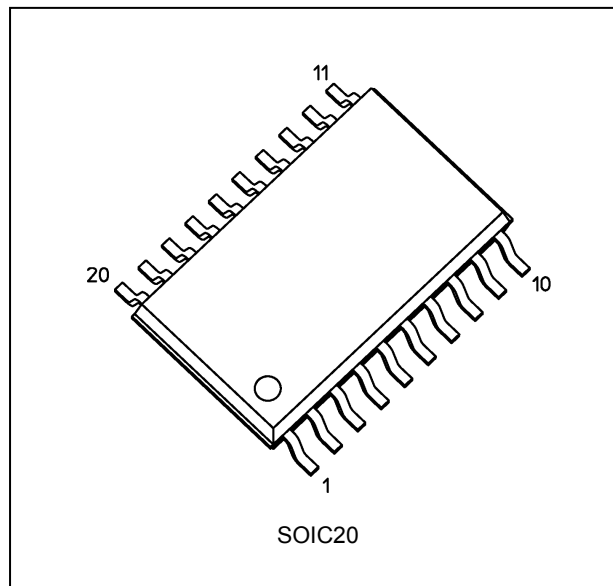
When either  $\overline{G1}$  or  $\overline{G2}$  are high, the terminal outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) High speed:  $t_{pd} = 9 \text{ ns (typ.)}$  at  $V_{CC} = 5.5 \text{ V}$
- (2) Low power dissipation:  $I_{CC} = 4.0 \mu\text{A (max)}$  at  $T_a = 25 \text{ }^\circ\text{C}$
- (3) Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V(max)}$   
 $V_{IH} = 2.0 \text{ V(min)}$
- (4) Wide interfacing ability: LSTTL, NMOS, CMOS
- (5) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$

## 4. Packaging

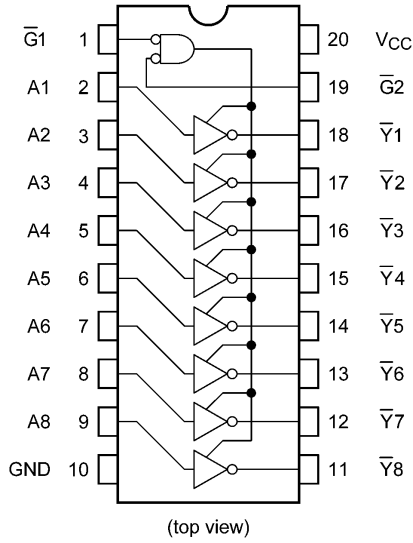


Start of commercial production

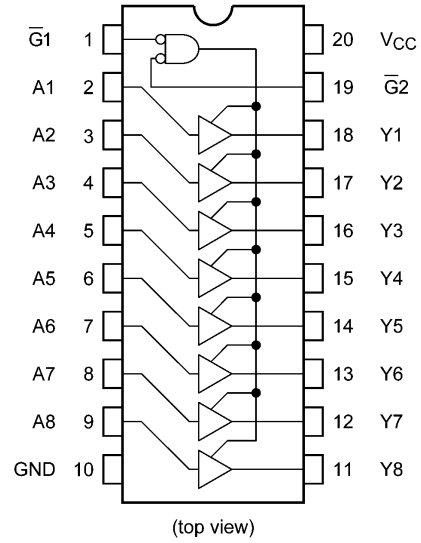
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**5. Pin Assignment**

74HCT540D

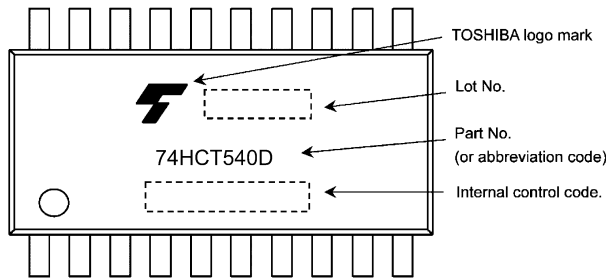


74HCT541D

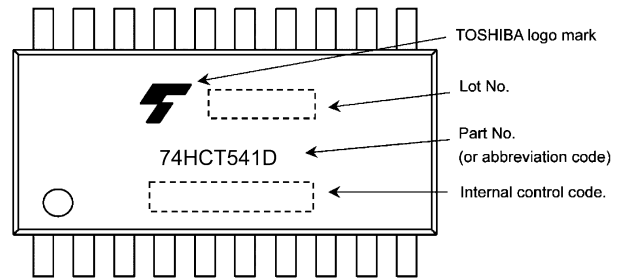


**6. Marking**

74HCT540D

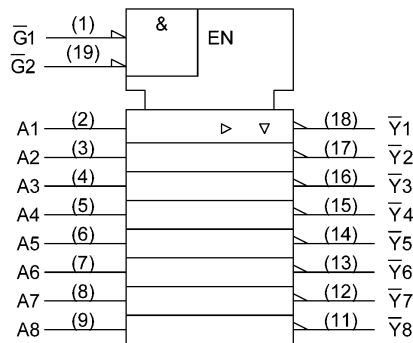


74HCT541D

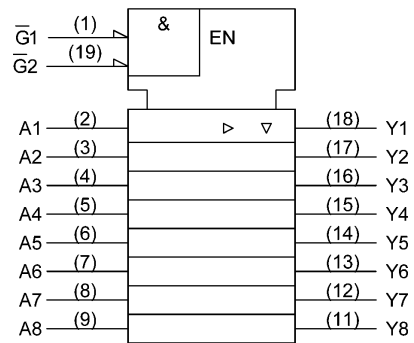


**7. IEC Logic Symbol**

74HCT540D



74HCT541D



**8. Truth Table**

Input $\bar{G}1$	Input $\bar{G}2$	Input $A_n$	Output $Y_n$	Output $\bar{Y}_n$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X: Don't care  
 Z: High impedance  
 $Y_n$ : 74HCT541D  
 $\bar{Y}_n$ : 74HCT540D

**9. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 35$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 75$	mA
Power dissipation	$P_D$		500	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**10. Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall times	$t_r, t_f$	0 to 500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
 Unused inputs must be tied to either  $V_{CC}$  or GND.

**11. Electrical Characteristics**

**11.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	4.5 to 5.5	2.0	—	—	V	
Low-level input voltage	$V_{IL}$	—	4.5 to 5.5	—	—	0.8	V	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	4.5	4.4	4.5	—	V
			$I_{OH} = -6\ \text{mA}$	4.5	4.18	4.31	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	4.5	—	0.0	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5	—	0.17	0.26	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 0.5$	$\mu\text{A}$	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	
	$I_{CCT}$	Per input: $V_{IN} = 0.5\ \text{V}$ or $2.4\ \text{V}$ Other input: $V_{CC}$ or GND	5.5	—	—	2.0	mA	

**11.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	4.5 to 5.5	2.0	—	V	
Low-level input voltage	$V_{IL}$	—	4.5 to 5.5	—	0.8	V	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	4.5	4.4	—	V
			$I_{OH} = -6\ \text{mA}$	4.5	4.13	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	4.5	—	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5	—	0.33	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 5.0$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	40.0	$\mu\text{A}$
	$I_{CCT}$	Per input: $V_{IN} = 0.5\ \text{V}$ or $2.4\ \text{V}$ Other input: $V_{CC}$ or GND	5.5	—	—	2.9	mA

**11.3. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )**

Characteristics	Part Number	Symbol	Note	Test Condition	$C_L$ (pF)	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Output transition time		$t_{TLH}, t_{THL}$		—	50	4.5	—	7	12	ns
						5.5	—	6	11	
Propagation delay time	74HCT540D	$t_{PLH}, t_{PHL}$		—	50	4.5	—	12	20	ns
						5.5	—	9	18	
					150	4.5	—	17	26	
						5.5	—	14	24	
Propagation delay time	74HCT541D	$t_{PLH}, t_{PHL}$		—	50	4.5	—	14	23	ns
						5.5	—	11	21	
					150	4.5	—	19	29	
						5.5	—	16	27	
3-state output enable time		$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	50	4.5	—	18	30	ns
						5.5	—	16	27	
					150	4.5	—	23	36	
						5.5	—	21	33	
3-state output disable time		$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	50	4.5	—	18	30	ns
						5.5	—	16	27	
Input capacitance		$C_{IN}$		—			—	5	10	pF
Output capacitance		$C_{OUT}$		—			—	10	—	pF
Power dissipation capacitance	74HCT540D	$C_{PD}$	(Note 1)	—			—	35	—	pF
	74HCT541D	$C_{PD}$		—			—	31	—	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

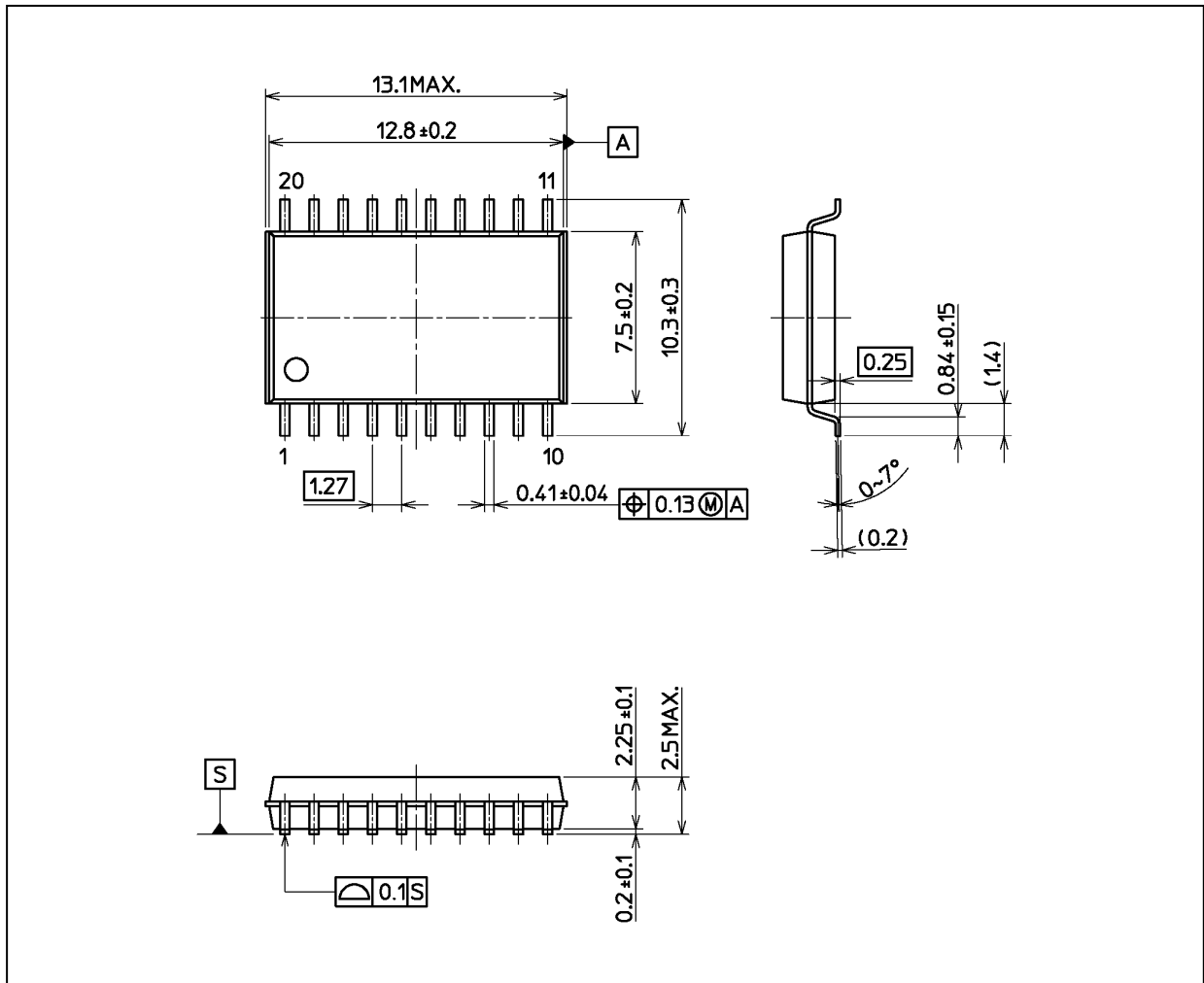
$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per bit)}$$

**11.4. AC Characteristics (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )**

Characteristics	Part Number	Symbol	Test Condition	$C_L$ (pF)	$V_{CC}$ (V)	Min	Max	Unit
Output transition time		$t_{TLH}, t_{THL}$	—	50	4.5	—	15	ns
					5.5	—	14	
Propagation delay time	74HCT540D	$t_{PLH}, t_{PHL}$	—	50	4.5	—	25	ns
					5.5	—	23	
				150	4.5	—	33	
					5.5	—	30	
Propagation delay time	74HCT541D	$t_{PLH}, t_{PHL}$	—	50	4.5	—	29	ns
					5.5	—	27	
				150	4.5	—	36	
					5.5	—	33	
3-state output enable time		$t_{PZL}, t_{PZH}$	$R_L = 1\text{ k}\Omega$	50	4.5	—	38	ns
					5.5	—	35	
				150	4.5	—	45	
					5.5	—	41	
3-state output disable time		$t_{PLZ}, t_{PHZ}$	$R_L = 1\text{ k}\Omega$	50	4.5	—	38	ns
					5.5	—	35	
Input capacitance		$C_{IN}$	—			—	10	pF

**Package Dimensions**

Unit: mm



Weight: 0.51 g (typ.)

Package Name(s)
Nickname: SOIC20

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