

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSV)

2SK3466

Chopper Regulator

- Low drain-source ON resistance: $R_{DS(ON)} = 1.35 \Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 4.0 S$ (typ.)
- Low leakage current: $I_{DSS} = 100 \mu A$ (max) ($V_{DS} = 500 V$)
- Enhancement-model: $V_{th} = 2.0$ to $4.0 V$ ($V_{DS} = 10 V$, $I_D = 1 mA$)

Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	500	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	500	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	5	A
	Pulse (Note 1)	I_{DP}	20	
Drain power dissipation ($T_c = 25^\circ C$)		P_D	50	W
Single pulse avalanche energy (Note 2)		E_{AS}	180	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 3)		E_{AR}	5	mJ
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	2.5	$^\circ C/W$

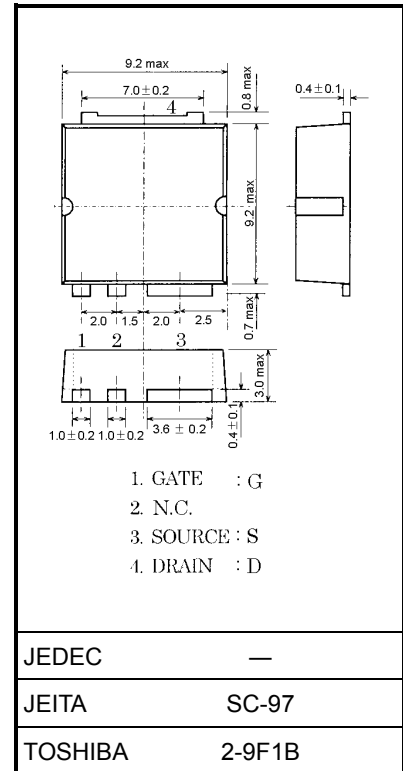
Note 1: Please use devices on condition that the channel temperature is below $150^\circ C$.

Note 2: $V_{DD} = 90 V$, $T_{ch} = 25^\circ C$ (initial), $L = 12.2 mH$, $R_G = 25 \Omega$, $I_{AR} = 5 A$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

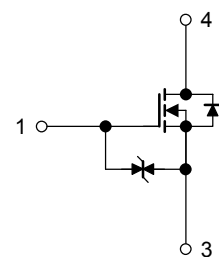
This transistor is an electrostatic sensitive device. Please handle with caution.

Unit: mm

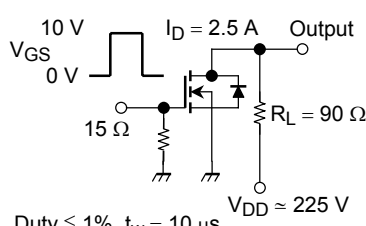


Weight: 0.74 g (typ.)

Circuit Configuration



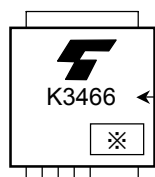
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-OFF current		I_{DSS}	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	500	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	1.35	1.50	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 5 \text{ A}$	2.5	4.0	—	S
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	780	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	
Output capacitance		C_{oss}		—	200	—	
Switching time	Rise time	t_r		—	12	—	ns
	Turn-ON time	t_{on}		—	25	—	
	Fall time	t_f		—	15	—	
	Turn-OFF time	t_{off}		—	60	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	17	—	nC
Gate-source charge		Q_{gs}		—	11	—	
Gate-drain ("miller") charge		Q_{gd}		—	6	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DSF}	—	—	—	5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5 \text{ A}, V_{GS} = 0 \text{ V},$	—	1400	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 100 \text{ A}/\mu\text{s}$	—	9	—	μC

Marking



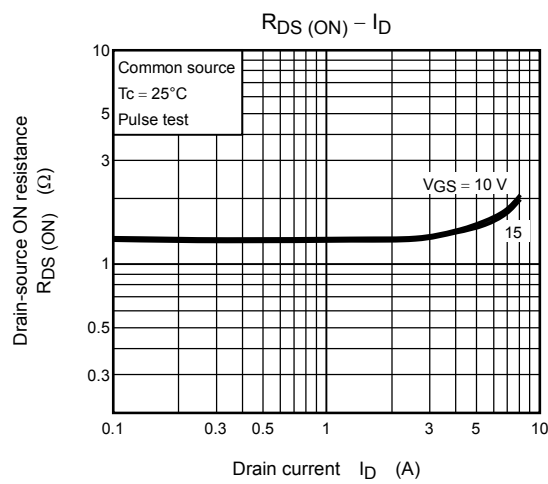
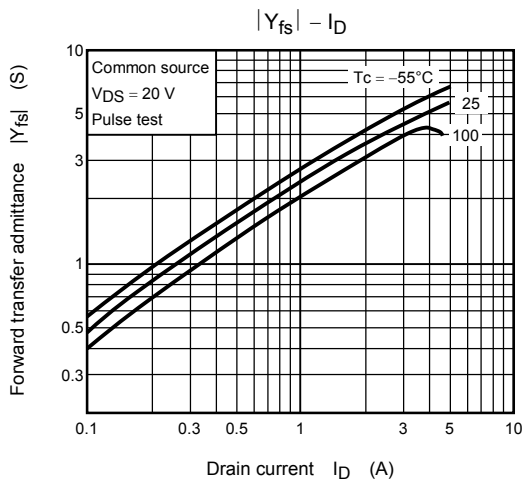
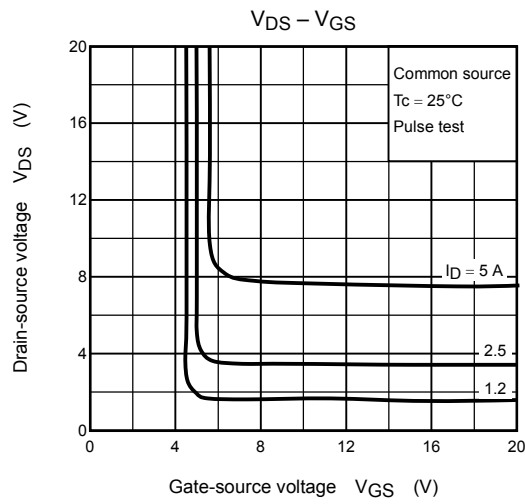
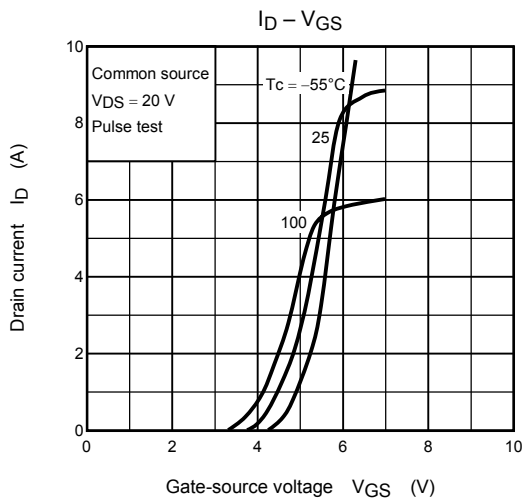
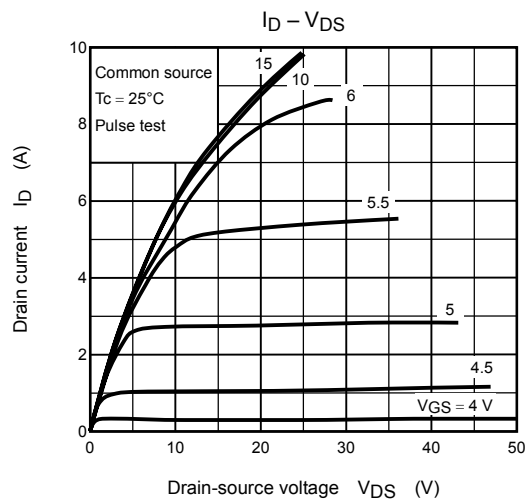
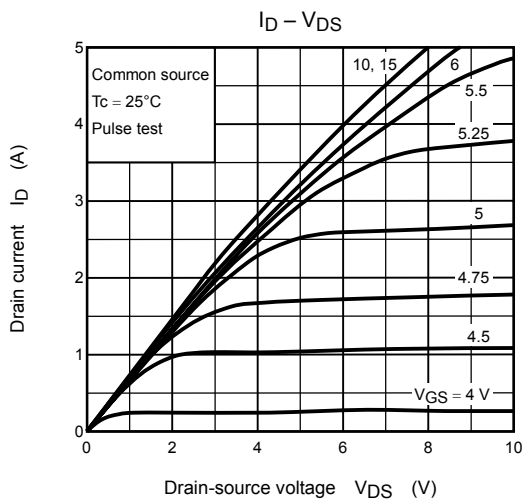
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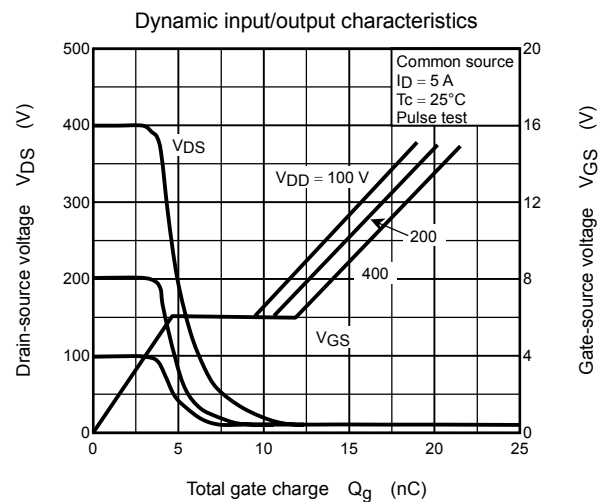
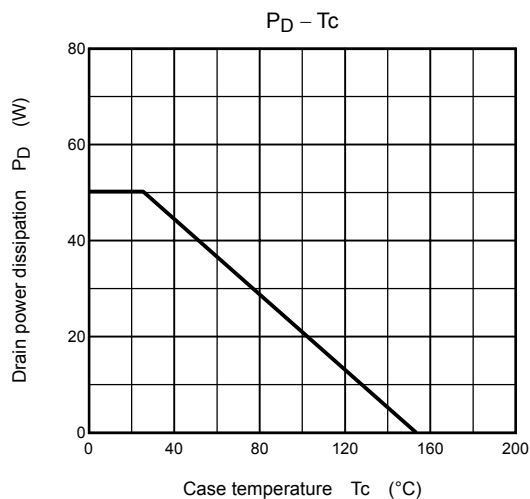
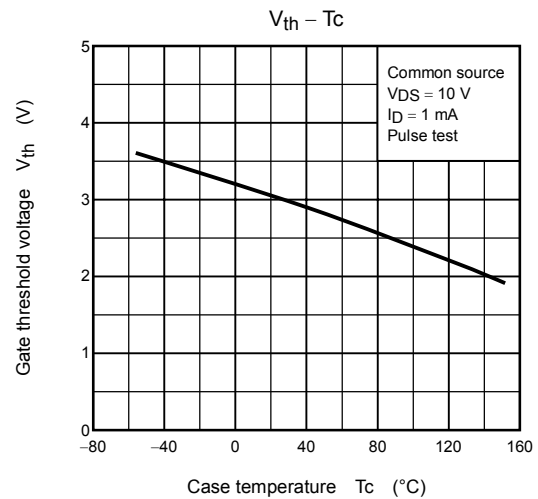
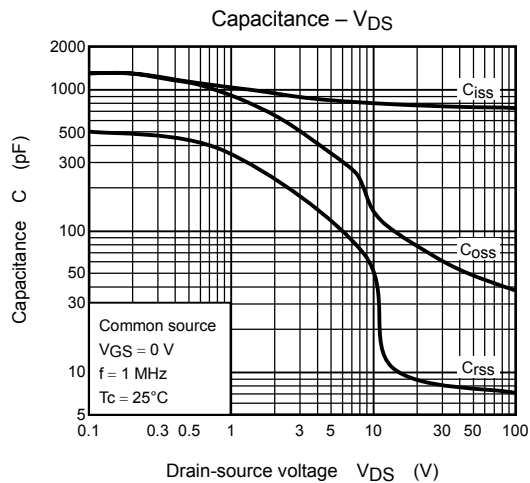
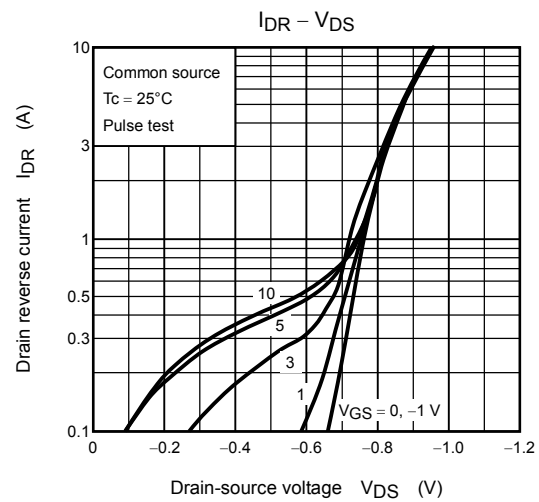
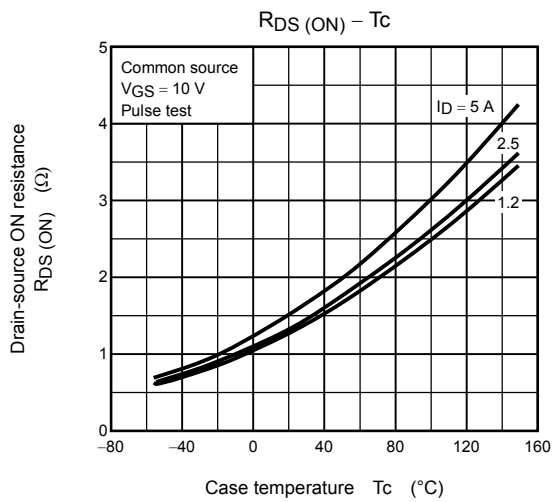
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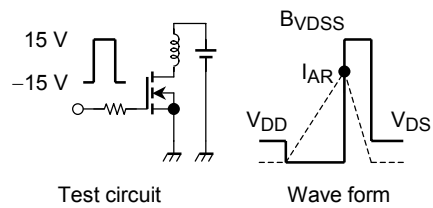
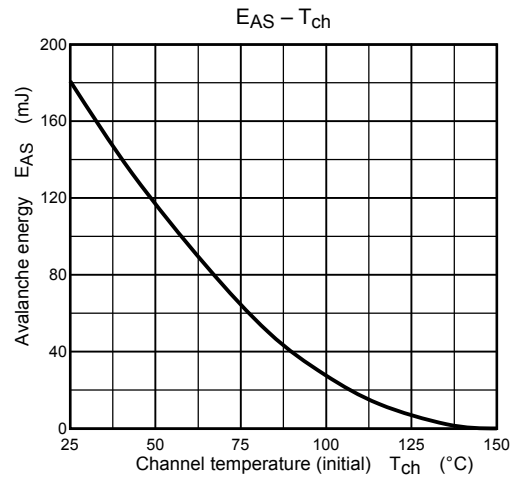
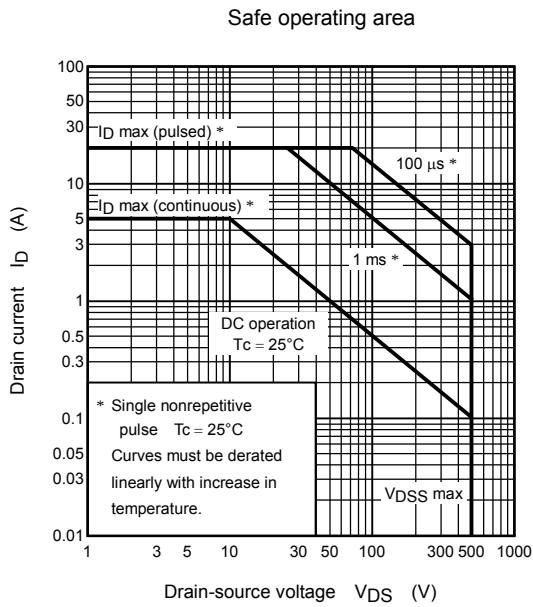
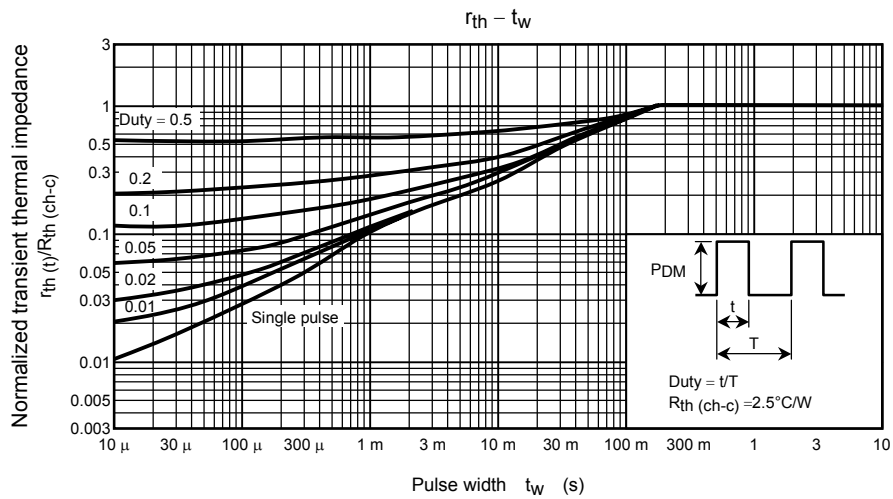


Month (starting from alphabet A)

Year (last number of the christian era)







$$R_G = 25 \, \Omega$$

$$V_{DD} = 90 \, \text{V}, L = 12.2 \, \text{mH}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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