OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ISL55190

May 28, 2010 FN7381.5

300MHz Low Noise Amplifiers

The EL5130 and EL5131 are ultra-low voltage noise, high speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communications and imaging. These devices offer extremely low power consumption for exceptional noise performance. Stable at gains as low as 5, these devices offer 100mA of drive performance. Not only do these devices find perfect application in high gain applications, they maintain their performance down to lower gain settings.

These amplifiers are available in small package options (SOT-23) as well as the industry-standard SOIC packages. All parts are specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5130IS	5130IS	-	8 Ld SOIC (150 mil)	MDP0027
EL5130ISZ (Note)	5130ISZ	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5130IS-T7	5130IS	7”	8 Ld SOIC (150 mil)	MDP0027
EL5130ISZ-T7 (Note)	5130ISZ	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5130IS-T13	5130IS	13”	8 Ld SOIC (150 mil)	MDP0027
EL5130ISZ-T13 (Note)	5130ISZ	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5131IW-T7	BBAA	7” (3k pcs)	5 Ld SOT-23	P5.064A
EL5131IWZ-T7 (Note)	BRAA	7” (3k pcs)	5 Ld SOT-23 (Pb-free)	P5.064A
EL5131IW-T7A	BBAA	7” (250 pcs)	5 Ld SOT-23	P5.064A
EL5131IWZ-T7A (Note)	BRAA	7” (250 pcs)	5 Ld SOT-23 (Pb-free)	P5.064A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

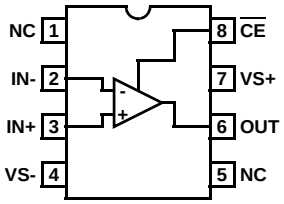
- 300MHz -3dB bandwidth
- Ultra low noise = 1.8nV/√Hz
- 350V/µs slew rate
- Low supply current = 4mA
- Single supplies from 5V to 12V
- Dual supplies from ±2.5V to ±6V
- Fast disable on the EL5130
- Low cost
- Pb-free plus anneal available (RoHS compliant)

Applications

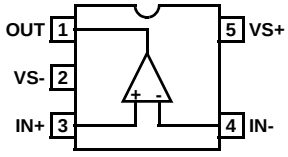
- Imaging
- Instrumentation
- Communications devices

Pinouts

EL5130
(8 LD SOIC)
TOP VIEW



EL5131
(5 LD SOT-23)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Slewrate between V_S+ and V_S- 1V/µs
Supply Voltage from V_S+ to V_S- 13.2V
I_{IN}-, I_{IN}+, $\overline{CE}$ . . . . . ±5mA
Continuous Output Current 100mA

Thermal Information

Storage Temperature . . . . . -65°C to +125°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . +125°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 500Ω, R_G = 50Ω, C_L = 5pF, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage		-0.9	0.2	0.9	mV
T_CV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		0.8		µV/°C
IB	Input Bias Current	V_{IN} = 0V	1.5	2.27	3.3	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-500	100	500	nA
T_CI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		-3		nA/°C
PSRR	Power Supply Rejection Ratio	V_S = ±4.75V to ±5.25V	75	90		dB
CMRR	Common Mode Rejection Ratio	V_{IN} = ±3.0V	95	110		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	±3	±3.3		V
R_{IN}	Input Resistance	Common mode	5	20		MΩ
C_{IN}	Input Capacitance			1		pF
I_S	Supply Current		3.0	3.54	4.1	mA
AVOL	Open Loop Gain	V_{OUT} = ±2.5V, R_L = 1kΩ to GND	10	16		kV/V
V_O	Output Voltage Swing	R_L = 1kΩ, R_F = 900Ω, R_G = 100Ω	±3.5	±3.8		V
		R_L = 150Ω	±3.5	±3.3		V
I_{SC}	Short Circuit Current	R_L = 10Ω	50	100		mA
BW	-3dB Bandwidth	A_V = +5, R_L = 500Ω		300		MHz
BW	±0.1dB Bandwidth	A_V = +5, R_L = 500Ω		60		MHz
GBWP	Gain Bandwidth Product			1500		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 6pF		55		°
SR	Slew Rate	V_S = ±5V, R_L = 150Ω, V_{OUT} = ±2.5V	225	350		V/µs
t_R, t_F	Rise Time, Fall Time	±0.1V_{STEP}		TBD		ns
t_{PD}	Propagation Delay	±0.1V_{STEP}		TBD		ns
t_S	0.01% Settling Time			14		ns
dG	Differential Gain	A_V = +2, R_F = 1kΩ		0.01		%
dP	Differential Phase	A_V = +2, R_F = 1kΩ		0.01		°
e_N	Input Noise Voltage	f = 10kHz		1.8		nV/√Hz
i_N	Input Noise Current	f = 10kHz		1.1		pA/√Hz

Typical Performance Curves

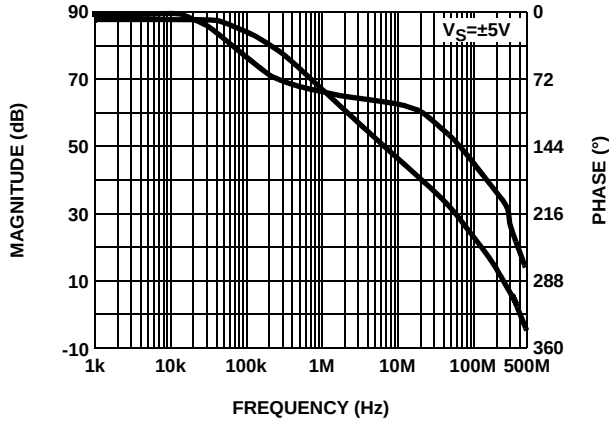


FIGURE 1. OPEN LOOP GAIN AND PHASE vs FREQUENCY

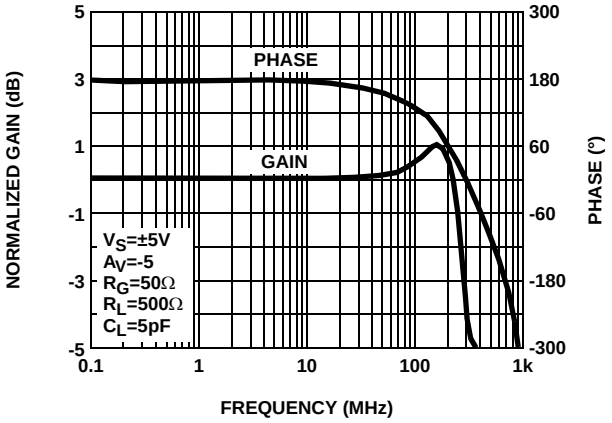


FIGURE 2. GAIN AND PHASE vs FREQUENCY (INVERTING)

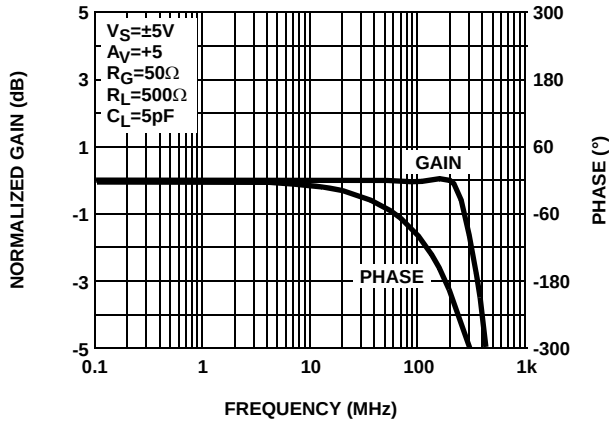


FIGURE 3. GAIN AND PHASE vs FREQUENCY (NON-INVERTING)

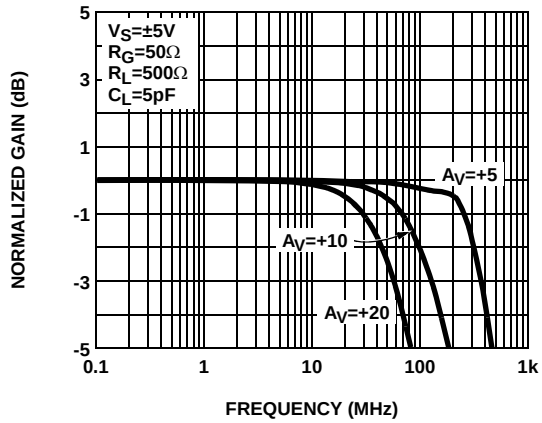


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS A_V+

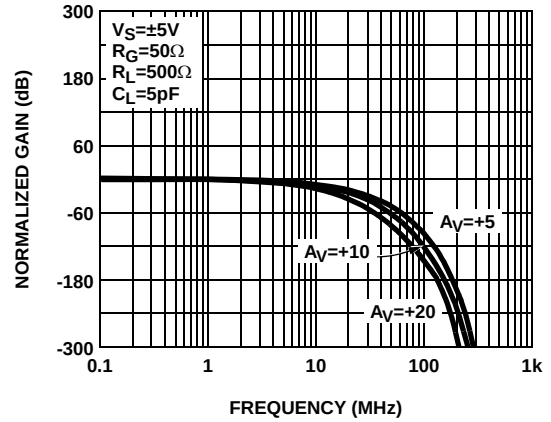


FIGURE 5. PHASE vs FREQUENCY FOR VARIOUS A_V+

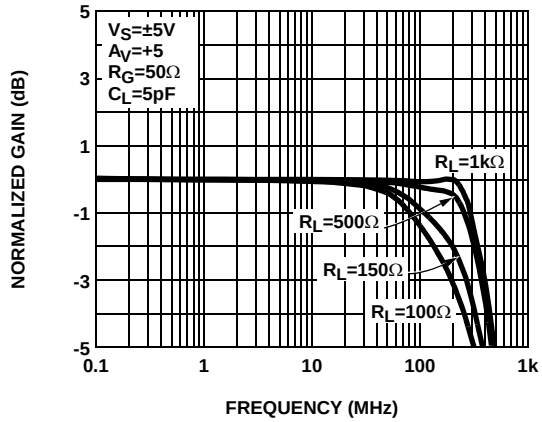


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS R_L (A_V=+5)

Typical Performance Curves

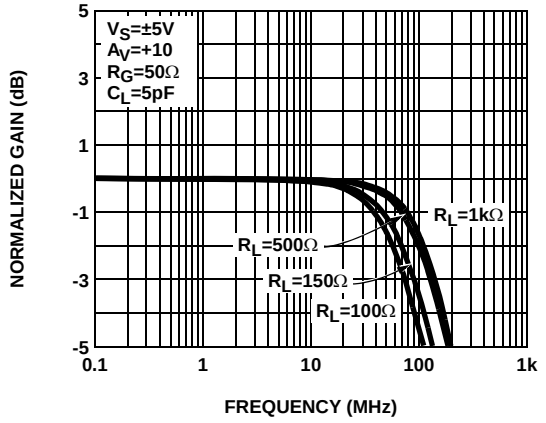


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS R_L (A_V=+10)

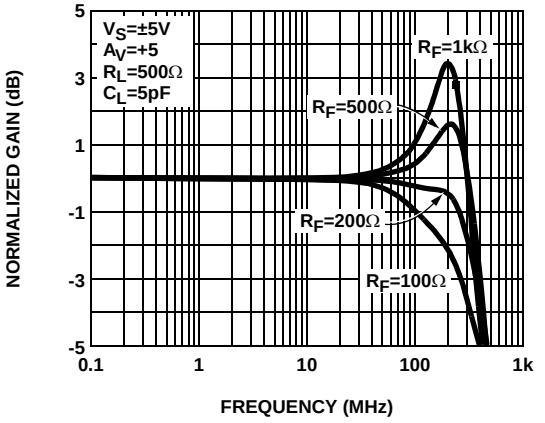


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V=+5)

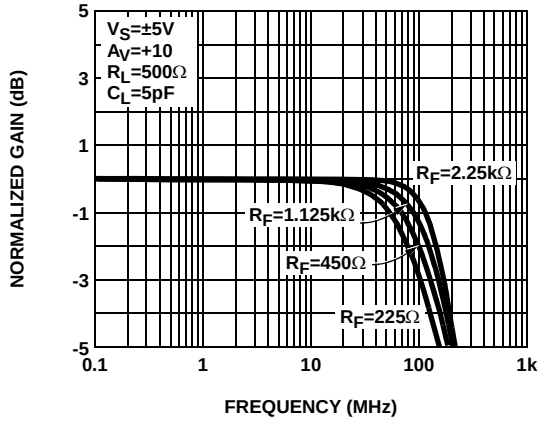


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V=+10)

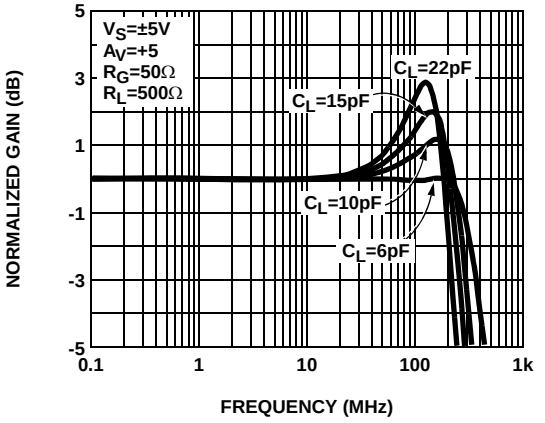


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS C_L (A_V=+5)

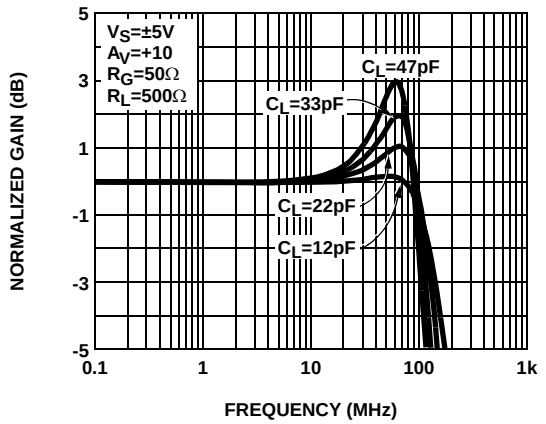


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_L (A_V=+10)

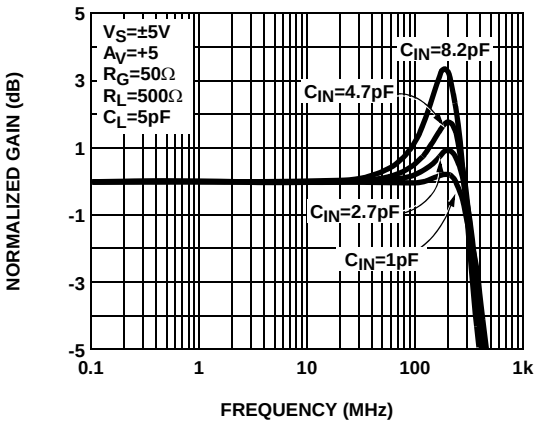


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{IN}- (A_V=+5)

Typical Performance Curves

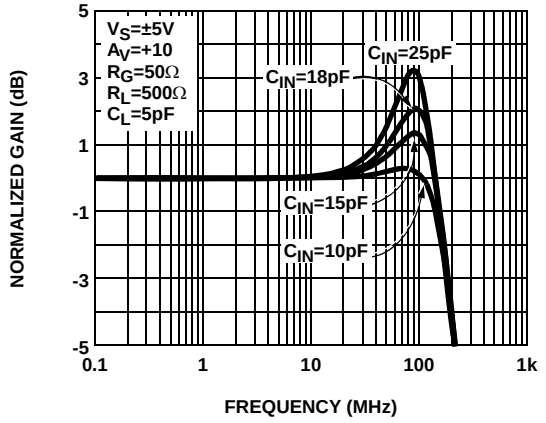


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS C_{IN}- (A_V=+10)

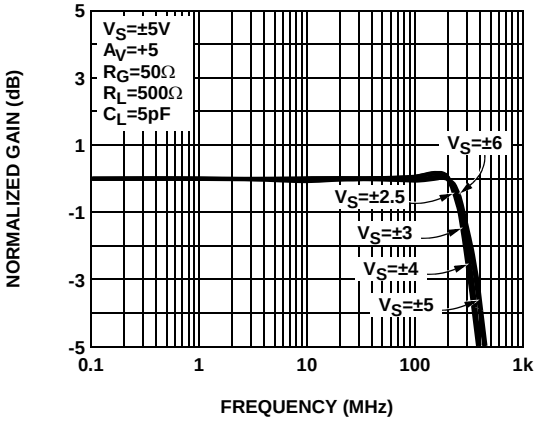


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS ±V_S (A_V=+5)

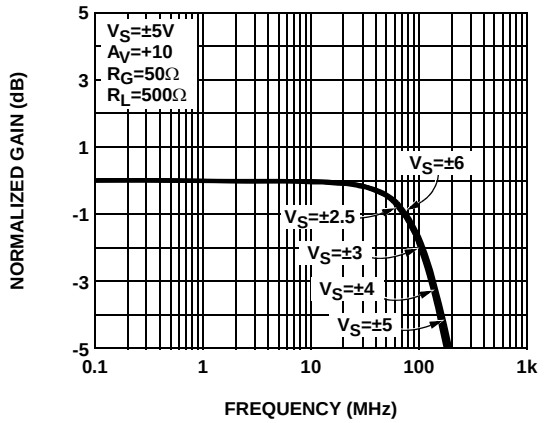


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS V_S± (A_V=+10)

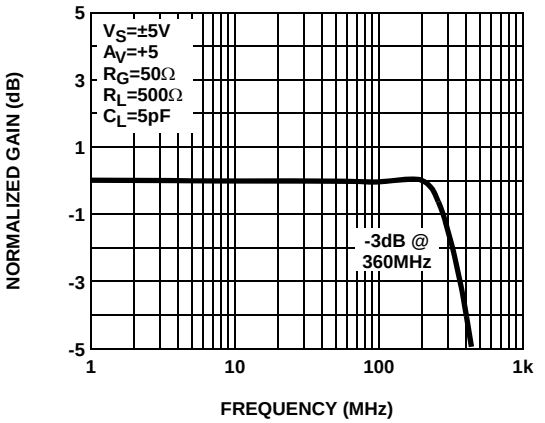


FIGURE 16. FREQUENCY RESPONSE (-3dB ROLL-OFF)

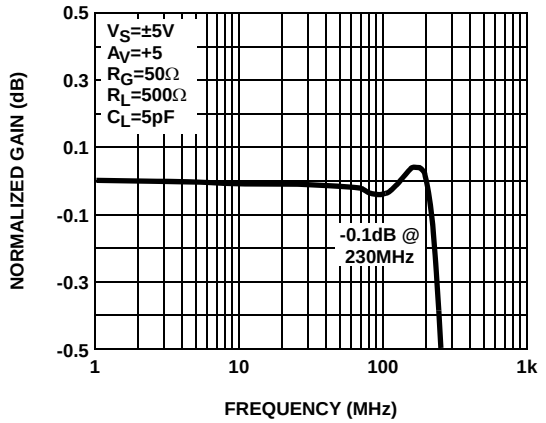


FIGURE 17. FREQUENCY RESPONSE (0.1dB GAIN FLATNESS)

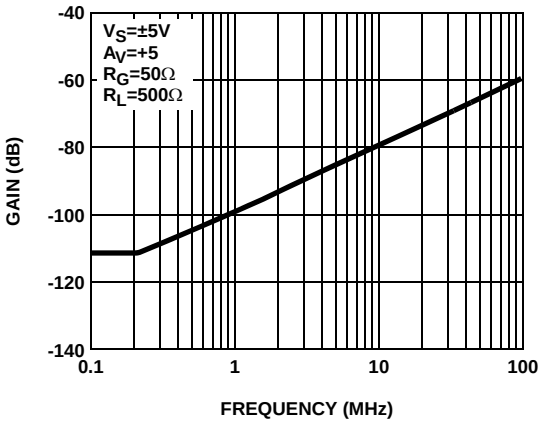


FIGURE 18. INPUT AND OUTPUT ISOLATION FOR DISABLE AMPLIFIER

Typical Performance Curves

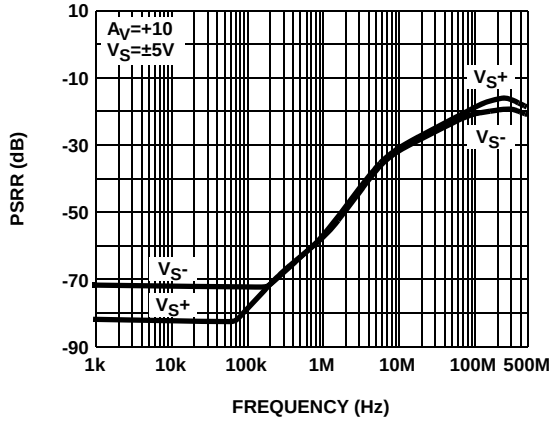


FIGURE 19. PSRR vs FREQUENCY

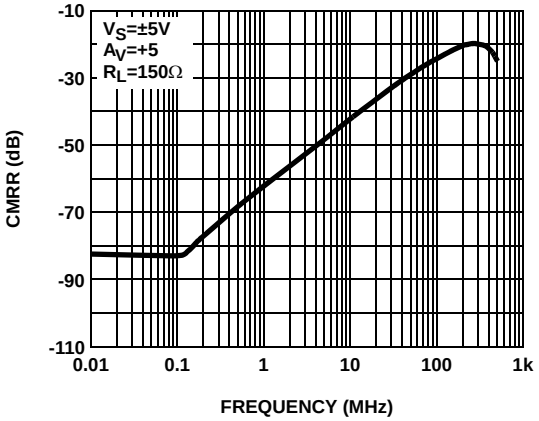


FIGURE 20. CMRR vs FREQUENCY

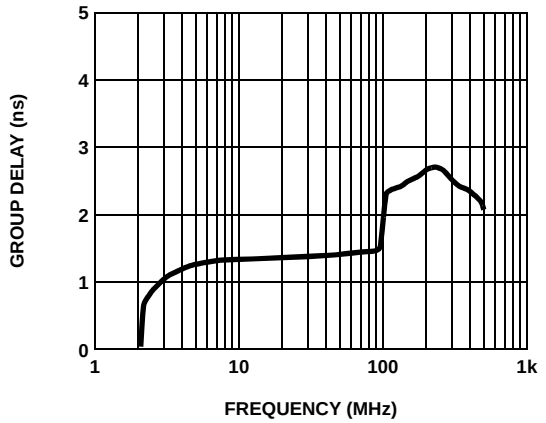


FIGURE 21. GROUP DELAY vs FREQUENCY

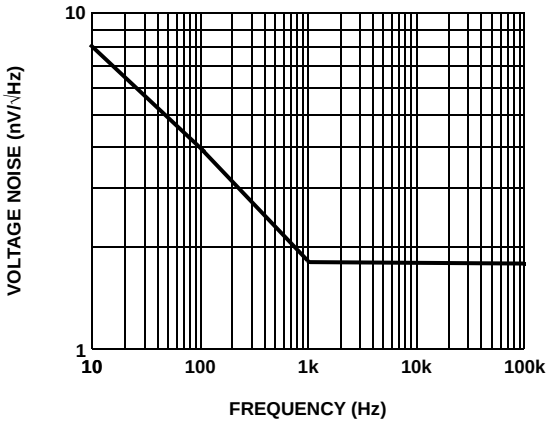


FIGURE 22. INPUT VOLTAGE NOISE

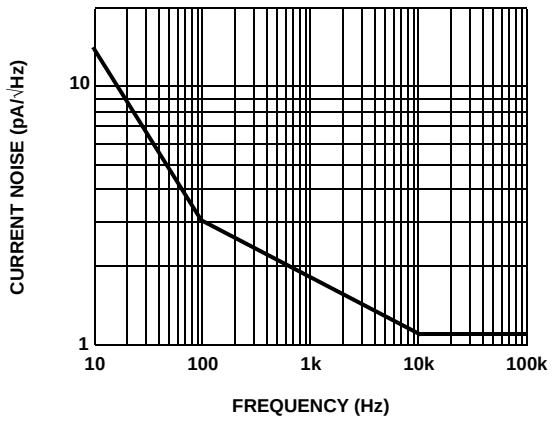


FIGURE 23. INPUT CURRENT NOISE

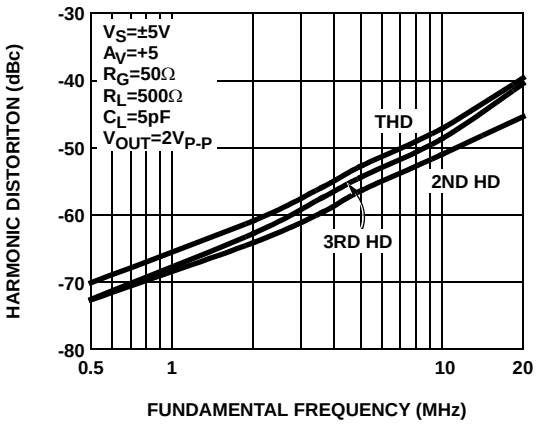


FIGURE 24. HARMONIC DISTORITON vs FREQUENCY (A_V=+5)

Typical Performance Curves

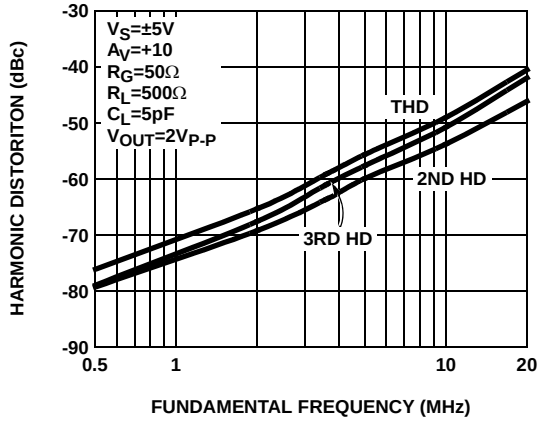


FIGURE 25. HARMONIC DISTORTION vs FREQUENCY (A_V=+10)

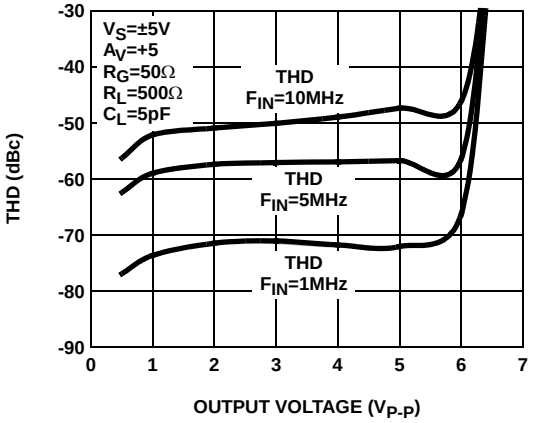


FIGURE 26. THD vs OUTPUT VOLTAGE (WORST HARMONIC)

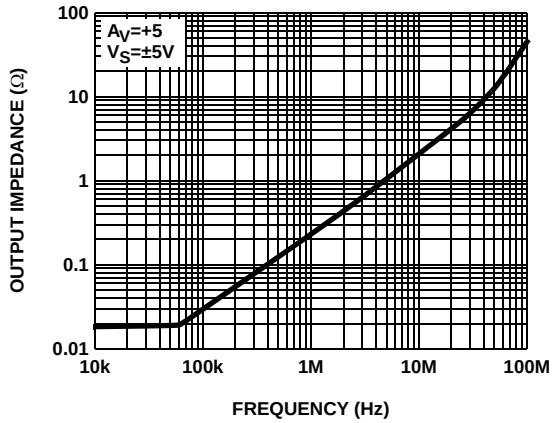


FIGURE 27. OUTPUT IMPEDANCE vs FREQUENCY

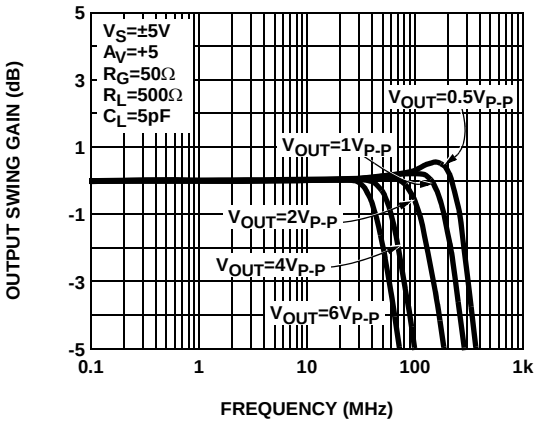


FIGURE 28. OUTPUT SWING vs FREQUENCY

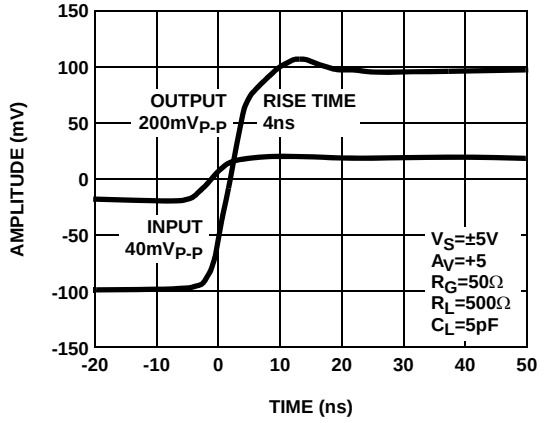


FIGURE 29. SMALL SIGNAL PULSE RESPONSE/RISE TIME

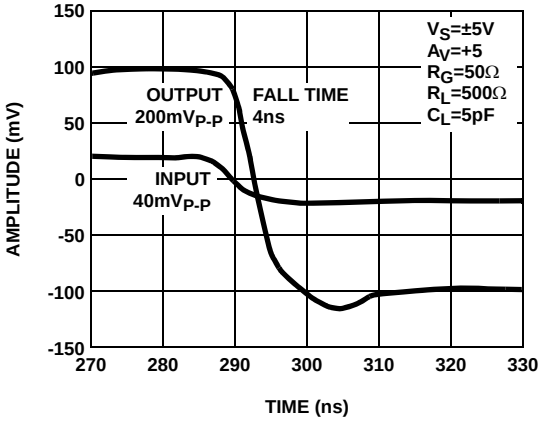


FIGURE 30. SMALL SIGNAL PULSE REPONSE/FALL TIME

Typical Performance Curves

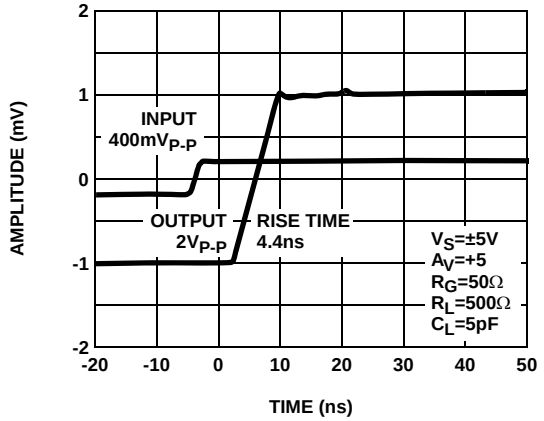


FIGURE 31. LARGE SIGNAL PULSE RESPONSE/RISE TIME

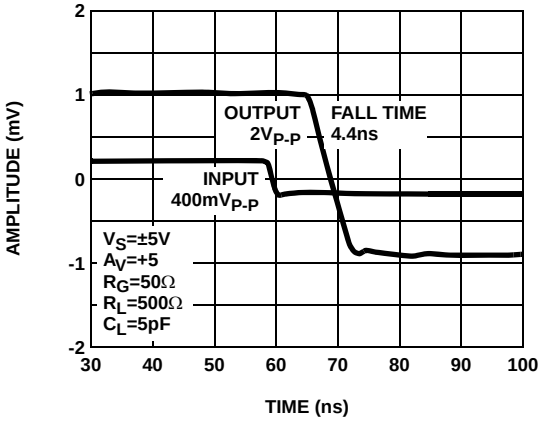


FIGURE 32. LARGE SIGNAL PULSE RESPONSE/RISE TIME

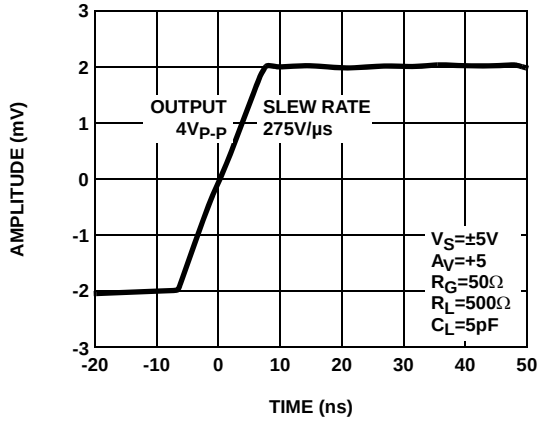


FIGURE 33. SLEW RATE (POSITIVE)

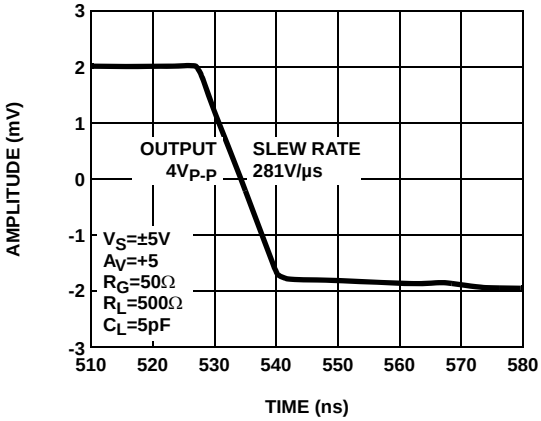


FIGURE 34. SLEW RATE (NEGATIVE)

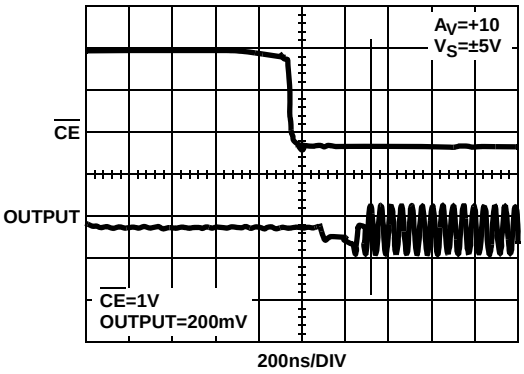


FIGURE 35. ENABLE RESPONSE/TURN-ON TIME

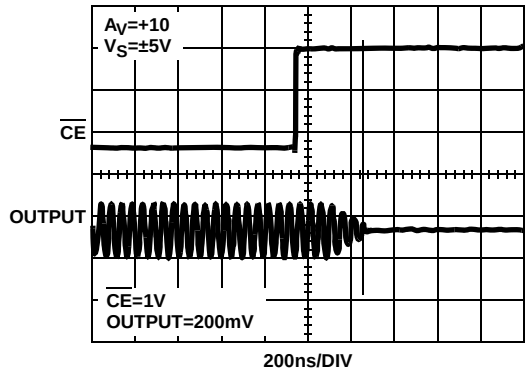


FIGURE 36. DISABLE RESPONSE/TURN-OFF TIME

Typical Performance Curves

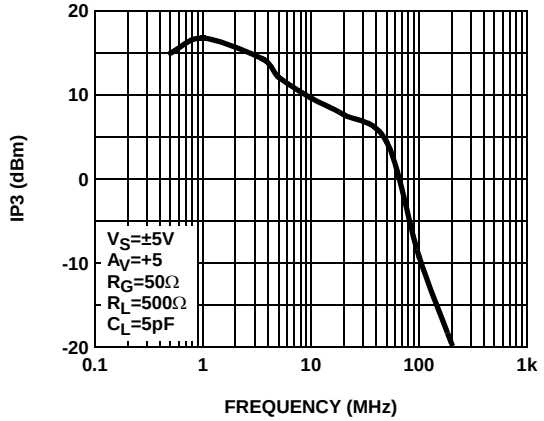


FIGURE 37. THIRD-ORDER INTERCEPT POINT

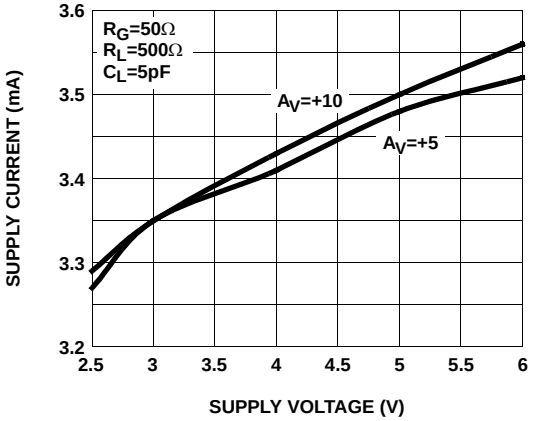


FIGURE 38. SUPPLY CURRENT vs SUPPLY VOLTAGE

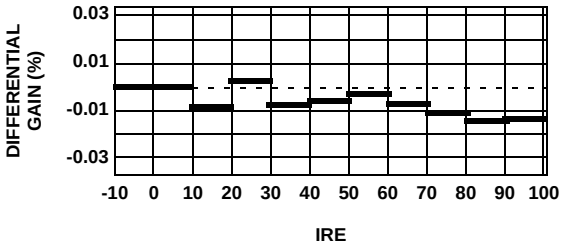


FIGURE 39. DIFFERENTIAL GAIN ERRORS

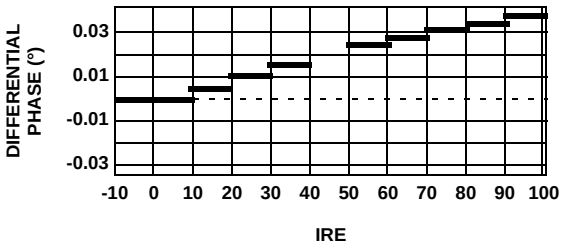


FIGURE 40. DIFFERENTIAL PHASE ERRORS

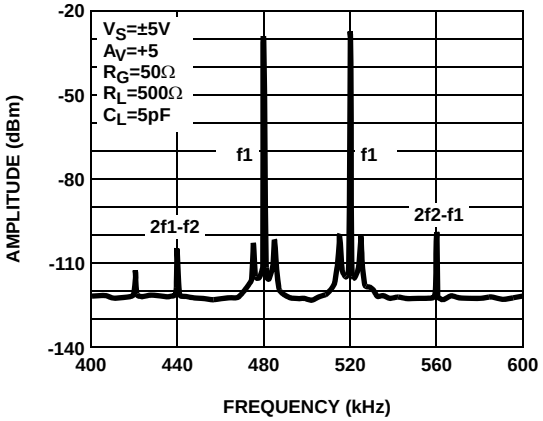


FIGURE 41. IP3

Typical Performance Curves

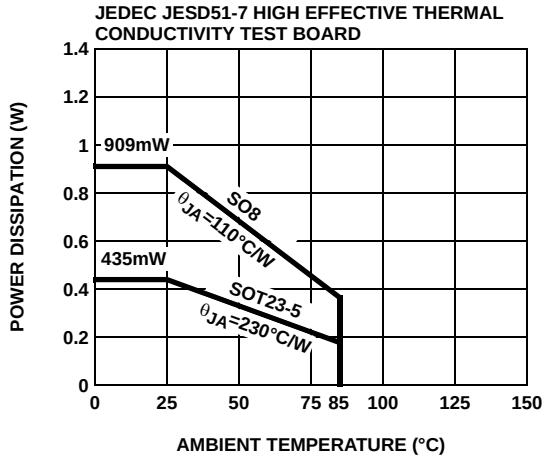


FIGURE 42. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

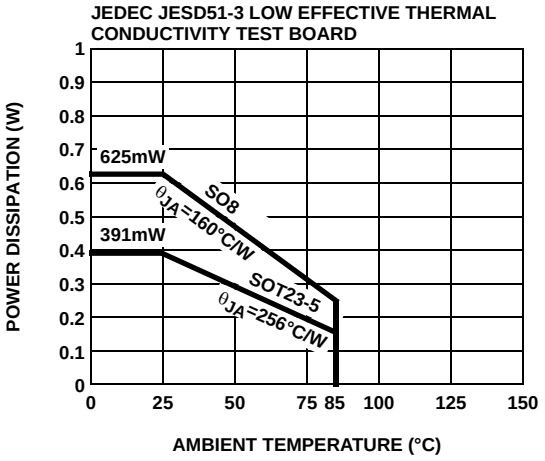
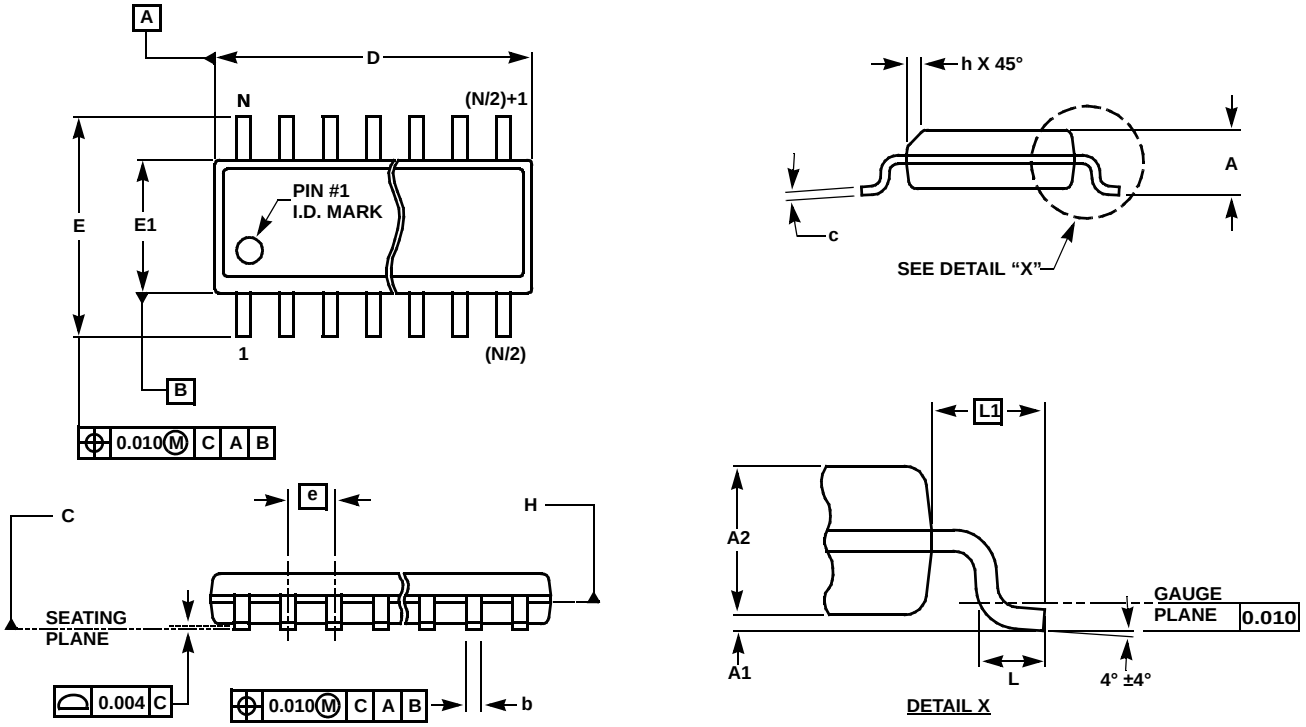


FIGURE 43. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Package Outline Drawing

P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
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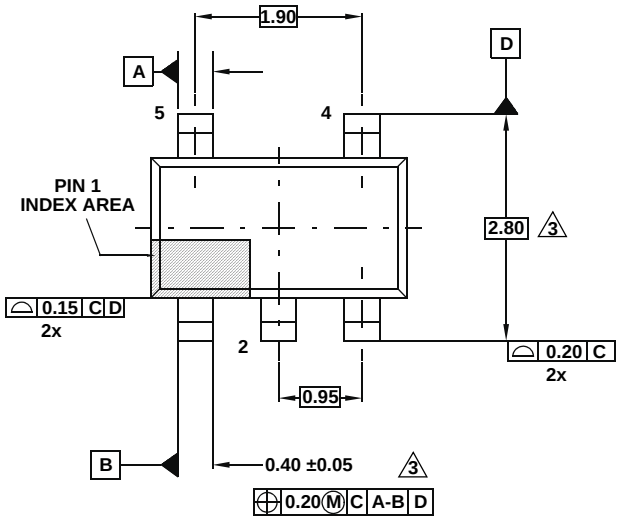
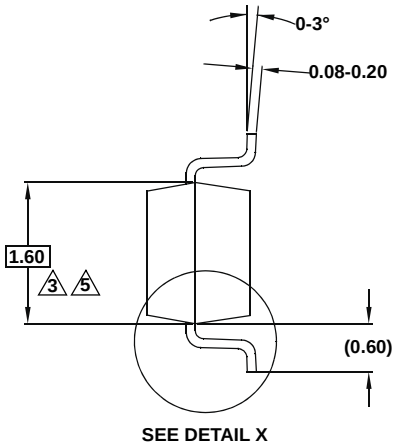
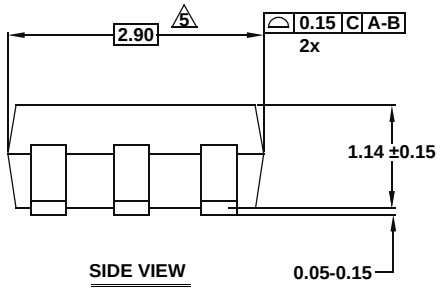


TOP VIEW

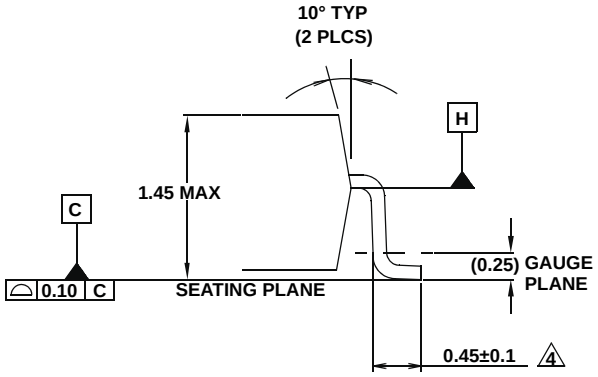


SEE DETAIL X

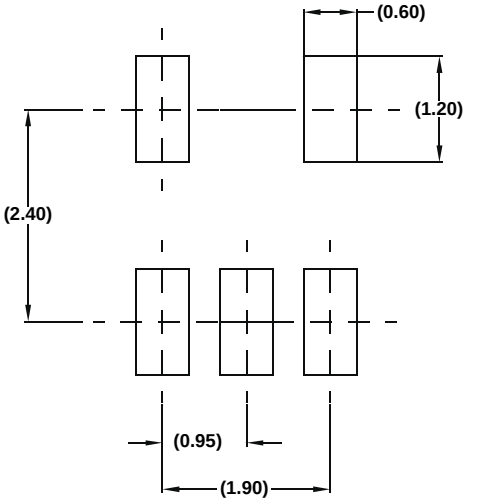
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.