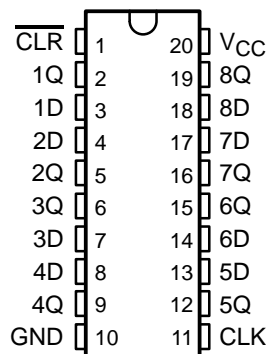


# SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

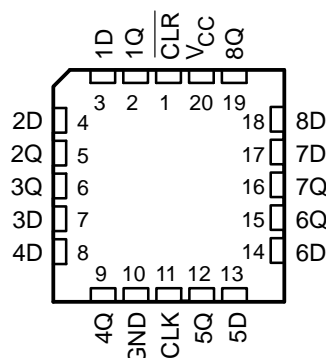
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- Inputs Are TTL-Voltage Compatible
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54AHCT273 . . . J OR W PACKAGE  
SN74AHCT273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT273 . . . FK PACKAGE  
(TOP VIEW)



## description

These devices are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT273N	AHCT273
	SOIC – DW	Tube	SN74AHCT273DW	
		Tape and reel	SN74AHCT273DWR	AHCT273
	SOP – NS	Tape and reel	SN74AHCT273NSR	
	SSOP – DB	Tape and reel	SN74AHCT273DBR	
	TSSOP – PW	Tape and reel	SN74AHCT273PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT273DGVR	HB273
	CDIP – J	Tube	SNJ54AHCT273J	SNJ54AHCT273J
	CFP – W	Tube	SNJ54AHCT273W	SNJ54AHCT273W
	LCCC – FK	Tube	SNJ54AHCT273FK	SNJ54AHCT273FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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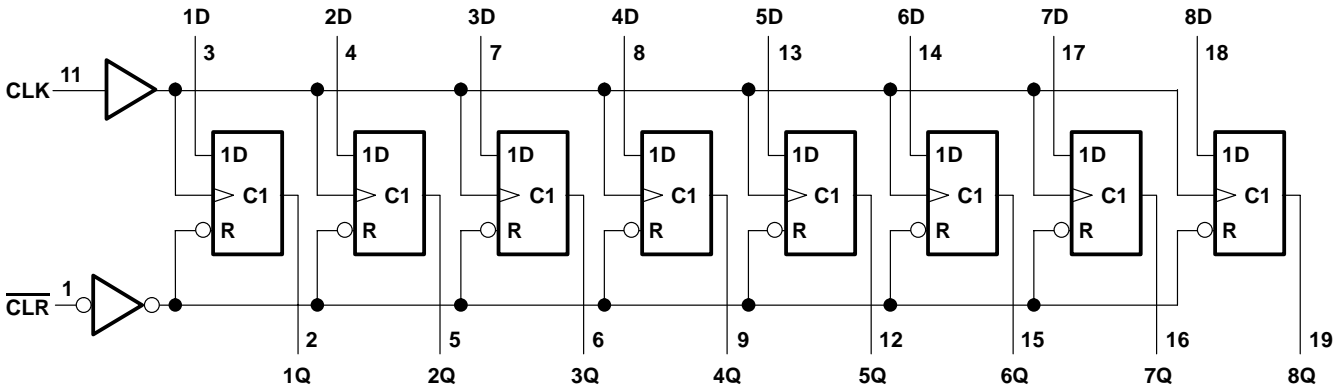
# SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS375E – JUNE 1997 – REVISED APRIL 2002

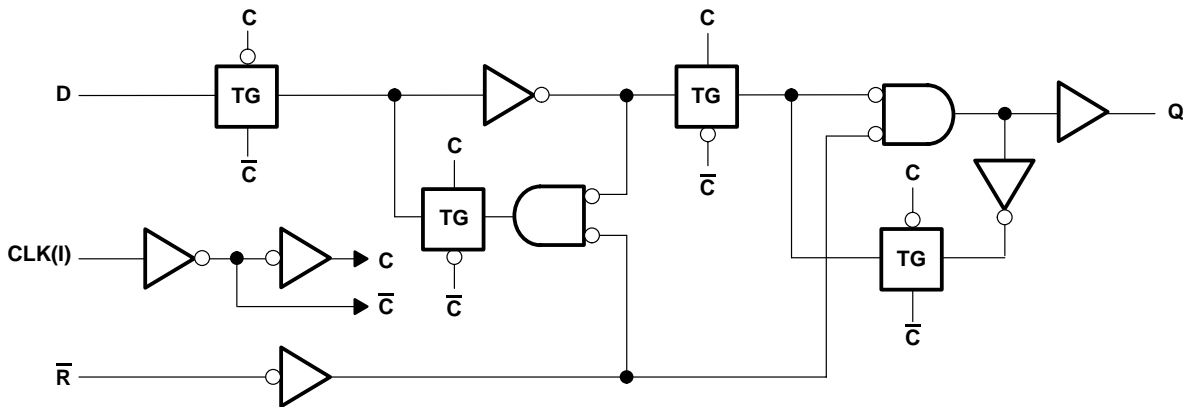
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	$Q_0$

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



## SCLS375E – JUNE 1997 – REVISED APRIL 2002

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	.....	$\pm 75$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):		
	DB package	70°C/W
	DGV package	92°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

		SN54AHCT273		SN74AHCT273		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		−8		−8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall time		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	−55	125	−40	85	°C

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# SN54AHCT273, SN74AHCT273

## OCTAL D-TYPE FLIP-FLOPS

### WITH CLEAR

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT273		SN74AHCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I <sub>OH</sub> = –8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	µA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		SN54AHCT273		SN74AHCT273		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration							ns
	CLR low	5		6		6		
	CLK high or low	5		6.5		6.5		
t <sub>su</sub>	Setup time							ns
	Data before CLK↑	5		5		5		
	CLR before CLK↑	2.5		2.5		2.5		
t <sub>h</sub>	Hold time, data after CLK↑	0		0		0		ns

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT273		SN74AHCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	75**	120**		65**		65		MHz
			C <sub>L</sub> = 50 pF	50	75		45		45		
t <sub>PHL</sub>	CLR	Q	C <sub>L</sub> = 15 pF		7.5**	10**	1**	11.6**	1	11.6	ns
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF		5.5**	7.5**	1**	8.8**	1	8.8	ns
t <sub>PHL</sub>					5.8**	8.2**	1**	10**	1	10	
t <sub>PHL</sub>	CLR	Q	C <sub>L</sub> = 50 pF		8.5	11	1	12.6	1	12.6	ns
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 50 pF		6.5	8.5	1	9.8	1	9.8	ns
t <sub>PHL</sub>					6.8	9.2	1	11	1	11	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1***				1	ns

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

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**SN54AHCT273, SN74AHCT273**  
**OCTAL D-TYPE FLIP-FLOPS**  
**WITH CLEAR**

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**noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)**

PARAMETER	SN74AHCT273			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.76		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.48		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.4		V
$V_{IH(D)}$ High-level dynamic input voltage		2		V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

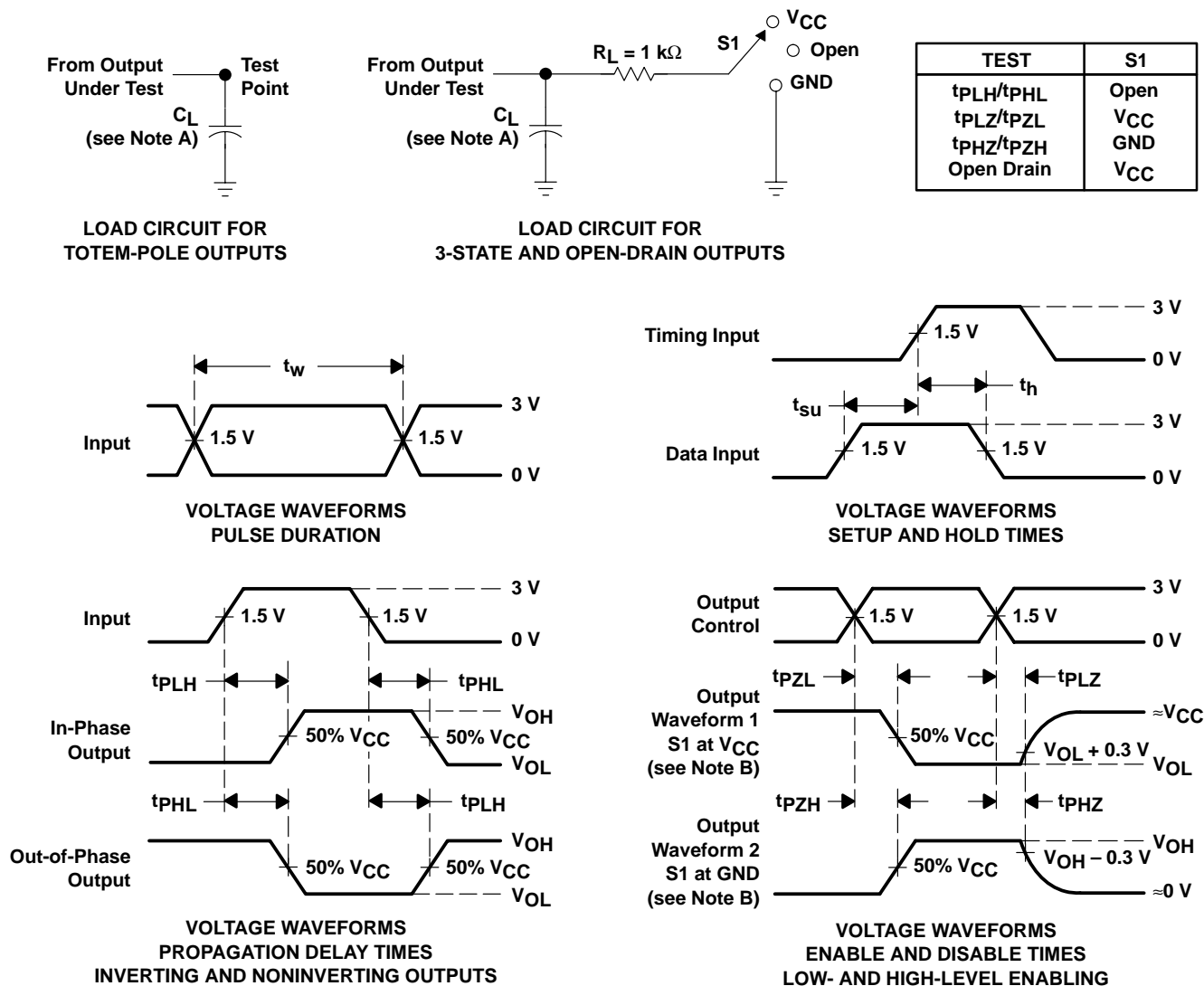
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	27	pF



# SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273DGVRE4	ACTIVE	TVSOP	DGV	20		TBD	Call TI	Call TI	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273DGVRG4	ACTIVE	TVSOP	DGV	20		TBD	Call TI	Call TI	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT273N	<a href="#">Samples</a>
SN74AHCT273NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT273N	<a href="#">Samples</a>
SN74AHCT273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT273	<a href="#">Samples</a>
SN74AHCT273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT273PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>
SN74AHCT273PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT273NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AHCT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHCT273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHCT273PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

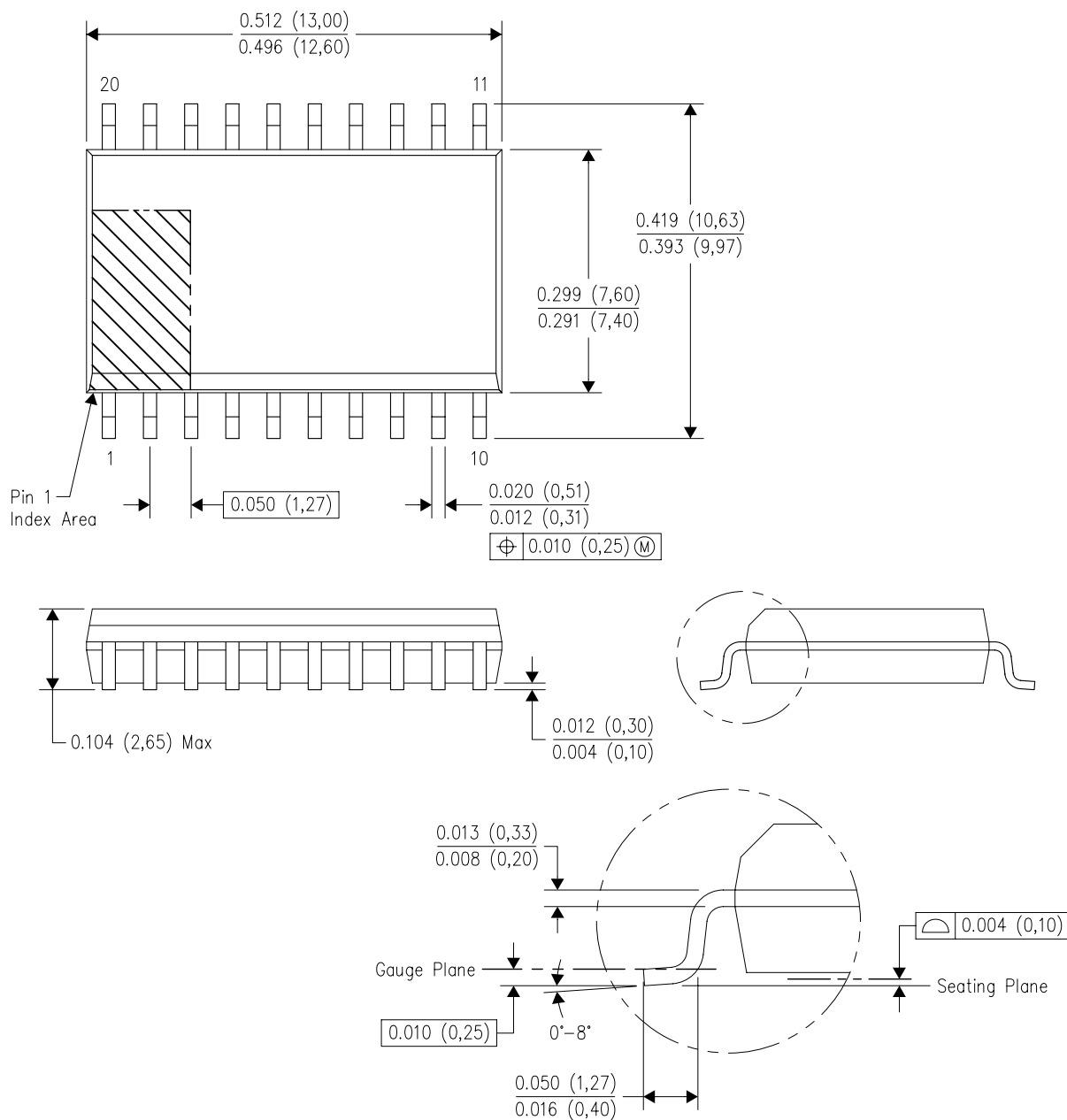
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

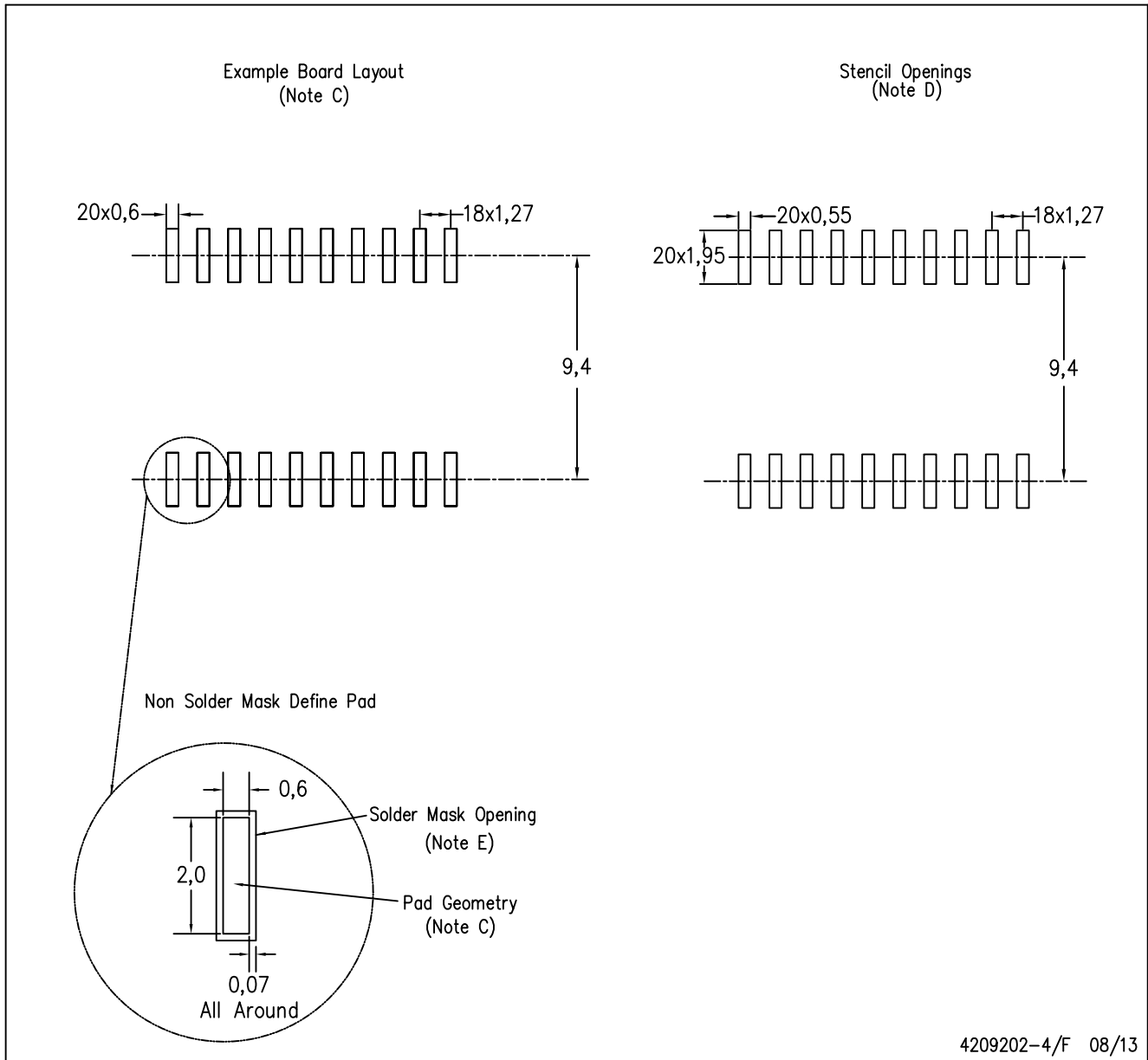


4040000-4/G 01/11

- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



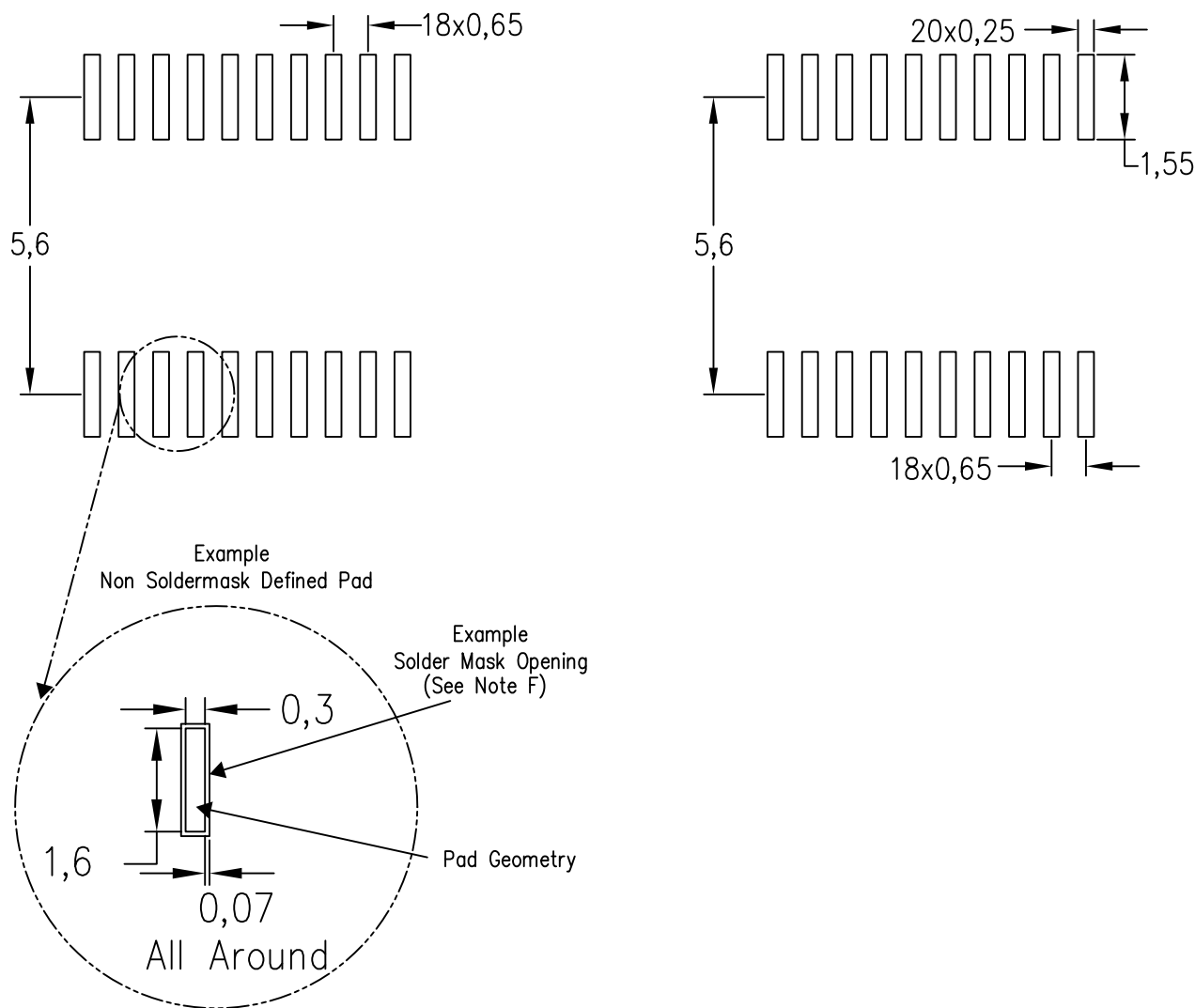
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

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