

CBT3257A

Quad 1-of-2 multiplexer/demultiplexer

Rev. 04 — 19 March 2009

Product data sheet

1. General description

The CBT3257A is a quad 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

Output enable ($\overline{\text{OE}}$) and select-control (S) inputs select the appropriate nB1 and nB2 outputs for the nA input data.

The CBT3257A is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features

- $5\text{ }\Omega$ switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- Latch-up protection exceeds 500 mA per JEDEC standard JESD78 class II level A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
CBT3257AD	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

Table 1. Ordering information ...continued

Type number	Temperature range	Package		
		Name	Description	Version
CBT3257ADS	−40 °C to +85 °C	SSOP16 ^[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3257APW	−40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
CBT3257ABQ	−40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

[1] Also known as QSOP16.

4. Functional diagram

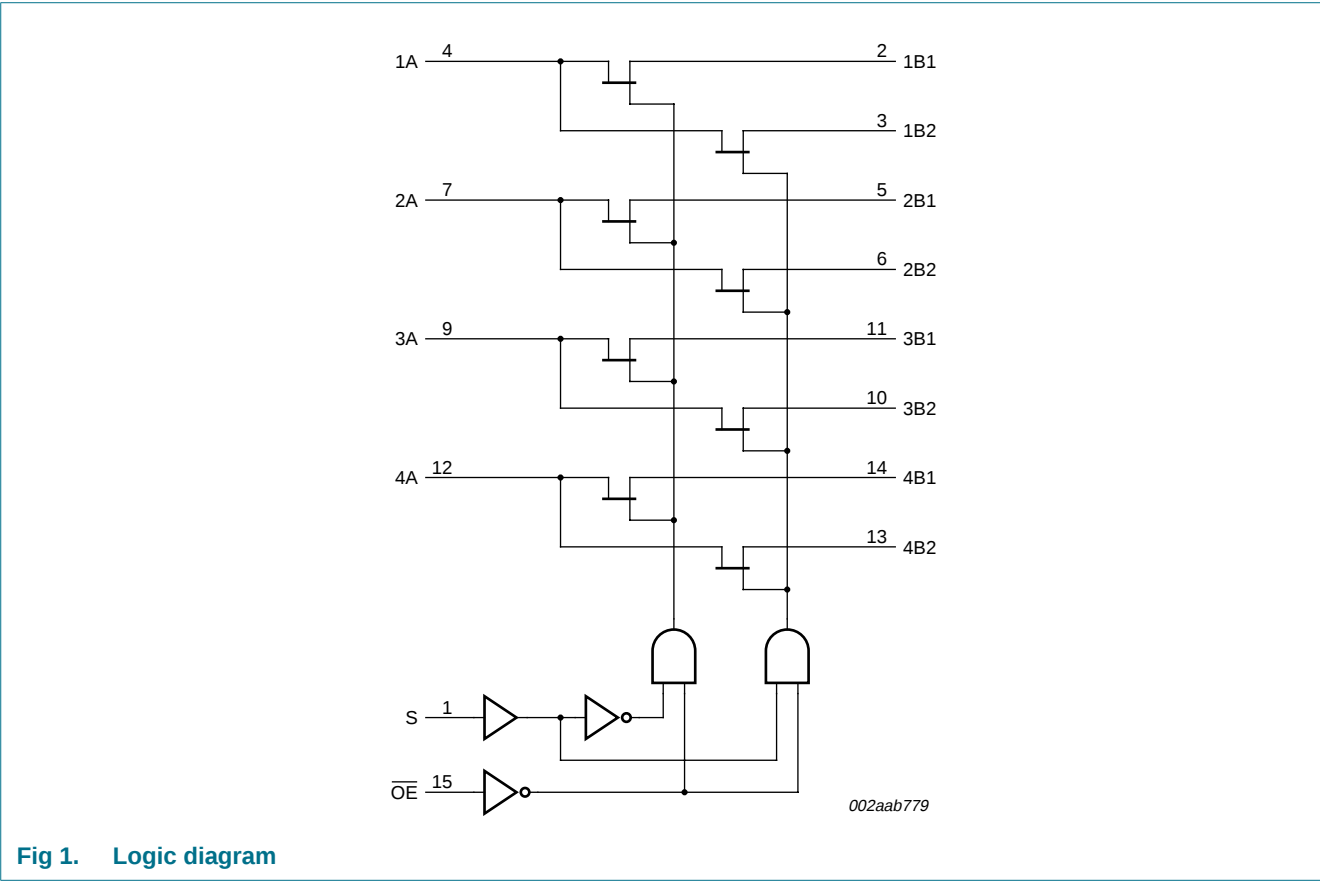
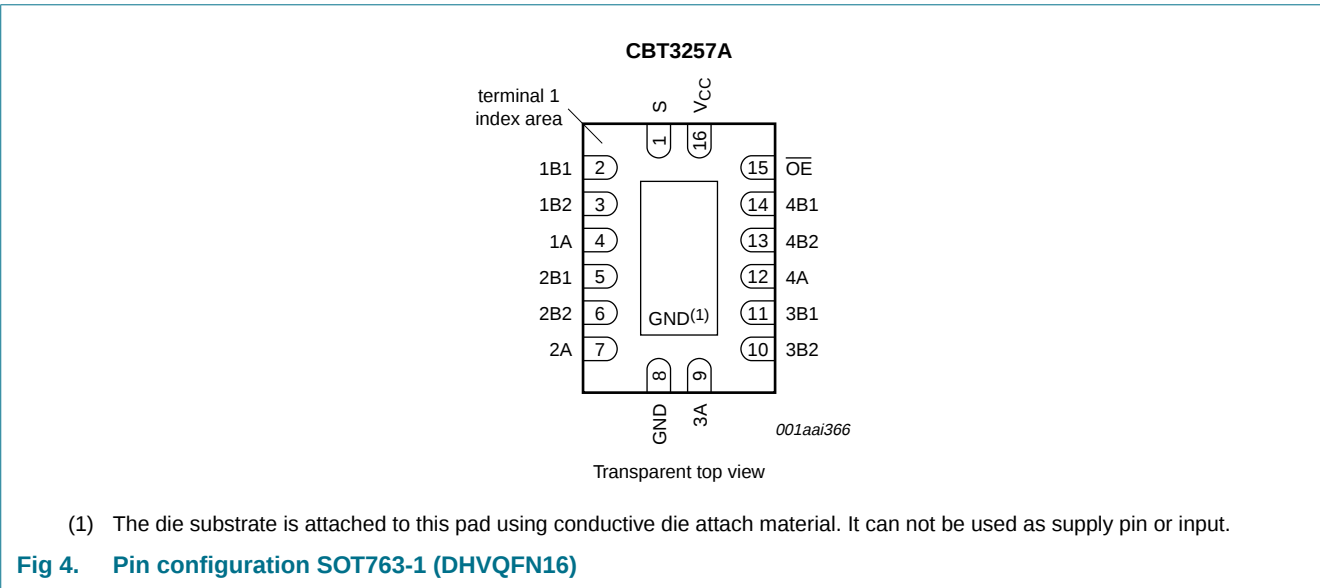
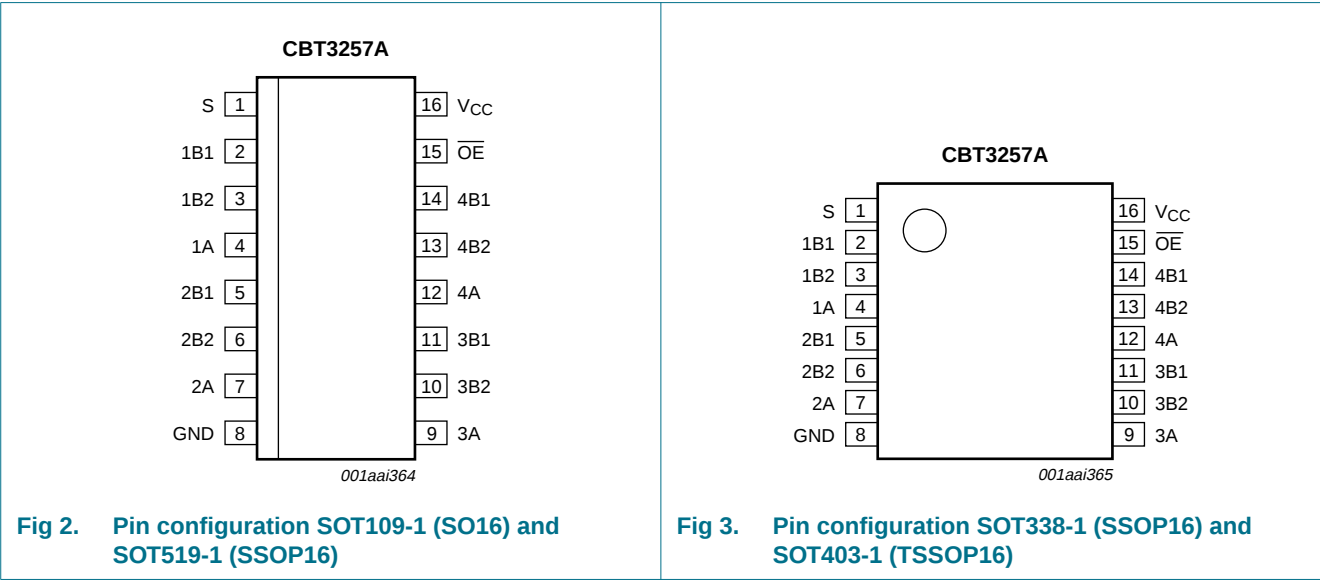


Fig 1. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1B1, 2B1, 3B1, 4B1,	2, 5, 11, 14	B1 outputs/inputs
1B2, 2B2, 3B2, 4B2	3, 6, 10, 13	B2 outputs/inputs
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs/outputs
GND	8	ground (0 V)
$\overline{\text{OE}}$	15	output enable (active LOW)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs		Switch
OE	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	switch off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		[1] -0.5	+7.0	V
I _{SW}	switch current	continuous current through each switch	-	128	mA
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SO16 package	[2] -	500	mW
		SSOP16 package	[3] -	500	mW
		TSSOP16 package	[3] -	500	mW
		DHVQFN16 package	[4] -	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 70 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
T_{amb}	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_I = -18\text{ mA}$	-	-	-1.2	V
V_{pass}	pass voltage	$V_I = V_{CC} = 5.0\text{ V}$; $I_O = -100\text{ }\mu\text{A}$	3.4	3.6	3.9	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	-	± 1	μA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ mA}$; $V_I = V_{CC}$ or GND	-	-	3	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V, other inputs at V_{CC} or GND ^[2]	-	-	2.5	mA
C_I	input capacitance	control pins; $V_I = 3\text{ V}$ or 0 V	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	9.9	-	pF
		B port; $V_O = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	6.4	-	pF
R_{ON}	ON resistance	$V_{CC} = 4.5\text{ V}$ ^[3]				
		$V_I = 0\text{ V}$; $I_I = 64\text{ mA}$	-	5	7	Ω
		$V_I = 0\text{ V}$; $I_I = 30\text{ mA}$	-	5	7	Ω
		$V_I = 2.4\text{ V}$; $I_I = 15\text{ mA}$	-	10	15	Ω

[1] All typical values are measured at $V_{CC} = 5\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

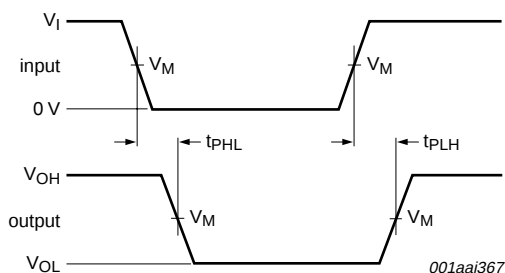
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Max	Unit
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Figure 5	[1][2] -	0.25	ns
		S to nA or nBn; see Figure 5	[1][2] 1.6	5.0	ns
t_{en}	enable time	$\overline{OE}$ to nA or nBn; see Figure 6	[2] 1.8	5.1	ns
		S to nA or nBn; see Figure 6	[2] 1.6	5.2	ns
t_{dis}	disable time	$\overline{OE}$ to nA or nBn; see Figure 6	[2] 2.2	5.5	ns
		S to nA or nBn; see Figure 6	[2] 1.0	5.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{PLH} and t_{PHL} are the same as t_{pd} .
 t_{PZL} and t_{PZH} are the same as t_{en} .
 t_{PLZ} and t_{PHZ} are the same as t_{dis} .

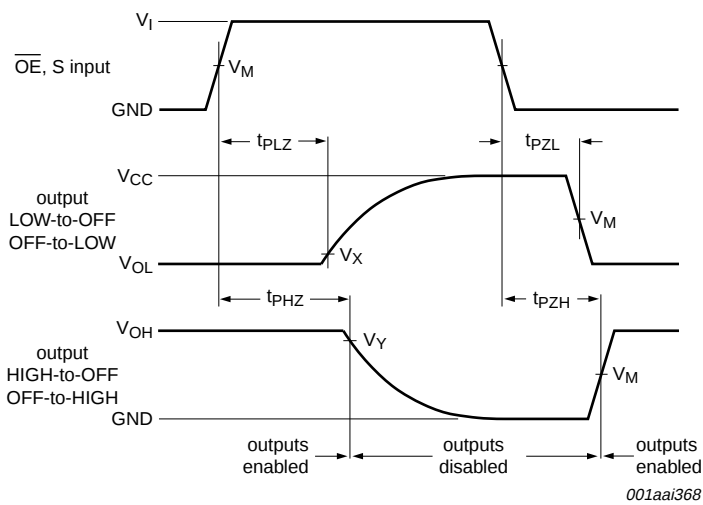
11. AC waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. The input (nA; nBn) to output (nBn; nA) or input (S) to output (nBn; nA) propagation delay times



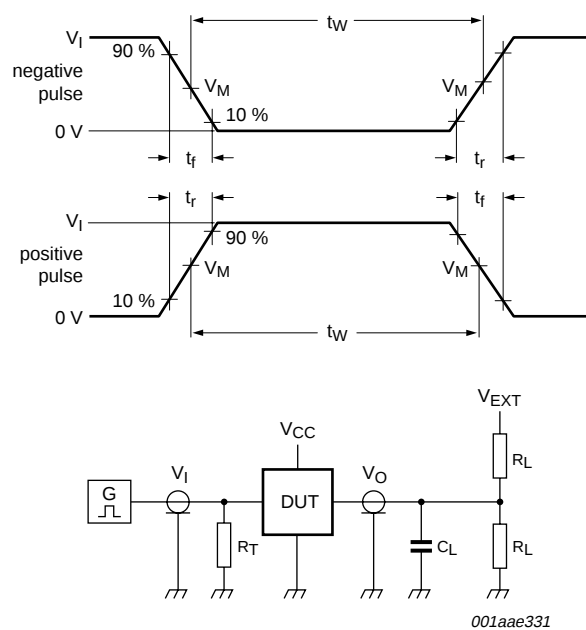
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

12. Test information



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

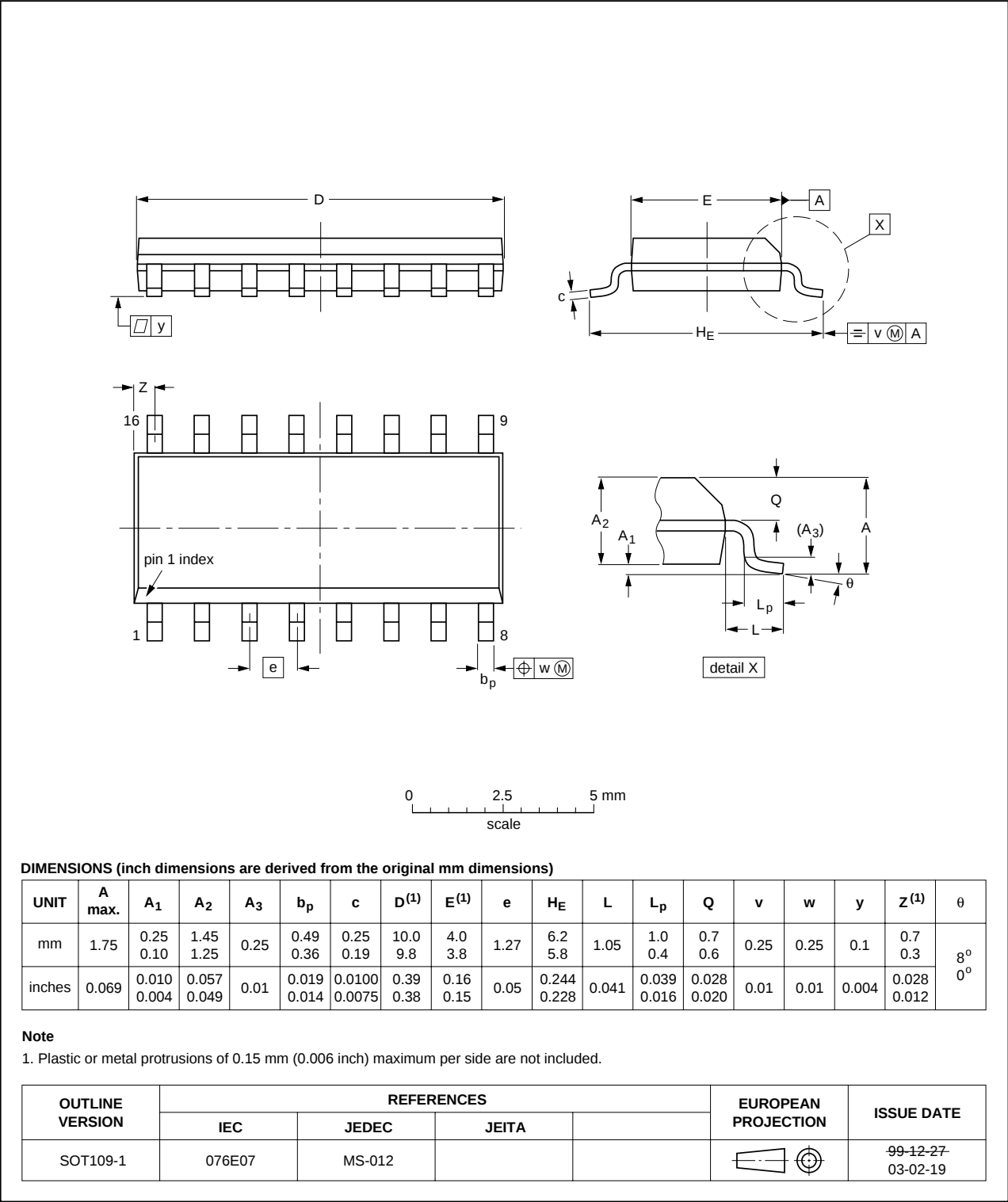


Fig 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

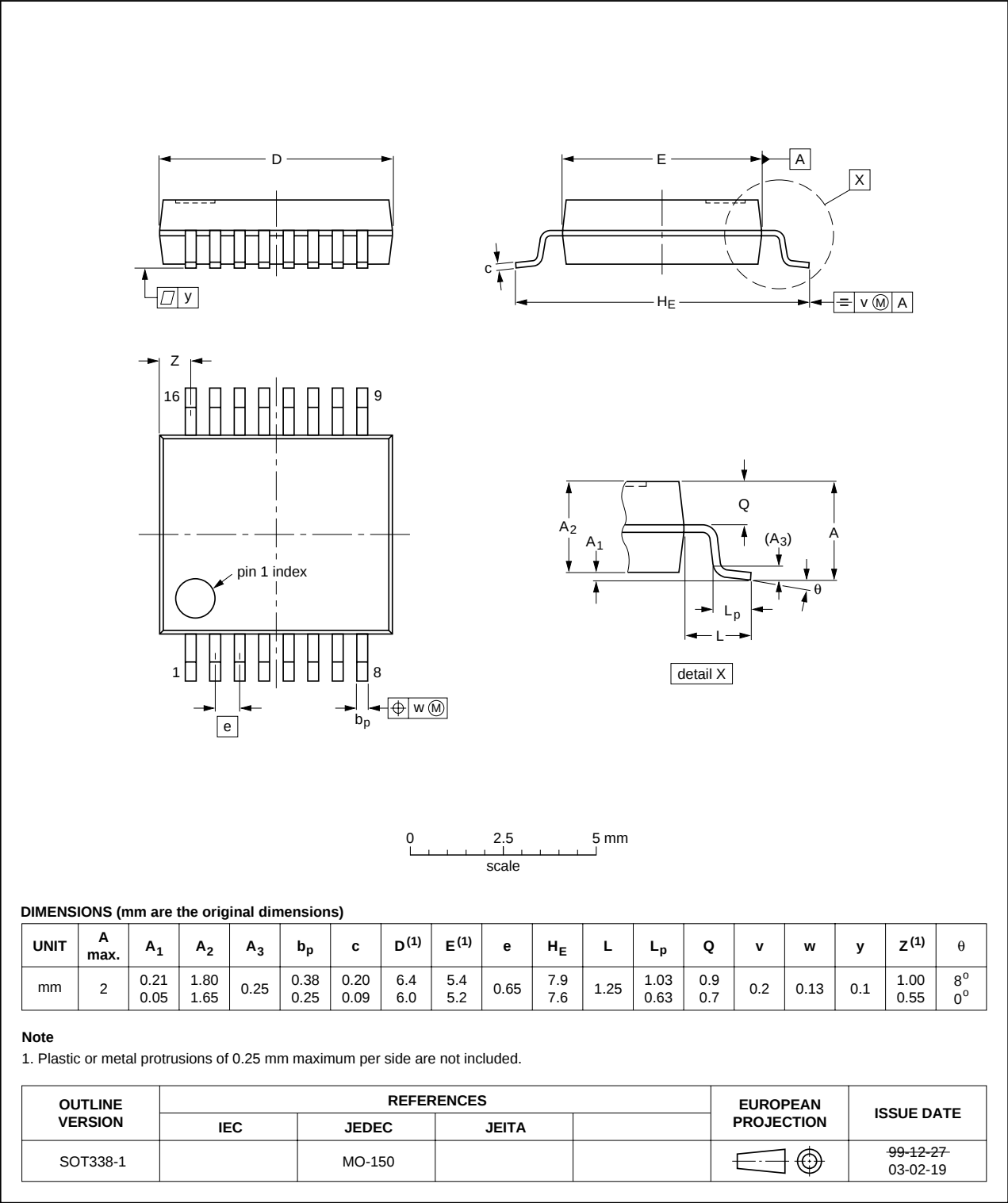


Fig 9. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

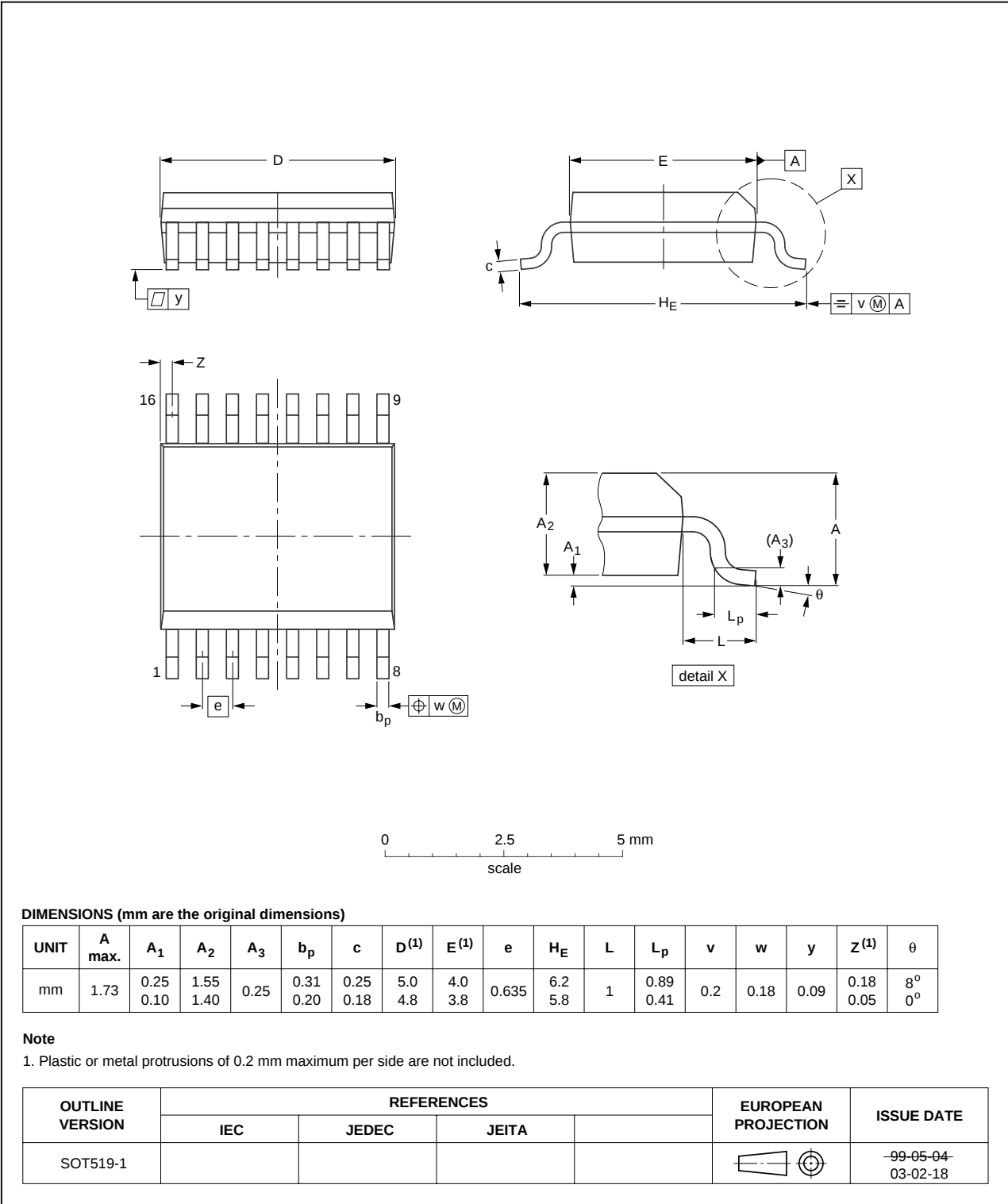


Fig 10. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

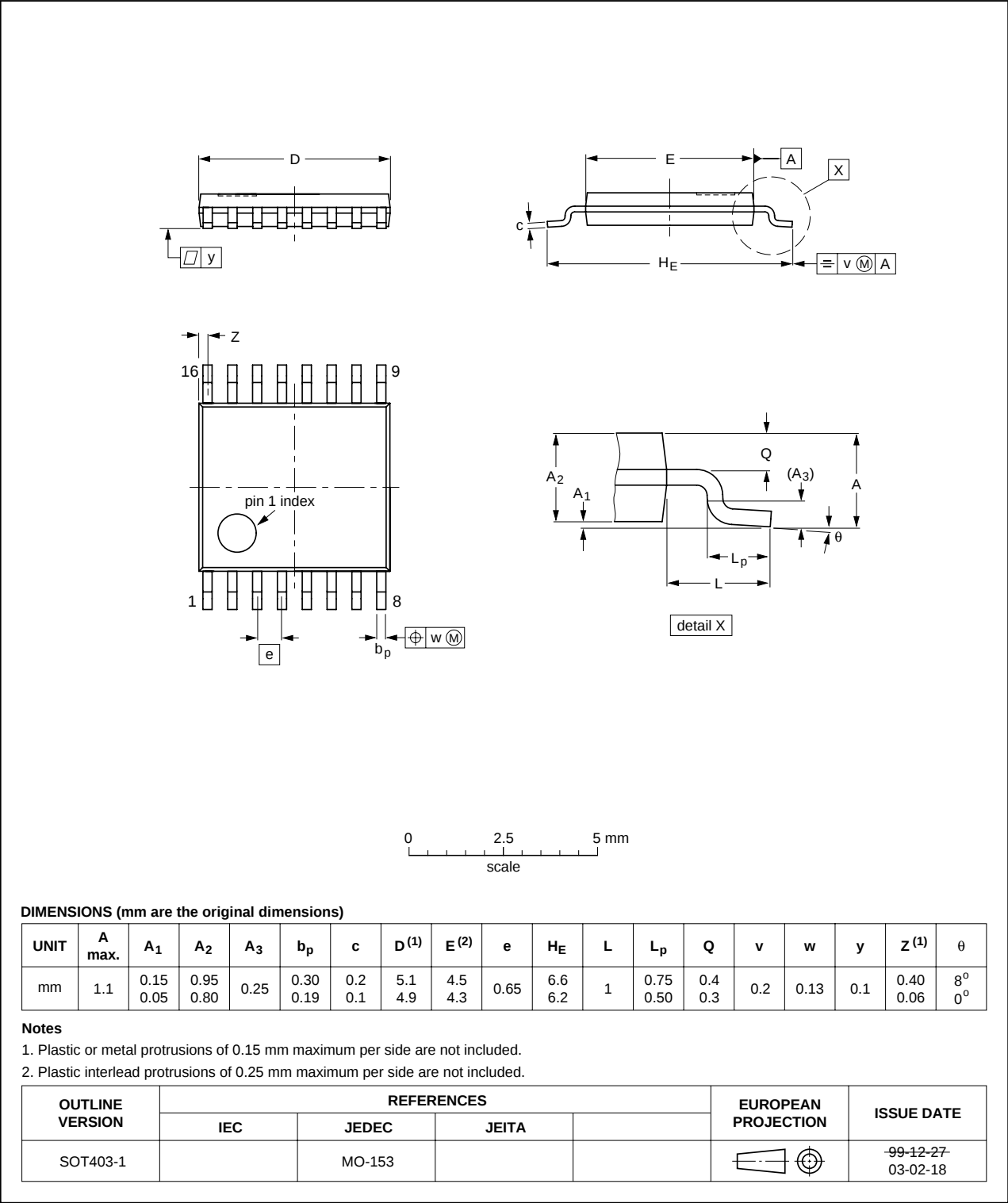


Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

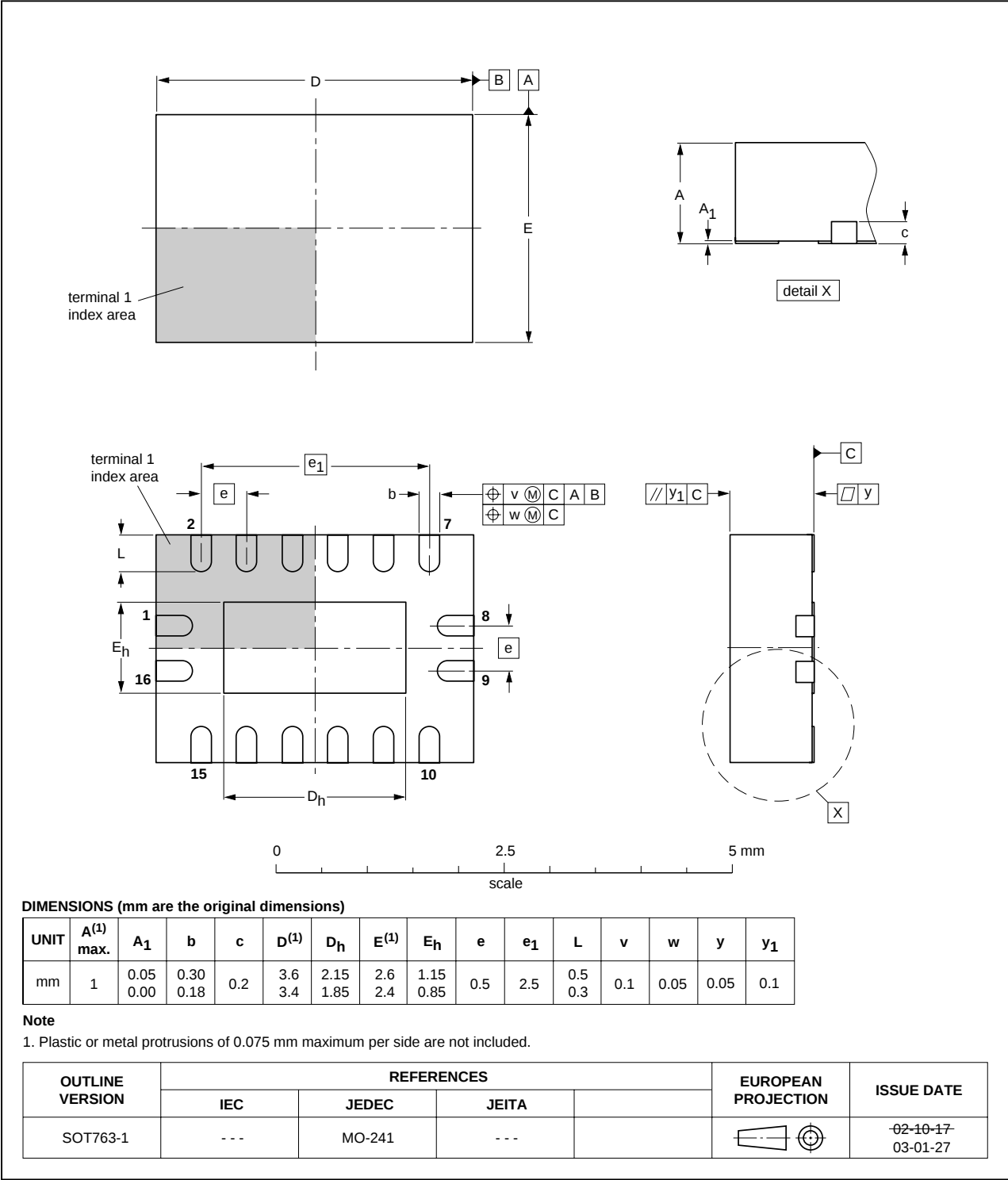


Fig 12. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A_4	20090319	Product data sheet	-	CBT3257A_3
Modifications:	• Table 4 "Limiting values" modified.			
CBT3257A_3	20080704	Product data sheet	-	CBT3257A_2
CBT3257A_2	20070704	Product data sheet	-	CBT3257A_1
CBT3257A_1	20051027	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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