



# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## General Description

The MAX9121/MAX9122 quad low-voltage differential signaling (LVDS) differential line receivers are ideal for applications requiring high data rates, low power, and low noise. The MAX9121/MAX9122 are guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100Ω. The transmission media may be printed circuit (PC) board traces or cables.

The MAX9121/MAX9122 accept four LVDS differential inputs and translate them to LVCMOS outputs. The MAX9122 features integrated parallel termination resistors (nominally 107Ω), which eliminate the requirement for four discrete termination resistors and reduce stub lengths. The MAX9121 inputs are high impedance and require an external termination resistor when used in a point-to-point connection.

The devices support a wide common-mode input range of 0.05V to 2.35V, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or parallel terminated. The EN and  $\overline{\text{EN}}$  inputs control the high-impedance output. The enables are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS outputs. The MAX9121/MAX9122 operate from a single +3.3V supply, and are specified for operation from -40°C to +85°C. These devices are available in 16-pin TSSOP and SO packages. Refer to the MAX9123 data sheet for a quad LVDS line driver with flow-through pinout.

## Applications

Digital Copiers  
Laser Printers  
Cellular Phone Base Stations  
Add/Drop Muxes  
Digital Cross-Connects  
DSLAMs  
Network Switches/Routers  
Backplane Interconnect  
Clock Distribution

## Features

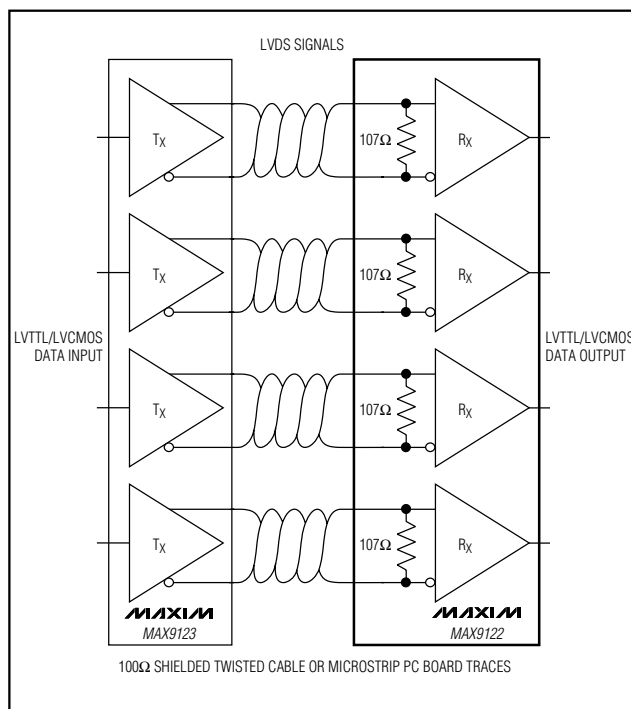
- ♦ Integrated Termination Eliminates Four External Resistors (MAX9122)
- ♦ Flow-Through Pinout  
Simplifies PC Board Layout  
Reduces Crosstalk
- ♦ Pin Compatible with DS90LV048A
- ♦ Guaranteed 500Mbps Data Rate
- ♦ 300ps Pulse Skew (max)
- ♦ Conform to ANSI TIA/EIA-644 LVDS Standard
- ♦ Single +3.3V Supply
- ♦ Fail-Safe Circuit

## Ordering Information

| PART       | TEMP. RANGE    | PIN-PACKAGE |
|------------|----------------|-------------|
| MAX9121EUE | -40°C to +85°C | 16 TSSOP    |
| MAX9121ESE | -40°C to +85°C | 16 SO       |
| MAX9122EUE | -40°C to +85°C | 16 TSSOP    |
| MAX9122ESE | -40°C to +85°C | 16 SO       |

Pin Configuration appears at end of data sheet.

## Typical Application Circuit



# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$  to GND .....-0.3V to +4.0V  
 $IN_+$ ,  $IN_-$  to GND .....-0.3V to +4.0V  
 $EN$ ,  $\overline{EN}$  to GND .....-0.3V to ( $V_{CC} + 0.3V$ )  
 $OUT_-$  to GND .....-0.3V to ( $V_{CC} + 0.3V$ )  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     16-Pin TSSOP (derate 9.4mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....755mW  
     16-Pin SO (derate 8.7mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....696mW

Storage Temperature Range .....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Maximum Junction Temperature .....+150 $^\circ\text{C}$   
 Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$   
 ESD Protection  
     (Human Body Model,  $IN_+$ ,  $IN_-$ ) ..... $\pm 8\text{kV}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.0V$ , common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Note 1)

| PARAMETER                               | SYMBOL                                | CONDITIONS                                                       |                                                             | MIN  | TYP | MAX  | UNITS |
|-----------------------------------------|---------------------------------------|------------------------------------------------------------------|-------------------------------------------------------------|------|-----|------|-------|
| LVDS INPUTS (IN_+, IN_-)                |                                       |                                                                  |                                                             |      |     |      |       |
| Differential Input High Threshold       | V <sub>TH</sub>                       |                                                                  |                                                             |      |     | 100  | mV    |
| Differential Input Low Threshold        | V <sub>TL</sub>                       |                                                                  |                                                             | -100 |     |      | mV    |
| Input Current (MAX9121)                 | I <sub>IN_+</sub> , I <sub>IN_-</sub> | 0.1V ≤  V <sub>ID</sub>   ≤ 0.6V                                 |                                                             | -20  |     | 20   | μA    |
|                                         |                                       | 0.6V <  V <sub>ID</sub>   ≤ 1.0V                                 |                                                             | -25  |     | 25   | μA    |
| Power-Off Input Current (MAX9121)       | I <sub>INOFF</sub>                    | 0.1V ≤  V <sub>ID</sub>   ≤ 0.6V, V <sub>CC</sub> = 0            |                                                             | -20  |     | 20   | μA    |
|                                         |                                       | 0.6V <  V <sub>ID</sub>   ≤ 1.0V, V <sub>CC</sub> = 0            |                                                             | -25  |     | 25   | μA    |
| Input Resistor 1                        | R <sub>IN1</sub>                      | V <sub>CC</sub> = 3.6V or 0, Figure 1                            |                                                             | 35   |     |      | kΩ    |
| Input Resistor 2                        | R <sub>IN2</sub>                      | V <sub>CC</sub> = 3.6V or 0, Figure 1                            |                                                             | 132  |     |      | kΩ    |
| Differential Input Resistance (MAX9122) | R <sub>DIFF</sub>                     | V <sub>CC</sub> = 3.6V or 0, Figure 1                            |                                                             | 90   | 107 | 132  | Ω     |
| LVCMOS/LVTTL OUTPUTS (OUT_-)            |                                       |                                                                  |                                                             |      |     |      |       |
| Output High Voltage (Table 1)           | V <sub>OH</sub>                       | I <sub>OH</sub> = -4.0mA (MAX9121)                               | Open, undriven short, or undriven 100Ω parallel termination | 2.7  | 3.2 |      | V     |
|                                         |                                       |                                                                  | V <sub>ID</sub> = +100mV                                    | 2.7  | 3.2 |      |       |
|                                         |                                       | I <sub>OH</sub> = -4.0mA (MAX9122)                               | Open or undriven short                                      | 2.7  | 3.2 |      |       |
|                                         |                                       |                                                                  | V <sub>ID</sub> = +100mV                                    | 2.7  | 3.2 |      |       |
| Output Low Voltage                      | V <sub>OL</sub>                       | I <sub>OL</sub> = +4.0mA, V <sub>ID</sub> = -100mV               |                                                             |      | 0.1 | 0.25 | V     |
| Output Short-Circuit Current            | I <sub>OS</sub>                       | Enabled, V <sub>ID</sub> = 0.1V, V <sub>OUT_-</sub> = 0 (Note 2) |                                                             | -15  |     | -120 | mA    |
| Output High-Impedance Current           | I <sub>OZ</sub>                       | Disabled, V <sub>OUT</sub> = 0 or V <sub>CC</sub>                |                                                             | -10  |     | +10  | μA    |

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.0V$ , common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                                    | SYMBOL    | CONDITIONS             | MIN | TYP  | MAX      | UNITS   |
|------------------------------------------------------------------------------|-----------|------------------------|-----|------|----------|---------|
| <b>LOGIC INPUTS (<math>\overline{EN}</math>, <math>\overline{EN}</math>)</b> |           |                        |     |      |          |         |
| Input High Voltage                                                           | $V_{IH}$  |                        | 2.0 |      | $V_{CC}$ | V       |
| Input Low Voltage                                                            | $V_{IL}$  |                        | 0   |      | 0.8      | V       |
| Input Current                                                                | $I_{IN}$  | $V_{IN} = V_{CC}$ or 0 | -15 |      | 15       | $\mu A$ |
| <b>SUPPLY</b>                                                                |           |                        |     |      |          |         |
| Supply Current                                                               | $I_{CC}$  | Enabled, inputs open   |     | 9    | 15       | mA      |
| Disabled Supply Current                                                      | $I_{CCZ}$ | Disabled, inputs open  |     | 0.07 | 0.5      | mA      |

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $C_L = 15pF$ , differential input voltage  $|V_{ID}| = 0.2V$  to  $1.0V$ , common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ , input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $V_{CM} = 1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Notes 3, 4)

| PARAMETER                                                  | SYMBOL     | CONDITIONS                         | MIN | TYP  | MAX | UNITS |
|------------------------------------------------------------|------------|------------------------------------|-----|------|-----|-------|
| Differential Propagation Delay High to Low                 | $t_{PHLD}$ | Figures 2 and 3                    | 1.2 | 1.93 | 2.7 | ns    |
| Differential Propagation Delay Low to High                 | $t_{PLHD}$ | Figures 2 and 3                    | 1.2 | 1.79 | 2.7 | ns    |
| Differential Pulse Skew [ $t_{PHLD} - t_{PLHD}$ ] (Note 5) | $t_{SKD1}$ | Figures 2 and 3                    |     | 140  | 300 | ps    |
| Differential Channel-to-Channel Skew (Note 6)              | $t_{SKD2}$ | Figures 2 and 3                    |     |      | 400 | ps    |
| Differential Part-to-Part Skew (Note 7)                    | $t_{SKD3}$ | Figures 2 and 3                    |     |      | 0.8 | ns    |
| Differential Part-to-Part Skew (Note 8)                    | $t_{SKD4}$ | Figures 2 and 3                    |     |      | 1.5 | ns    |
| Rise-Time                                                  | $t_{TLH}$  | Figures 2 and 3                    |     | 0.55 | 1.0 | ns    |
| Fall-Time                                                  | $t_{THL}$  | Figures 2 and 3                    |     | 0.54 | 1.0 | ns    |
| Disable Time High to Z                                     | $t_{PHZ}$  | $R_L = 2k\Omega$ , Figures 4 and 5 |     |      | 14  | ns    |
| Disable Time Low to Z                                      | $t_{PLZ}$  | $R_L = 2k\Omega$ , Figures 4 and 5 |     |      | 14  | ns    |
| Enable Time Z to High                                      | $t_{PZH}$  | $R_L = 2k\Omega$ , Figures 4 and 5 |     |      | 70  | ns    |
| Enable Time Z to Low                                       | $t_{PZL}$  | $R_L = 2k\Omega$ , Figures 4 and 5 |     |      | 70  | ns    |
| Maximum Operating Frequency (Note 9)                       | $f_{MAX}$  | All channels switching             | 250 | 300  |     | MHz   |

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $C_L = 15pF$ , differential input voltage  $|V_{ID}| = 0.2V$  to  $1.0V$ , common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ , input rise and fall time =  $1ns$  (20% to 80%), input frequency =  $100MHz$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $V_{CM} = 1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 3, 4)

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$ ,  $V_{TL}$ , and  $V_{ID}$ .

**Note 2:** Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

**Note 3:** AC parameters are guaranteed by design and characterization.

**Note 4:**  $C_L$  includes scope probe and test jig capacitance.

**Note 5:**  $t_{SKD1}$  is the magnitude difference of differential propagation delays in a channel.  $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$ .

**Note 6:**  $t_{SKD2}$  is the magnitude difference of the  $t_{PLHD}$  or  $t_{PHLD}$  of one channel and the  $t_{PLHD}$  or  $t_{PHLD}$  of any other channel on the same part.

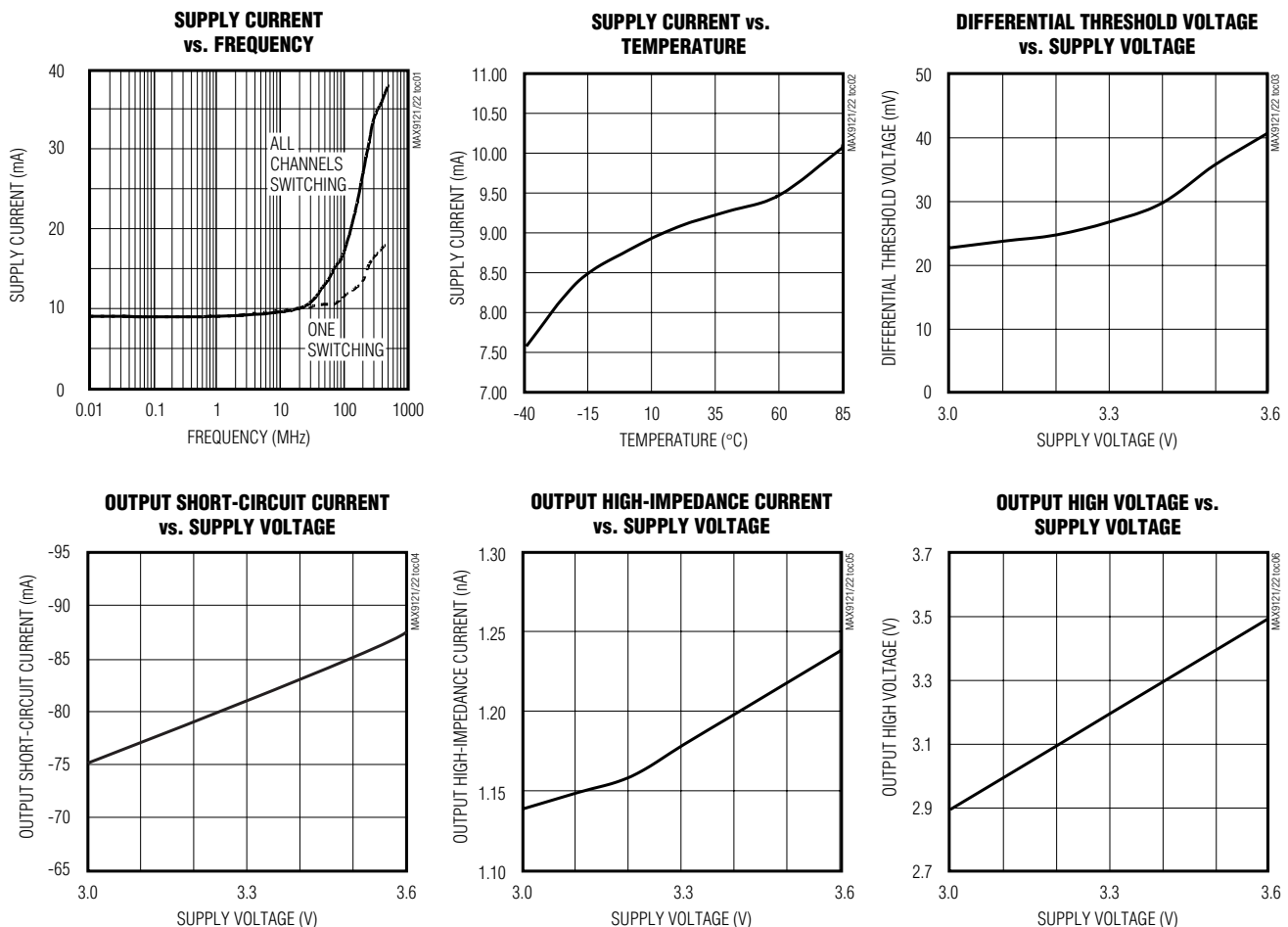
**Note 7:**  $t_{SKD3}$  is the magnitude difference of any differential propagation delays between parts operating over rated conditions at the same  $V_{CC}$  and within  $5^\circ C$  of each other.

**Note 8:**  $t_{SKD4}$  is the magnitude difference of any differential propagation delays between parts operating over rated conditions.

**Note 9:**  $f_{MAX}$  generator output conditions: rise-time = fall-time =  $1ns$  (0% to 100%), 50% duty cycle,  $V_{OH} = +1.3V$ ,  $V_{OL} = +1.1V$ , MAX9121/MAX9122 output criteria: 60% to 40% duty cycle,  $V_{OL} = 0.4V$  (max),  $V_{OH} = 2.7V$  (min), load =  $15pF$ .

## Typical Operating Characteristics

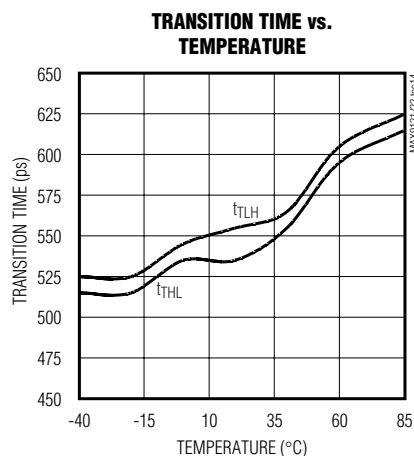
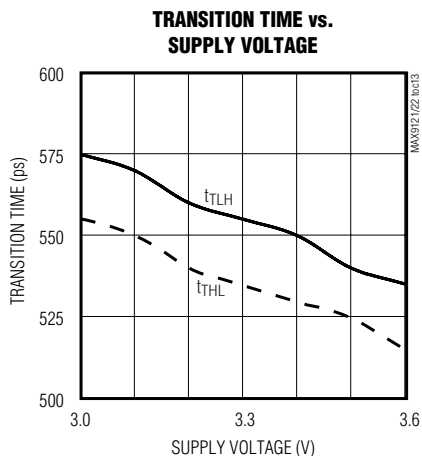
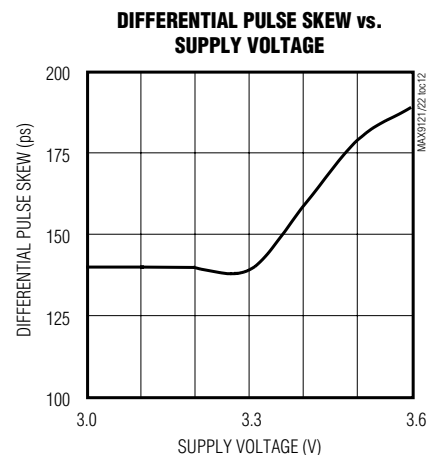
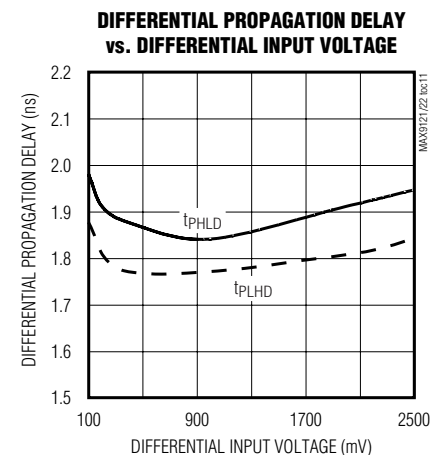
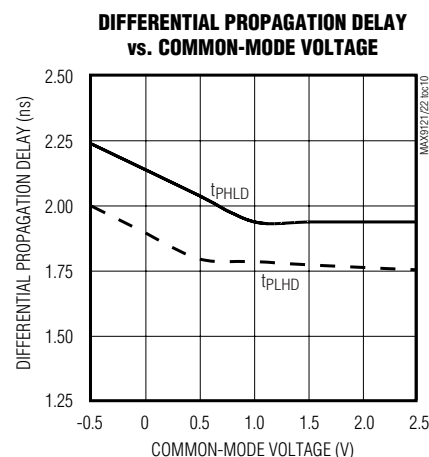
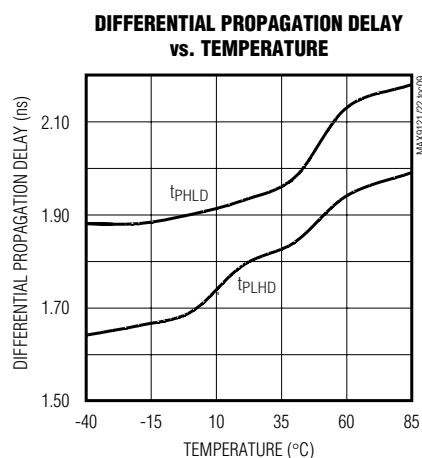
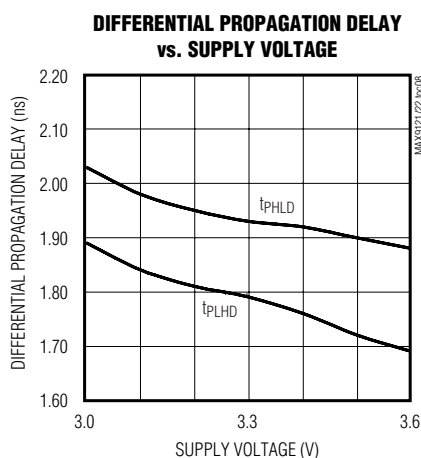
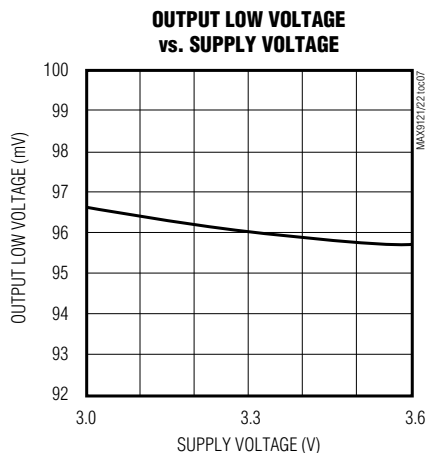
( $V_{CC} = +3.3V$ ,  $V_{CM} = +1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Figures 2 and 3)



# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $V_{CM} = +1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Figures 2 and 3)



MAX9121/MAX9122

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## Pin Description

| PIN            | NAME                        | FUNCTION                                                                                                                                                                                                           |
|----------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 4, 5, 8     | IN <sub>-</sub>             | Inverting Differential Receiver Inputs                                                                                                                                                                             |
| 2, 3, 6, 7     | IN <sub>+</sub>             | Noninverting Differential Receiver Inputs                                                                                                                                                                          |
| 9, 16          | $\overline{\text{EN}}$ , EN | Receiver Enable Inputs. When EN = high and $\overline{\text{EN}}$ = low or open, the outputs are active. For other combinations of EN and $\overline{\text{EN}}$ , the outputs are disabled and in high impedance. |
| 10, 11, 14, 15 | OUT <sub>-</sub>            | LVC MOS/LVTTL Receiver Outputs                                                                                                                                                                                     |
| 12             | GND                         | Ground                                                                                                                                                                                                             |
| 13             | V <sub>CC</sub>             | Power-Supply Input. Bypass V <sub>CC</sub> to GND with 0.1μF and 0.001μF ceramic capacitors.                                                                                                                       |

**Table 1. Input/Output Function Table**

| ENABLES                               |                        | INPUTS                                  |                                                             | OUTPUT           |
|---------------------------------------|------------------------|-----------------------------------------|-------------------------------------------------------------|------------------|
| EN                                    | $\overline{\text{EN}}$ | (IN <sub>+</sub> ) - (IN <sub>-</sub> ) |                                                             | OUT <sub>-</sub> |
| H                                     | L or open              | V <sub>ID</sub> ≥ +100mV                |                                                             | H                |
|                                       |                        | V <sub>ID</sub> ≤ -100mV                |                                                             | L                |
|                                       |                        | MAX9121                                 | Open, undriven short, or undriven 100Ω parallel termination | H                |
|                                       |                        | MAX9122                                 | Open or undriven short                                      |                  |
| All other combinations of ENABLE pins |                        | Don't care                              |                                                             | Z                |

## Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9121/MAX9122 are 500Mbps, four-channel LVDS receivers intended for high-speed, point-to-point, low-power applications. Each channel accepts an LVDS input and translates it to an LVTTL/LVC MOS output. The receiver is capable of detecting differential signals as low as 100mV and as high as 1V within an input voltage range of 0 to 2.4V. The 250mV to 400mV differential output of an LVDS driver is nominally centered around a +1.2V offset. This offset, coupled with the receiver's 0 to 2.4V input voltage range, allows an approximate ±1V shift in the signal (as seen by the receiver). This allows for a difference in ground refer-

ences of the transmitter and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to +2.4V referenced to receiver ground.

The MAX9122 has an integrated termination resistor that is internally connected across each receiver input. The internal termination saves board space, eases layout, and reduces stub length compared to an external termination resistor. In other words, the transmission line is terminated on the IC.

### Fail-Safe

The fail-safe feature of the MAX9121/MAX9122 sets an output high when:

- Inputs are open.
- Inputs are undriven and shorted.
- Inputs are undriven and terminated.

A fail-safe circuit is important because under these conditions, noise at the inputs may switch the receiver and it may appear to the system that data is being

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MAX9121/MAX9122

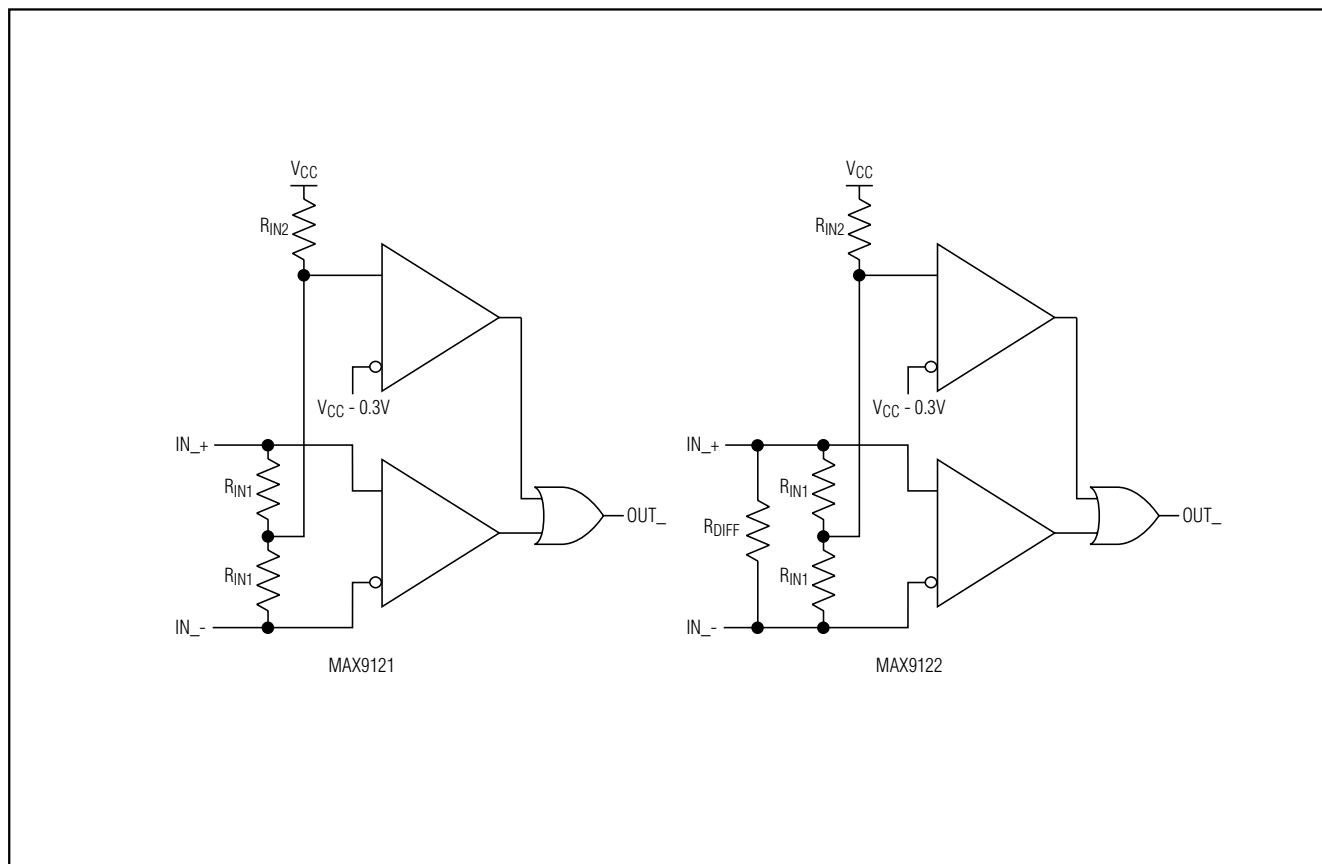


Figure 1. Input with Fail-Safe Network

received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when the LVDS driver outputs are high impedance. A short condition can occur because of a cable failure.

The fail-safe input network (Figure 1) samples the input common-mode voltage and compares it to  $V_{CC} - 0.3V$  (nominal). When the input is driven to levels specified in the LVDS standards, the input to the common-mode voltage is less than  $V_{CC} - 0.3V$  and the fail-safe circuit is not activated. If the inputs are open or if the inputs are undriven and shorted or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the fail-safe circuit pulls both inputs above  $V_{CC} - 0.3V$ , activating the fail-safe circuit and forcing the output high.

## Applications Information

### Power-Supply Bypassing

Bypass the  $V_{CC}$  pin with high-frequency surface-mount ceramic  $0.1\mu F$  and  $0.001\mu F$  capacitors in parallel as

close to the device as possible, with the smaller valued capacitor closest to  $V_{CC}$ .

### Differential Traces

Input trace characteristics affect the performance of the MAX9121/MAX9122. Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor is also matched to this characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Each channel's differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid  $90^\circ$  turns and minimize the number of vias to further prevent impedance discontinuities.

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

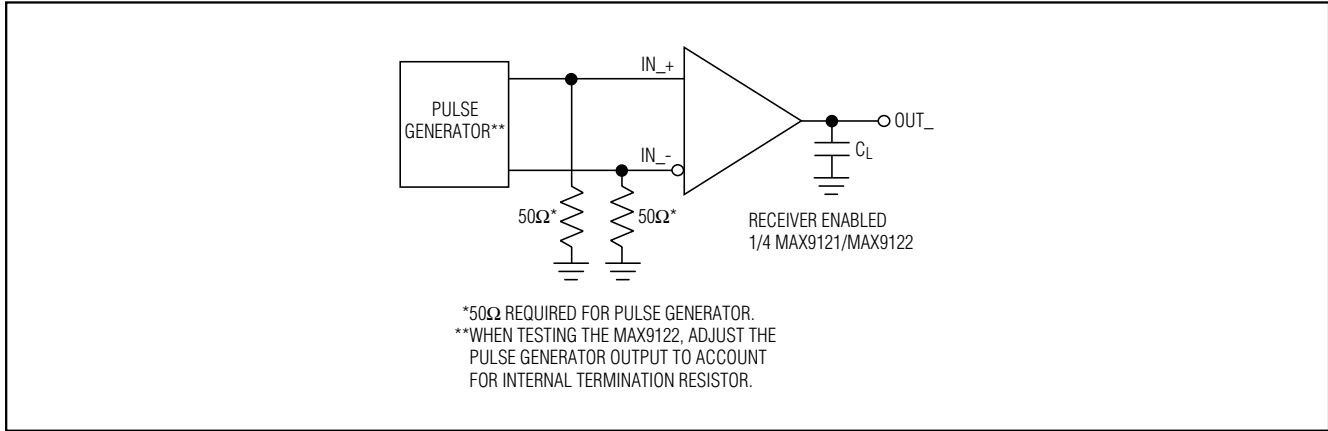


Figure 2. Propagation Delay and Transition Time Test Circuit

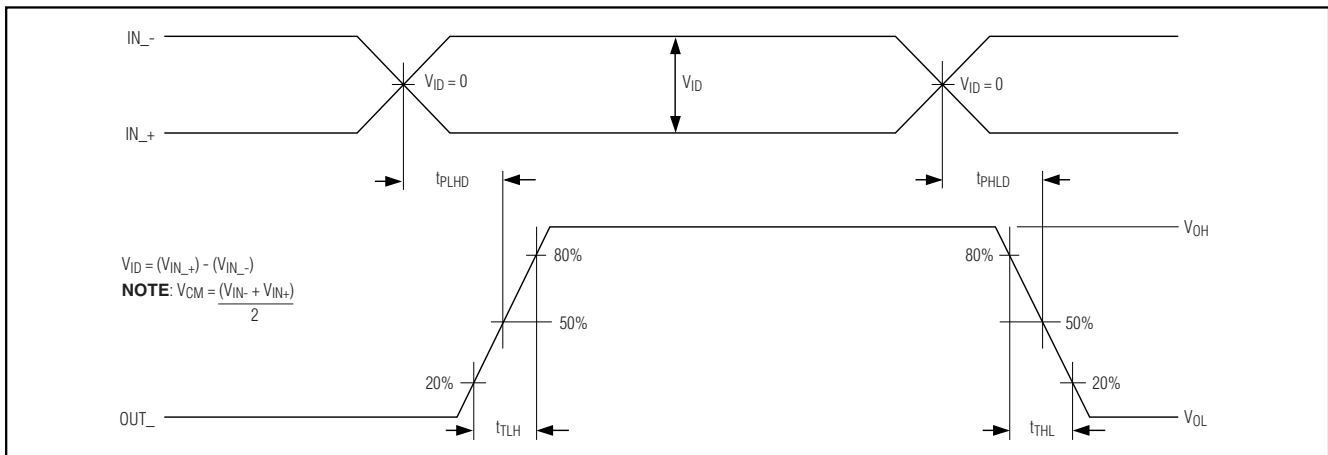


Figure 3. Propagation Delay and Transition Time Waveforms

## Cables and Connectors

Transmission media typically have a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

## Termination

The MAX9122 has an integrated termination resistor connected across the inputs of each receiver. The

value of the integrated resistor is specified in the DC characteristics.

The MAX9121 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance values may range between 90Ω to 132Ω, depending on the characteristic impedance of the transmission medium.

When using the MAX9121, minimize the distance between the input termination resistors and the MAX9121 receiver inputs. Use 1% surface-mount resistors.



# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

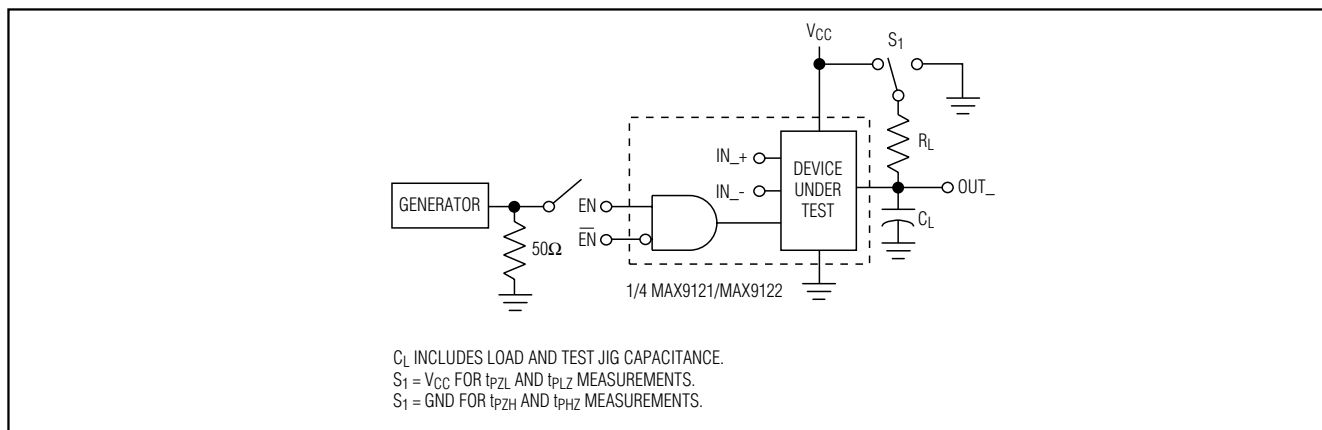


Figure 4. High-Impedance Delay Test Circuit

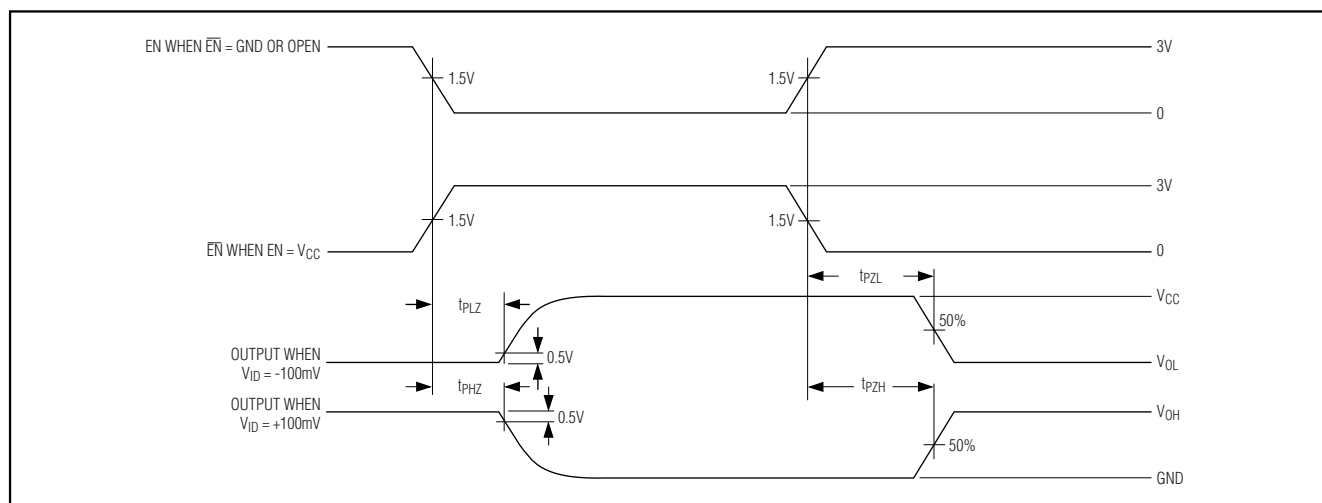


Figure 5. High-Impedance Delay Waveforms

## Board Layout

Because the MAX9121/MAX9122 feature a flow-through pinout, no special layout precautions are required. Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the input LVDS signals from each other to prevent coupling. Isolate the output LVCMOS/LVTTL signals from each other to prevent coupling. Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

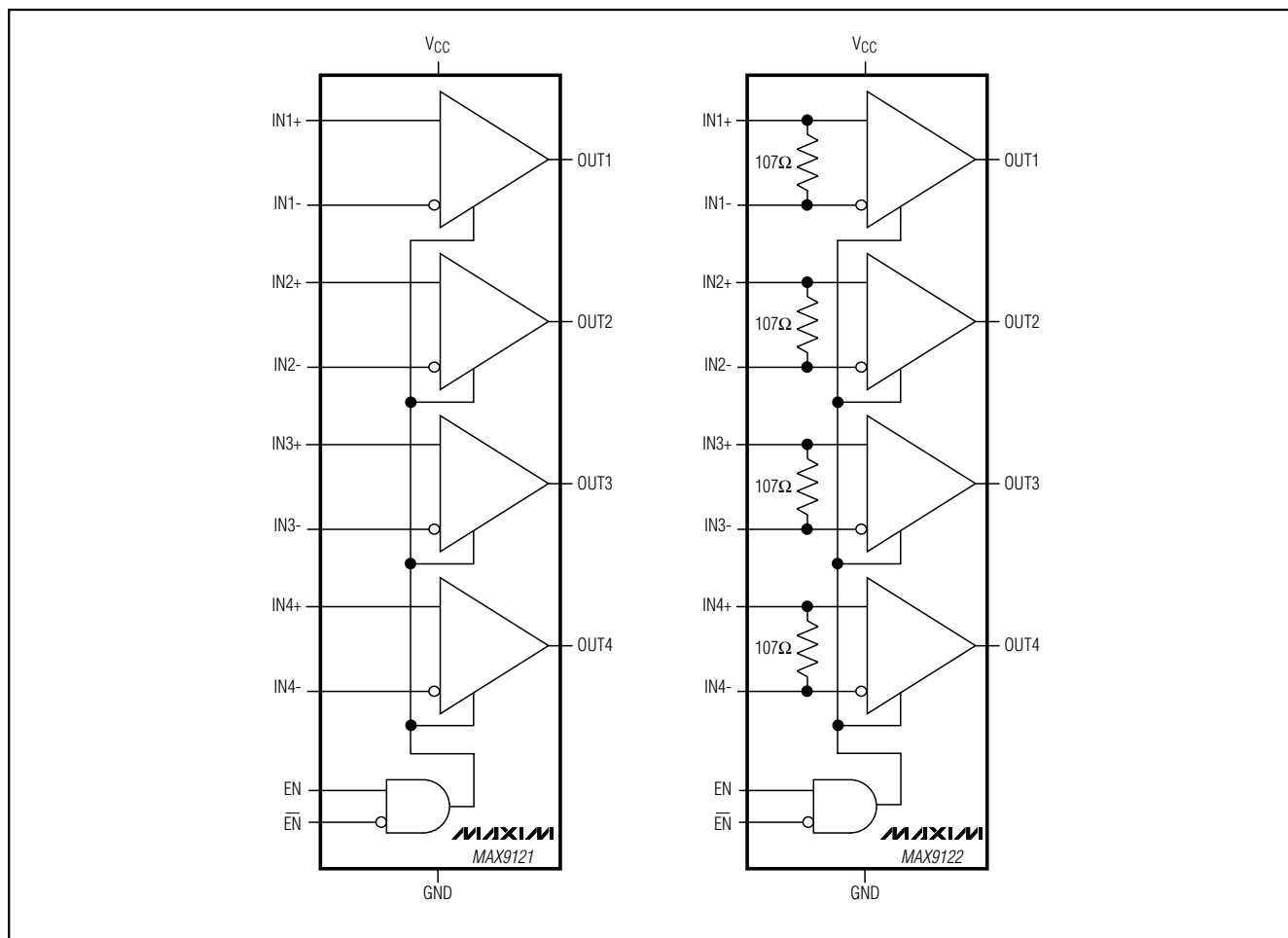
## Chip Information

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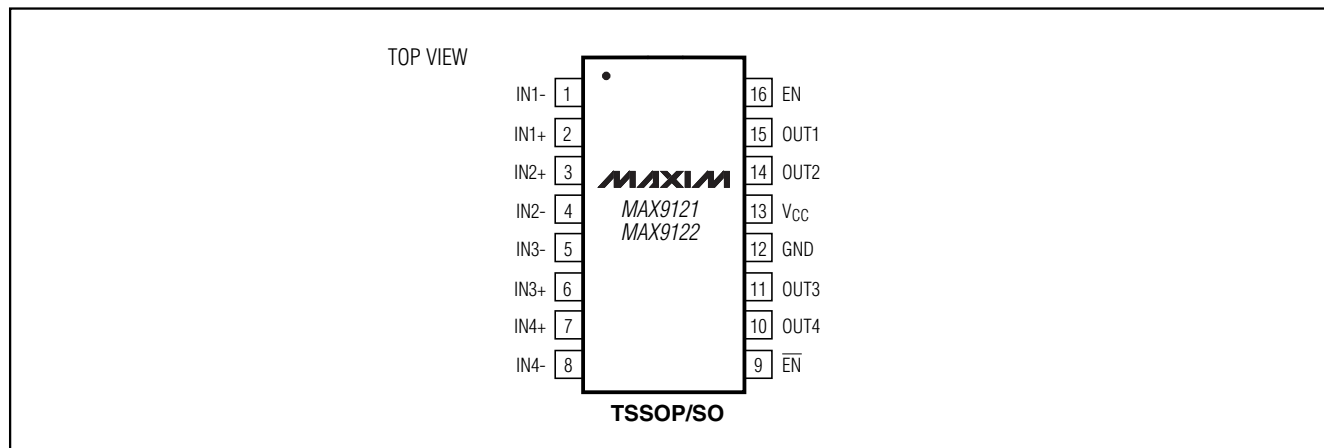
PROCESS: CMOS

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## Functional Diagram

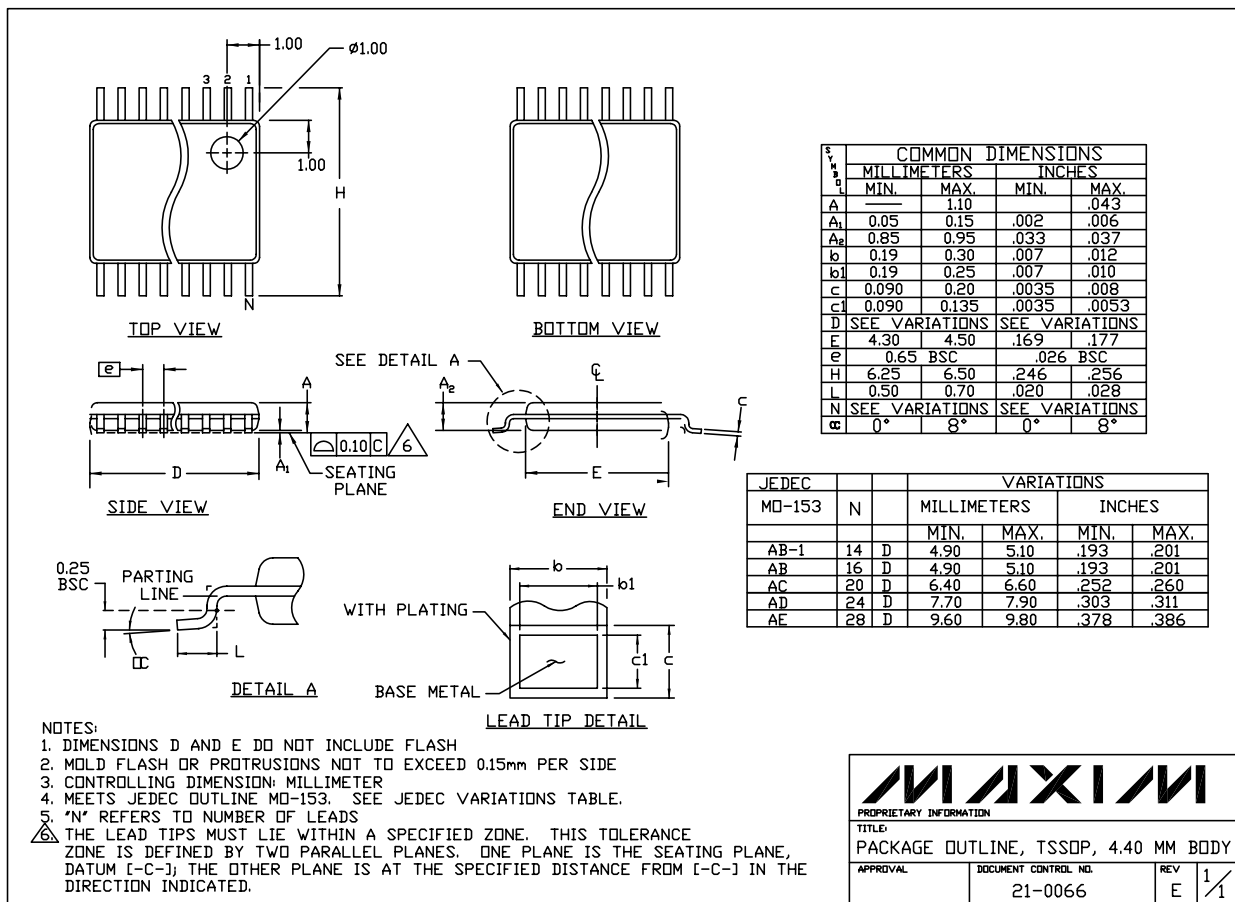


## Pin Configuration



# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## Package Information

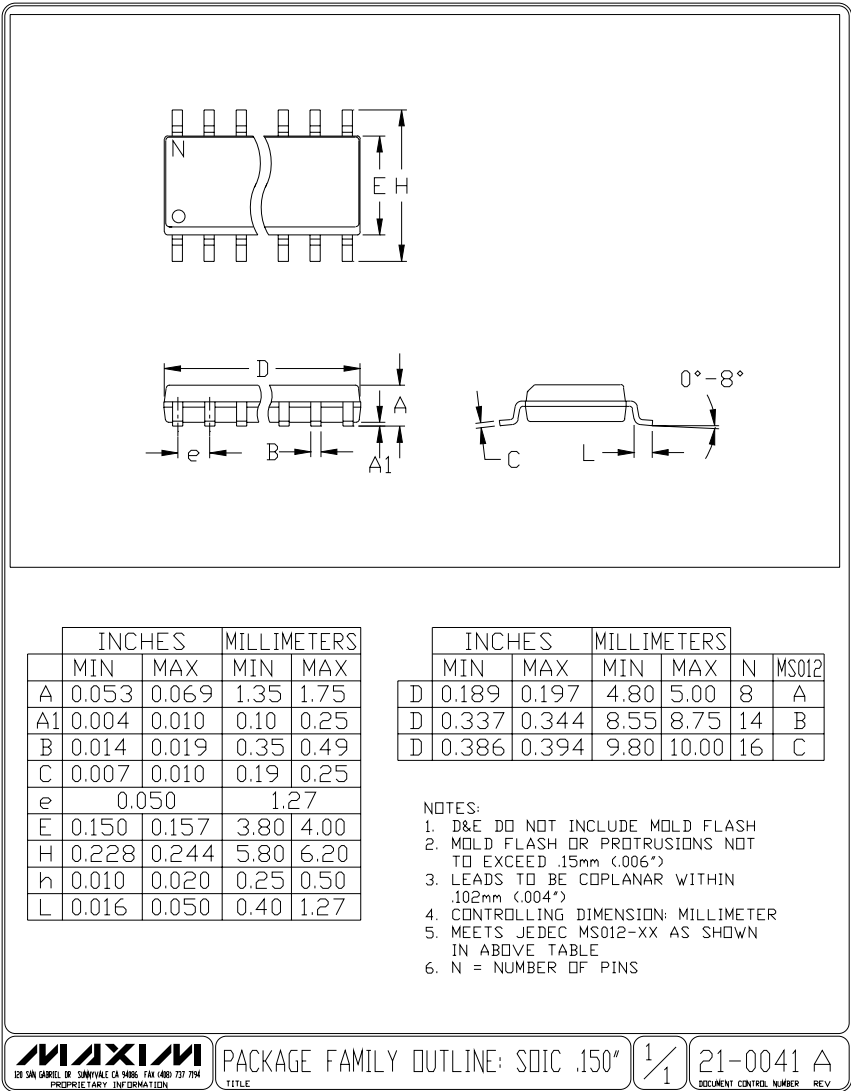


TSSOP, NO PADS/EP

MAX9121/MAX9122

# Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout

## Package Information (continued)



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