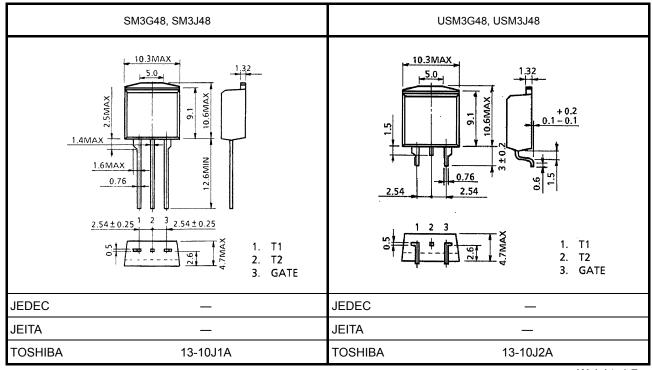
TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM3G48, USM3G48, SM3J48, USM3J48

AC POWER CONTROL APPLICATIONS

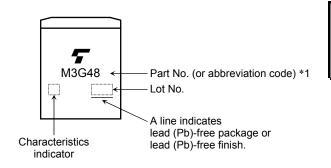
- Repetitive Peak Off-State Voltage: VDRM=400V, 600V
- R.M.S On-State Current: IT (RMS)=3A
- Gate Trigger Current: IGT=20mA Max.

Unit: mm



Weight: 1.7g

MARKING



*1	Part No. (or abbreviation code)	Part No.		
	M3G48	SM3G48, USM3G48		
	M3J48	SM3J48, USM3J48		



ABSOLUTE MAXIMUM RATINGS

CHARACTERIS	STIC	SYMBOL RATING		UNIT	
Repetitive Peak	(U)SM3G48	Vanu	400	V	
Off-State Voltage	(U)SM3J48	V _{DRM}	600	V	
R.M.S On-State Current	I _{T (RMS)}	3	Α		
Peak One Cycle Surge On-State Current (Non-Repetitive)		I _{TSM}	30 (50Hz)	Α	
		ISM	33 (60Hz)	_ ^	
I ² t Limit Value		l ² t	4.5	A ² s	
Critical Rate of Rise of C Current	n-State (Note 1)	di / dt	50	A / μs	
Peak Gate Power Dissip	ation	P _{GM}	5	W	
Average Gate Power Dis	ssipation	P _G (AV) 0.5		W	
Peak Forward Gate Volta	age	V_{GM}	м 10		
Peak Forward Gate Curr	ent	I _{GM}	:M 2		
Junction Temperature		Tj	-40~125	°C	
Storage Temperature Ra	ange	T _{stg}	-40~125	°C	

Note 1: V_{DRM}=0.5×Rated

I_{TM}≤4.5A

tgw≥10μs

tgr≤250ns

 $i_{gp}=I_{GT}\times 2.0$

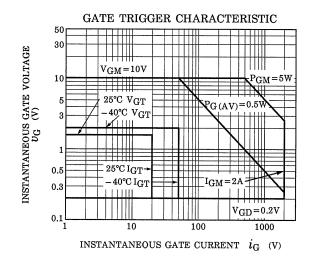
Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

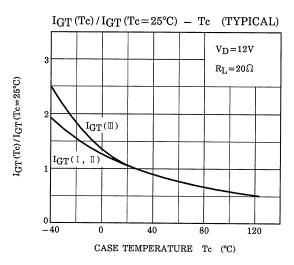
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

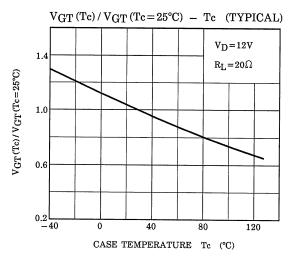
ELECTRICAL CHARACTERISTICS (Ta=25°C)

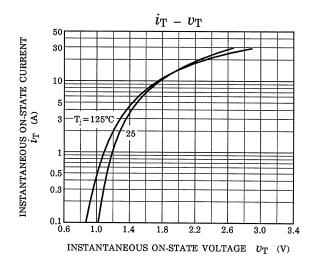
CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current		I _{DRM}	V _{DRM} =Rated		_	_	20	μА
	I	V _{GT}	V _D =12V R _L =20Ω	T2 (+), Gate (+)	_	_	1.5	V
Cata Trigger Voltage	II			T2 (+), Gate (-)	_	_	1.5	
Gate Trigger Voltage	III			T2 (-), Gate (-)	_	_	1.5	
	IV			T2 (-), Gate (+)	_	_	_	
	I	- I _{GT}	V _D =12V R _L =20Ω	T2 (+), Gate (+)	_	_	20	- mA
Gate Trigger Current	II			T2 (+), Gate (-)	_	_	20	
Gate migger Current	III			T2 (-), Gate (-)	_	_	20	
	IV			T2 (-), Gate (+)	_	_	_	
Peak On-State Voltage		V_{TM}	I _{TM} =4.5A		_	_	1.5	V
Gate Non-Trigger Voltage		V_{GD}	V _D =Rated, Tc=125°C		0.2	_	_	V
Holding Current		lн	V _D =12V, I _{TM} =1A		_	_	30	mA
Thermal Resistance		R _{th (j-c)}	Junction to Case, AC		_	_	3.6	°C / W
Critical Rate of Rise of Off-State Voltage		dv / dt	V _{DRM} =Rated, T _j =125°C Exponential Rise		_	300	_	V / μs
Critical Rate of Rise of Off-State Voltage at Commutation		(dv / dt) c	V _{DRM} =400V, T _j =125°C (di /dt) c=-2.0A / ms		10	_	_	V / μs

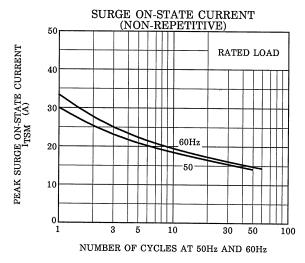
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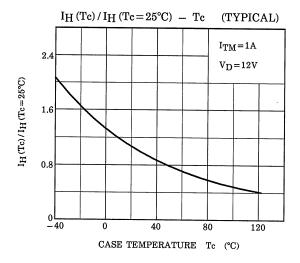


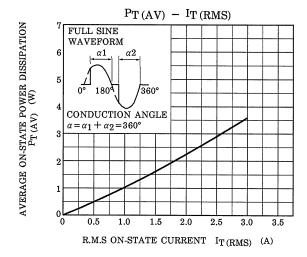


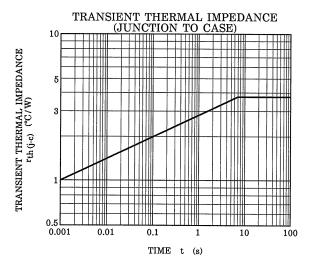


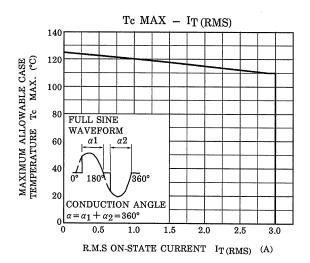


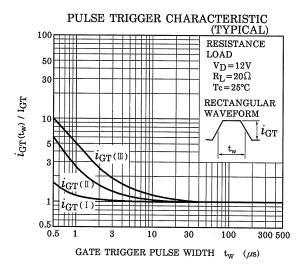












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