

74LVC16244A; 74LVCH16244A

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

Rev. 12 — 5 March 2012

Product data sheet

1. General description

The 74LVC16244A; 74LVCH16244A are 16-bit non-inverting buffer/line drivers with 3-state bus compatible outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. It features four output enable inputs, ($\overline{1OE}$ to $\overline{4OE}$) each controlling four of the 3-state outputs. A HIGH on \overline{nOE} causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH16244A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- All data inputs have bus hold. (74LVCH16244A only)
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

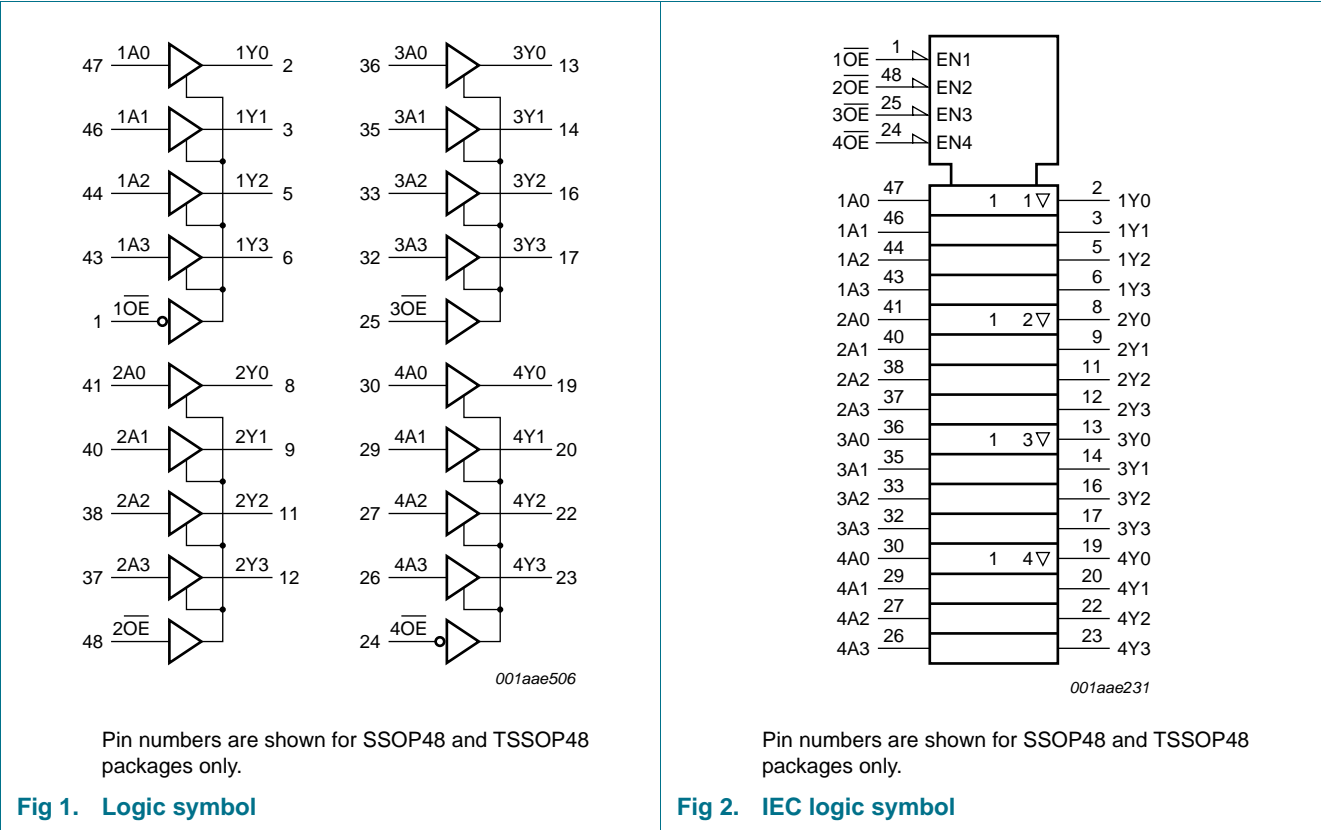


3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC16244ADL	−40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVCH16244ADL				
74LVC16244ADGG	−40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16244ADGG				
74LVC16244AEV	−40 °C to +125 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVCH16244AEV				
74LVC16244ABX	−40 °C to +125 °C	HXQFN60	plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 × 6 × 0.5 mm	SOT1134-2
74LVCH16244ABX				

4. Functional diagram



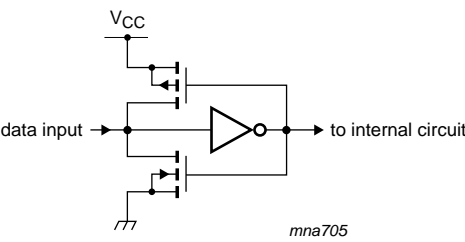


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning

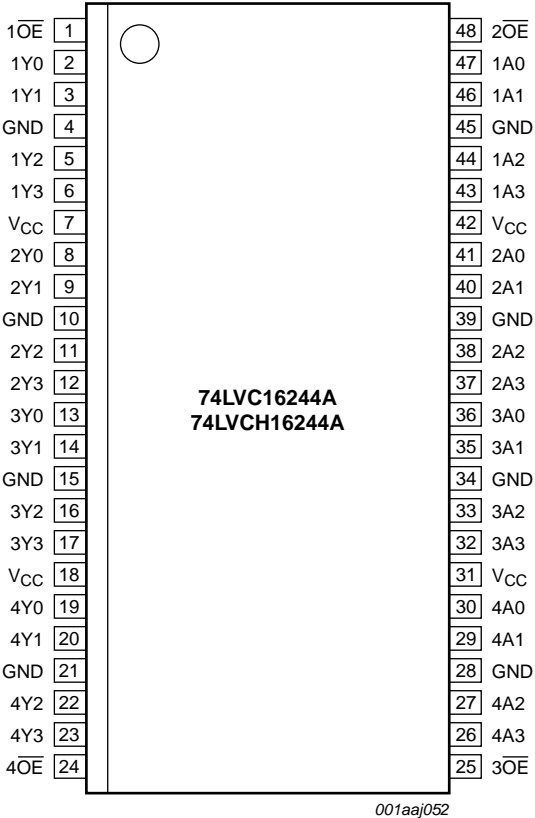


Fig 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

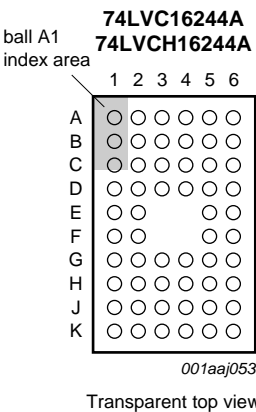
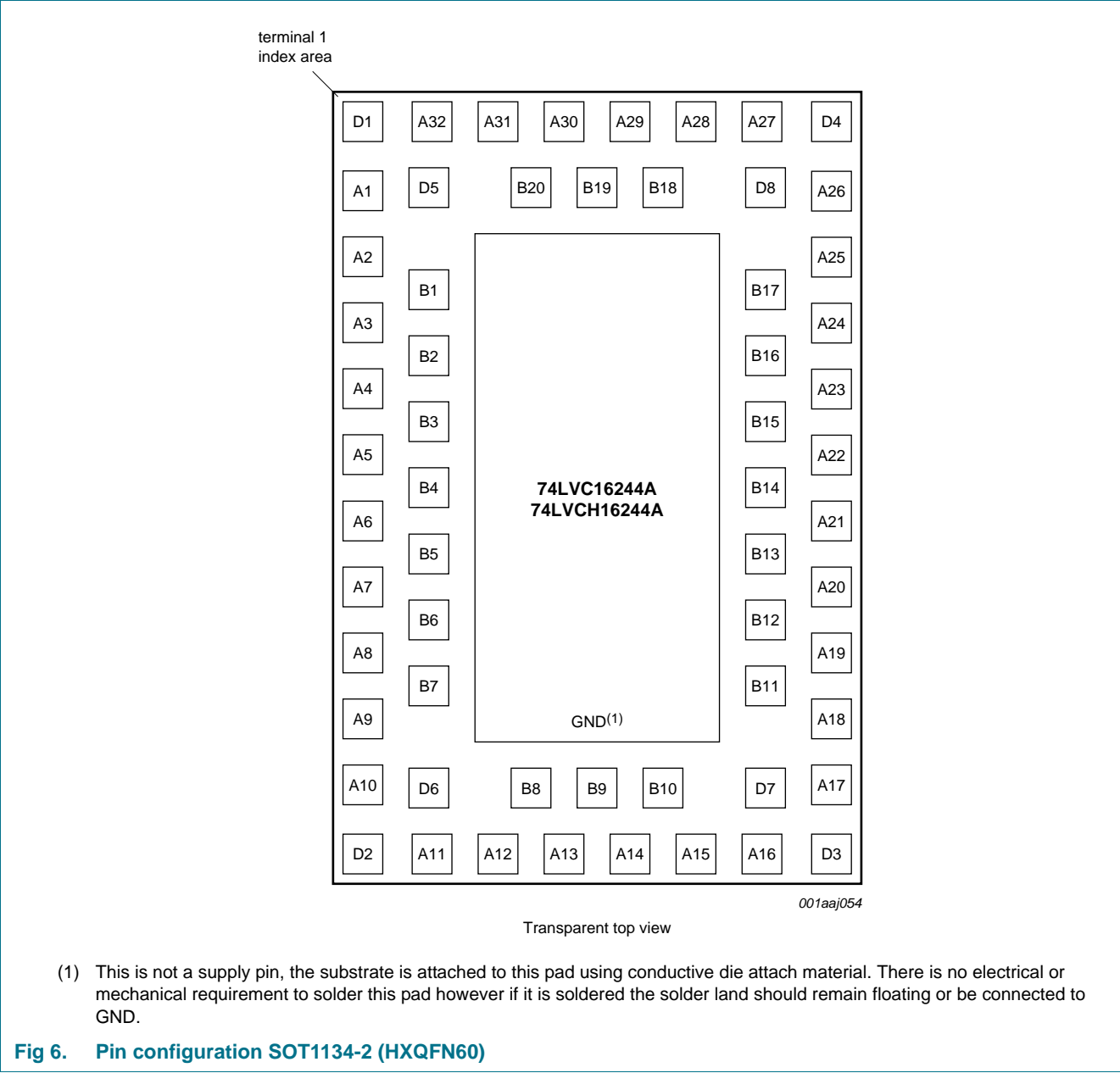


Fig 5. Pin configuration SOT702-1 (VFBGA56)



5.2 Pin description

Table 2. Pin description

Symbol	Pin			Description
	SOT370-1 and SOT362-1	SOT702-1	SOT1134-2	
$\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$, $\overline{4OE}$	1, 48, 25, 24	A1, A6, K6, K1	A30, A29, A14, A13	output enable input (active LOW)
1Y0 to 1Y3	2, 3, 5, 6	B2, B1, C2, C1	B20, A31, D5, D1	data output
2Y0 to 2Y3	8, 9, 11, 12	D2, D1, E2, E1	A2, B2, B3, A5	data output
3Y0 to 3Y3	13, 14, 16, 17	F1, F2, G1, G2	A6, B5, B6, A9	data output
4Y0 to 4Y3	19, 20, 22, 23	H1, H2, J1, J2	D2, D6, A12, B8	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	B3, B4, D3, D4, G3, G4, J3, J4	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V _{CC}	7, 18, 31, 42	C3, C4, H3, H4	A1, A10, A17, A26	supply voltage
1A0 to 1A3	47, 46, 44, 43	B5, B6, C5, C6	B18, A28, D8, D4	data input
2A0 to 2A3	41, 40, 38, 37	D5, D6, E5, E6	A25, B16, B15, A22	data input
3A0 to 3A3	36, 35, 33, 32	F6, F5, G6, G5	A21, B13, B12, A18	data input
4A0 to 4A3	30, 29, 27, 26	H6, H5, J6, J5	D3, D7, A15, B10	data input
n.c.	-	A2, A3, A4, A5, K2, K3, K4, K5	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

6. Functional description

Table 3. Function table^[1]

Control	Input	Output
\overline{nOE}	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	output HIGH or LOW	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C;			
		(T)SSOP48 package	[3] -	500	mW
		VFBGA56 package	[4] -	1000	mW
		HXQFN60 package	[4] -	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
		functional	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.2$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = –100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} – 0.2	-	-	V _{CC} – 0.3	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = –18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current ^[2]	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	-	±0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	20	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} – 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF
I _{BHL}	bus hold LOW current ^{[3][4]}	V _{CC} = 1.65; V _I = 0.58 V	10	-	-	10	-	µA
		V _{CC} = 2.3; V _I = 0.7 V	30	-	-	25	-	µA
		V _{CC} = 3.0; V _I = 0.8 V	75	-	-	60	-	µA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{BHH}	bus hold HIGH current ^{[3][4]}	V _{CC} = 1.65; V _I = 1.07 V	–10	-	-	–10	-	μA
		V _{CC} = 2.3; V _I = 1.7 V	–30	-	-	–25	-	μA
		V _{CC} = 3.0; V _I = 2.0 V	–75	-	-	–60	-	μA
I _{BHLO}	bus hold LOW overdrive current ^{[3][5]}	V _{CC} = 1.95 V	200	-	-	200	-	μA
		V _{CC} = 2.7 V	300	-	-	300	-	μA
		V _{CC} = 3.6 V	500	-	-	500	-	μA
I _{BHHO}	bus hold HIGH overdrive current ^{[3][5]}	V _{CC} = 1.95 V	–200	-	-	–200	-	μA
		V _{CC} = 2.7 V	–300	-	-	–300	-	μA
		V _{CC} = 3.6 V	–500	-	-	–500	-	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.

[3] Valid for data inputs only. Control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

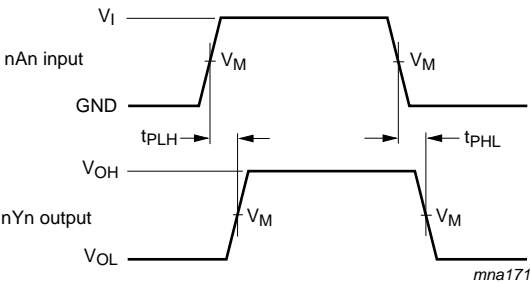
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[2]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nYn; see Figure 7 ^[1]						
		V _{CC} = 1.2 V	-	11.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	4.8	10.7	1.5	11.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.3	1.0	5.9	ns
		V _{CC} = 2.7 V	1.0	2.6	4.7	1.0	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	2.2	4.1	1.1	5.5	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nYn; see Figure 8 ^[1]						
		V _{CC} = 1.2 V	-	15.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.2	12.1	1.5	12.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.5	6.4	1.0	7.1	ns
		V _{CC} = 2.7 V	1.0	3.3	5.8	1.0	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.8	4.6	1.0	6.0	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nYn; see Figure 8 ^[1]						
		V _{CC} = 1.2 V	-	10.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.4	8.7	2.5	9.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.4	4.9	1.0	5.3	ns
		V _{CC} = 2.7 V	1.0	3.2	6.2	1.0	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	3.1	5.2	1.8	6.5	ns

Table 7. Dynamic characteristics ...continued
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[2]	Max	Min	Max	
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC}						
		V _{CC} = 1.65 V to 1.95 V	-	4.8	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	8.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

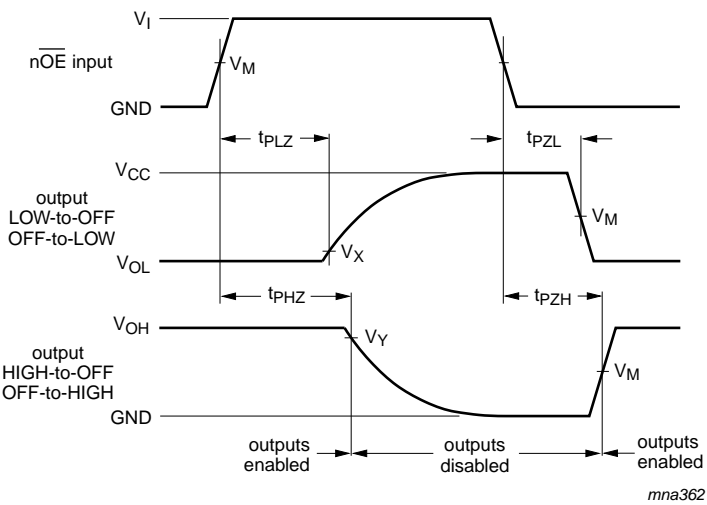
- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11. Waveforms



Measurement points are given in Table 8.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The input (nAn) to output (nYn) propagation delays

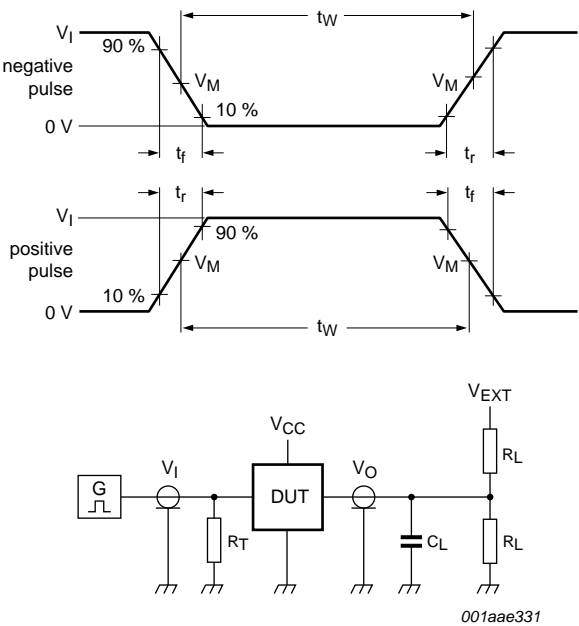


Measurement points are given in [Table 8](#).
Logic levels: VOL and VOH are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times.

Table 8. Measurement points

Supply voltage	VM	Input			
VCC		VI	tr = tf	Vx	Vy
1.2 V	0.5 × VCC	VCC	≤ 2.5 ns	VOL + 0.15 V	VOH – 0.15 V
1.65 V to 1.95 V	0.5 × VCC	VCC	≤ 2.5 ns	VOL + 0.15 V	VOH – 0.15 V
2.3 V to 2.7 V	0.5 × VCC	VCC	≤ 2.5 ns	VOL + 0.15 V	VOH – 0.15 V
2.7 V	1.5 V	2.7 V	≤ 2.5 ns	VOL + 0.3 V	VOH – 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns	VOL + 0.3 V	VOH – 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1

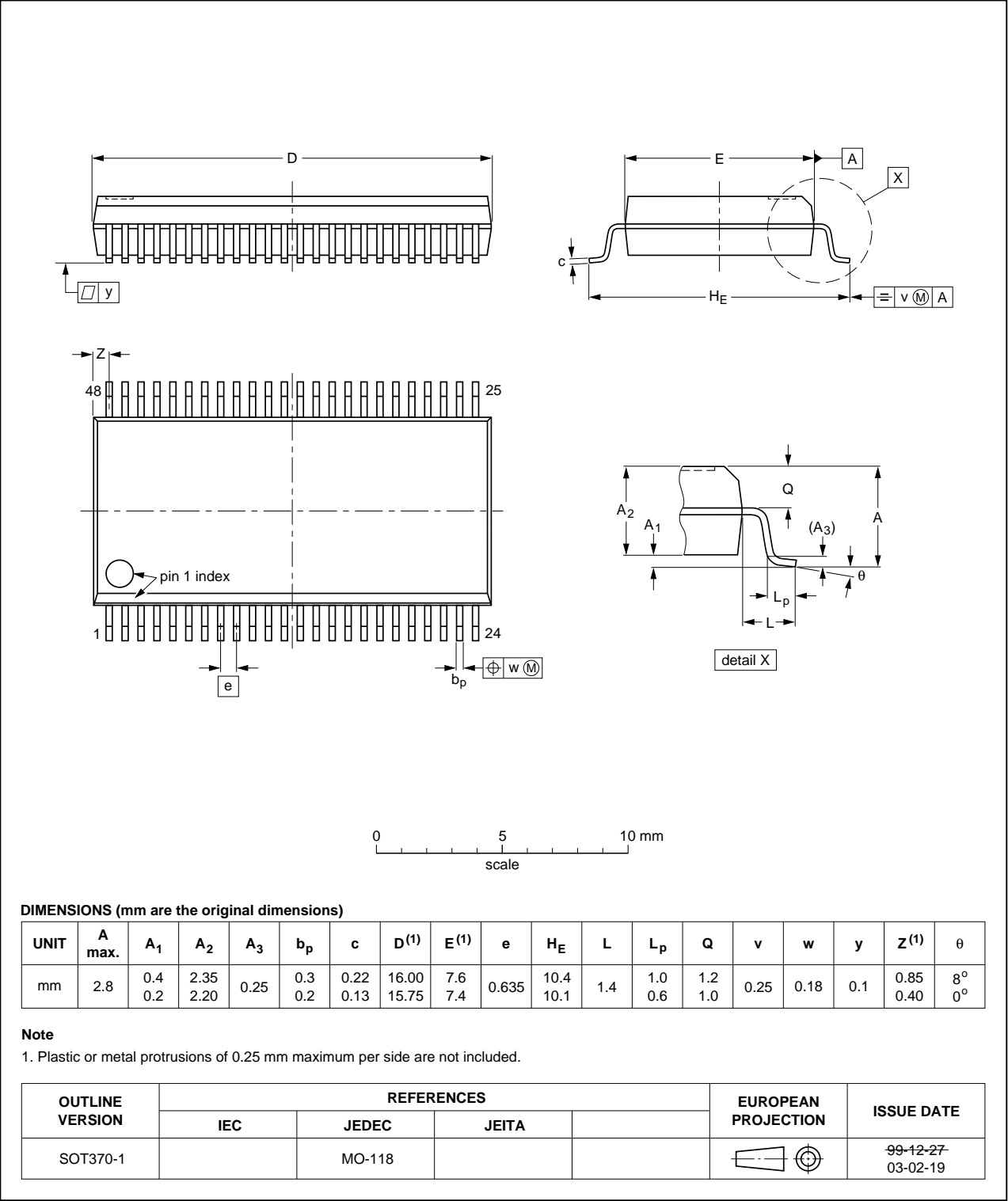
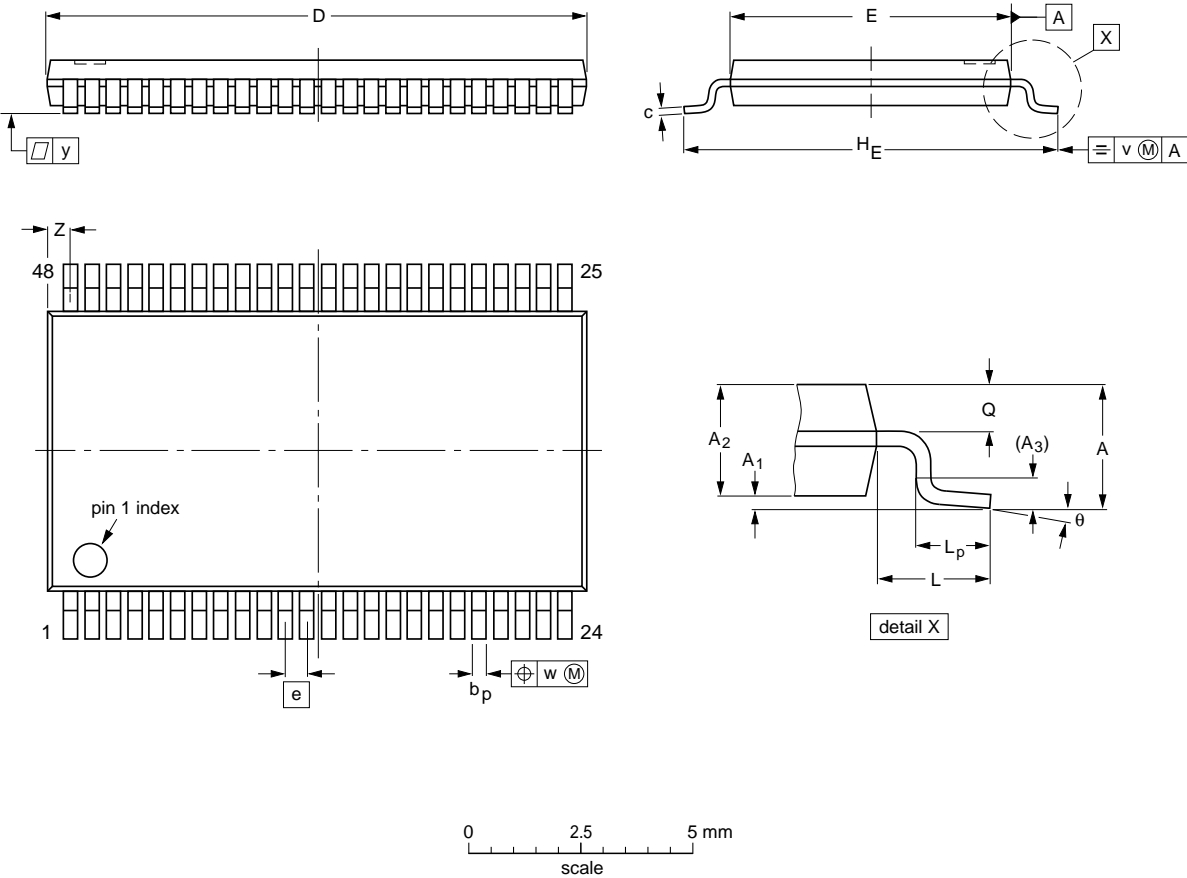


Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

- Notes**
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				99-12-27 03-02-19

Fig 11. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

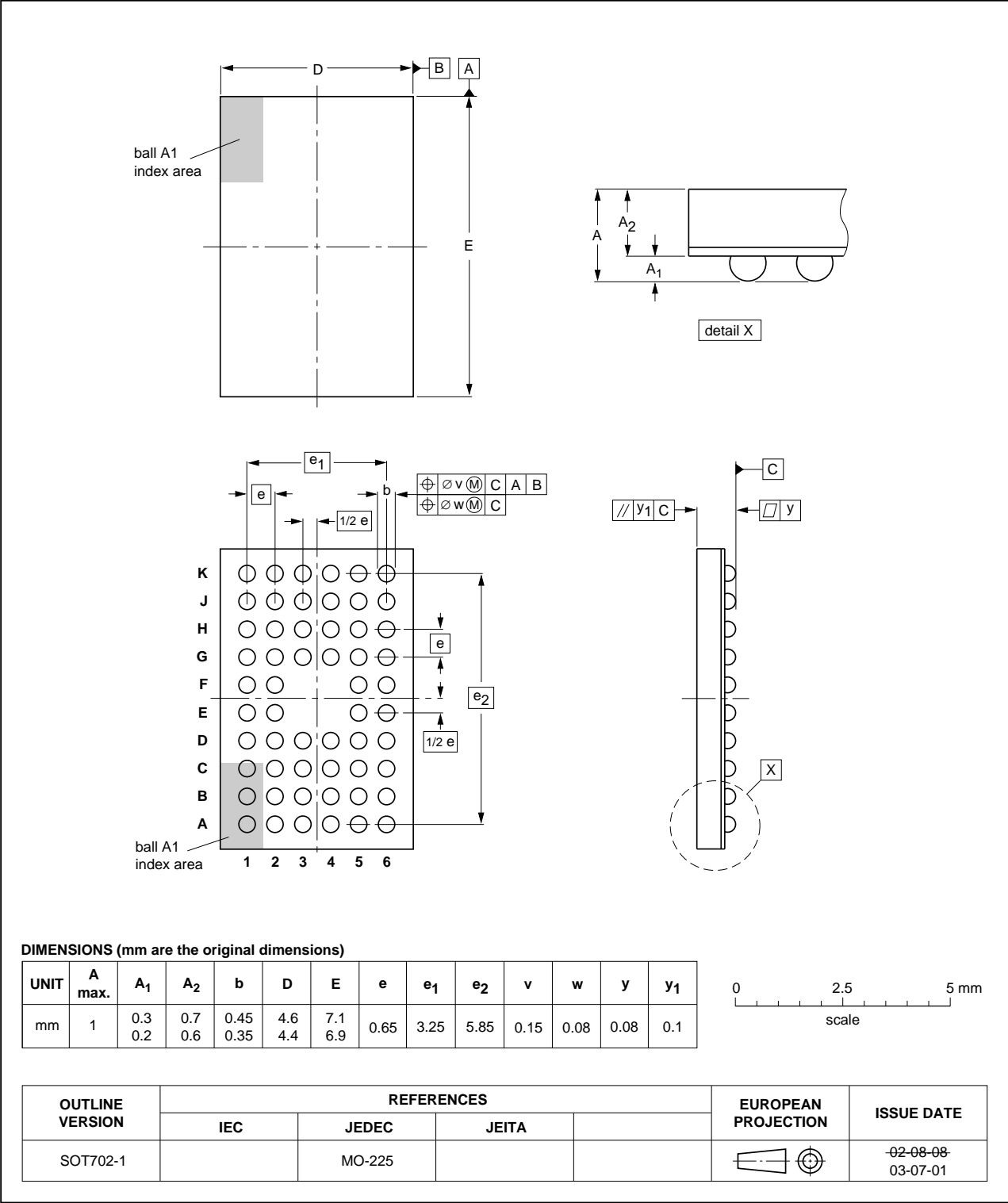


Fig 12. Package outline SOT702-1 (VFBGA56)

HXQFN60: plastic compatible thermal enhanced extremely thin quad flat package; no leads;
 60 terminals; body 4 x 6 x 0.5 mm

SOT1134-2

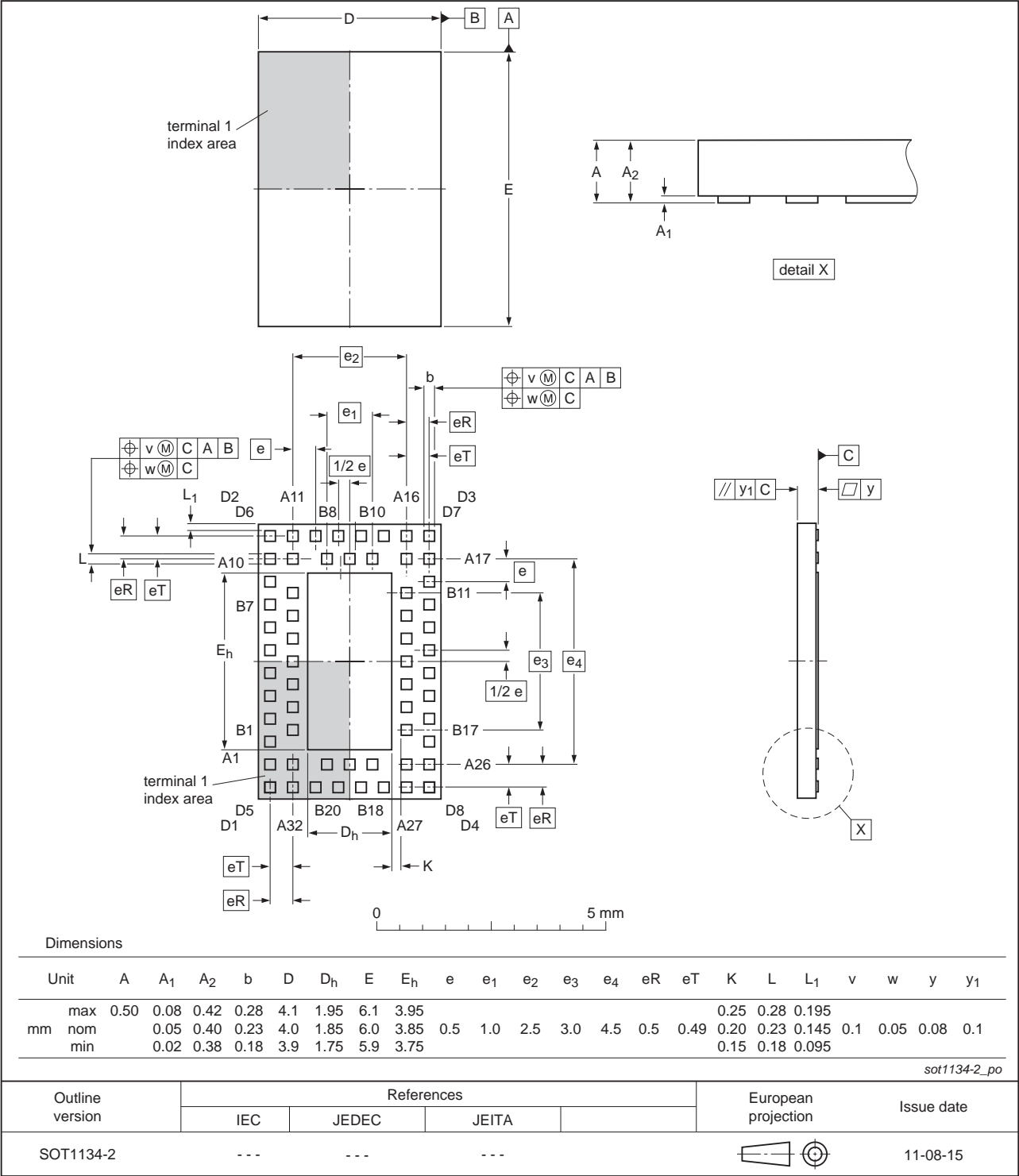


Fig 13. Package outline SOT1134-2 (HXQFN60)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16244A v.12	20120305	Product data sheet	-	74LVC_LVCH16244A v.11
Modifications:	<ul style="list-style-type: none"> For type number 74LVC16244ABX and 74LVCH16244ABX the sot code has changed to SOT1134-2. 			
74LVC_LVCH16244A v.11	20111027	Product data sheet	-	74LVC_LVCH16244A v.10
Modifications:	<ul style="list-style-type: none"> Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. 			
74LVC_LVCH16244A v.10	20110429	Product data sheet	-	74LVC_LVCH16244A v.9
Modifications:	<ul style="list-style-type: none"> type numbers 74LVC16244ABQ and 74LVCH16244ABQ changed to 74LVC16244ABX and 74LVCH16244ABX. Figure 6: figure note 1 changed. 			
74LVC_LVCH16244A v.9	20100318	Product data sheet	-	74LVC_LVCH16244A v.8
74LVC_LVCH16244A v.8	20081117	Product data sheet	-	74LVC_LVCH16244A v.7
74LVC_LVCH16244A v.7	20031208	Product specification	-	74LVC_LVCH16244A v.6
74LVC_LVCH16244A v.6	20030130	Product specification	-	74LVC_LVCH16244A v.5
74LVC_LVCH16244A v.5	20021030	Product specification	-	74LVC_H16244A v.4
74LVC_H16244A v.4	19971028	Product specification	-	74LVC16244A_74LVCH16244A v.3
74LVC16244A_74LVCH16244A v.3	19971028	Product specification	-	74LVC16244A v.2
74LVC16244A v.2	19970630	Product specification	-	74LVC16244A v.1
74LVC16244A v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	5
6	Functional description	5
7	Limiting values	6
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	8
11	Waveforms	9
12	Package outline	12
13	Abbreviations	16
14	Revision history	16
15	Legal information	17
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	18
16	Contact information	18
17	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 5 March 2012

Document identifier: 74LVC_LVCH16244A

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[74LVC16244ADG](#) [74LVC16244ADL](#) [74LVC16244ADL-T](#) [74LVC16244AEV](#) [74LVC16244AEV-S](#) [74LVC16244AEV-T](#)
[74LVCH16244ADG](#) [74LVCH16244ADG-T](#) [74LVCH16244ADL](#) [74LVCH16244ADL-T](#) [74LVCH16244AEV](#)
[74LVCH16244AEV-S](#) [74LVCH16244AEV-T](#) [74LVCH16244AEV/G;5](#) [74LVC16244ADGG,112](#) [74LVC16244ADGG,118](#)
[74LVCH16244ADGG,11](#) [74LVCH16244ADGG:11](#) [74LVCH16244ABX,518](#) [74LVC16244ABX,518](#)
[74LVC16244ADGG,512](#) [74LVC16244ADGG,518](#) [74LVC16244ADL,112](#) [74LVC16244ADL,118](#) [74LVC16244AEV,157](#)
[74LVC16244AEV/G,55](#) [74LVC16244AEV/G:55](#) [74LVC16244AEV/G,51](#) [74LVC16244AEV,151](#) [74LVC16244AEV,118](#)
[74LVCH16244ADGG,51](#) [74LVCH16244ADGG:51](#) [74LVCH16244ADL,112](#) [74LVCH16244ADL,118](#)
[74LVCH16244AEV,157](#) [74LVCH16244AEV/G:5](#) [74LVCH16244AEV/G,5](#) [74LVCH16244AEV,518](#)
[74LVCH16244AEV,151](#) [74LVCH16244AEV,118](#) [74LVC16244ABQ,518](#) [74LVC16245ABQ,518](#)
[74LVCH16244ABQ,518](#)