

**Parallel Optical Link:  
PAROLI® Tx AC, 1.6 Gbit/s**

**V23814-U1306-M136**

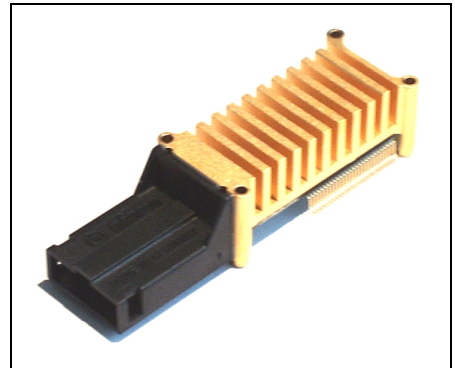
**Parallel Optical Link:  
PAROLI® Rx AC, 1.6 Gbit/s**

**V23815-U1306-M136**

### **Preliminary**

#### **Features**

- Power supply 3.3 V
- Multistandard differential signal electrical interface
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Transmission data rate of up to 1600 Mbit/s per channel, total link data rate up to 19 Gbit/s
- 850 nm VCSEL array technology
- PIN diode array technology
- 62.5 µm graded index multimode fiber ribbon
- MT based optical port
- SMD technology
- IEC Class 1M laser safety compliant
- GBE mask compliant modules available



#### **Optical Port**

- Designed for the Simplex MT Connector (SMC)
- Port outside dimensions: 15.4 mm x 6.8 mm (width x height)
- MT compatible (IEC 61754-5) fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Alignment pins fixed in module port
- Integrated mechanical keying
- Process plug (SMC dimensions) included with every module

**Features of the Simplex MT Connector (SMC)**

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule (IEC 61754-5)
- MT compatible fiber spacing (250  $\mu\text{m}$ ) and alignment pin spacing (4600  $\mu\text{m}$ )
- Snap-in mechanism
- Ferrule bearing spring loaded
- Integrated mechanical keying

**Applications**

Telecommunication

- Switching equipment
- Access network

Data Communication

- Interframe (rack-to-rack)
- Intraframe (board-to-board)
- On board (optical backplane)

## Pin Configuration

The numbering conventions for the Tx and Rx modules are the same.

## Numbering Conventions Transmitter/Receiver

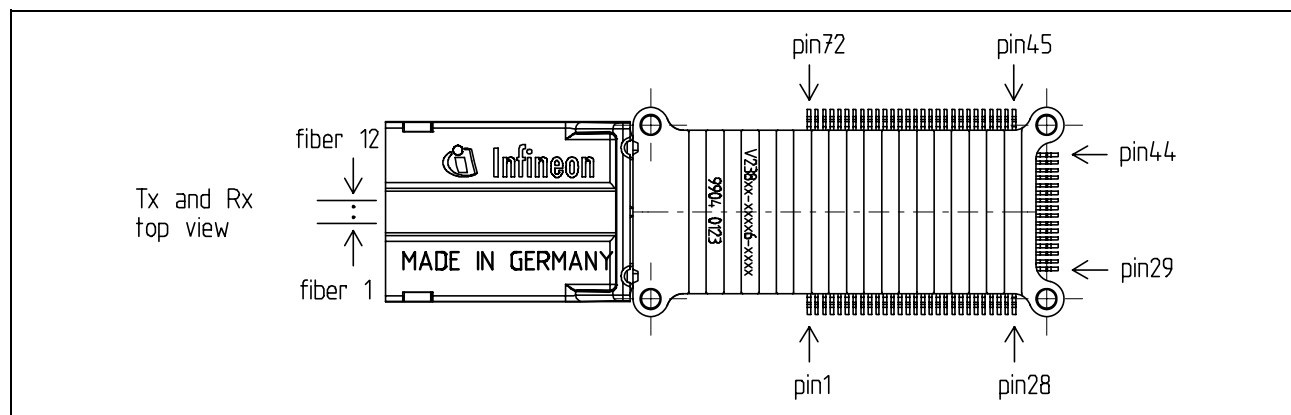


Figure 1

## Pin Description Transmitter

Pin No.	Symbol	Level/Logic	Description
1	$V_{CC}$		Power supply voltage of laser driver
2	t.b.l.o.		to be left open
3	t.b.l.o.		to be left open
4	t.b.l.o.		to be left open
5	t.b.l.o.		to be left open
6	LCU	LVC MOS Out	Laser Controller Up. High = normal operation. Low = laser fault or –RESET low.
7	$V_{EE}$		Ground
8	$V_{IN}$		Input $V_{IN}$ rail. CML: $V_{IN}$ = Reference supply (e.g. $V_{CC}$ ). LVPECL, LVDS: $V_{IN} = V_{EE}$ .
9	t.b.l.o.		to be left open
10	t.b.l.o.		to be left open
11	$V_{EE}$		Ground
12	$V_{EE}$		Ground

**Pin Configuration**
**Pin Description Transmitter (cont'd)**

<b>Pin No.</b>	<b>Symbol</b>	<b>Level/Logic</b>	<b>Description</b>
13	DI01N	Data In	Data Input #1, inverted
14	DI01P	Data In	Data Input #1, non-inverted
15	$V_{EE}$		Ground
16	$V_{EE}$		Ground
17	DI02N	Data In	Data Input #2, inverted
18	DI02P	Data In	Data Input #2, non-inverted
19	$V_{EE}$		Ground
20	$V_{EE}$		Ground
21	DI03N	Data In	Data Input #3, inverted
22	DI03P	Data In	Data Input #3, non-inverted
23	$V_{EE}$		Ground
24	$V_{EE}$		Ground
25	t.b.l.o.		to be left open
26	DI04N	Data In	Data Input #4, inverted
27	DI04P	Data In	Data Input #4, non-inverted
28	$V_{EE}$		Ground
29	DI05N	Data In	Data Input #5, inverted
30	DI05P	Data In	Data Input #5, non-inverted
31	$V_{EE}$		Ground
32	$V_{EE}$		Ground
33	DI06N	Data In	Data Input #6, inverted
34	DI06P	Data In	Data Input #6, non-inverted
35	$V_{EE}$		Ground
36	$V_{EE}$		Ground
37	DI07N	Data In	Data Input #7, inverted
38	DI07P	Data In	Data Input #7, non-inverted
39	$V_{EE}$		Ground
40	$V_{EE}$		Ground
41	DI08N	Data In	Data Input #8, inverted
42	DI08P	Data In	Data Input #8, non-inverted

**Pin Description Transmitter (cont'd)**

Pin No.	Symbol	Level/Logic	Description
43	$V_{EE}$		Ground
44	$V_{EE}$		Ground
45	$V_{EE}$		Ground
46	DI09N	Data In	Data Input #9, inverted
47	DI09P	Data In	Data Input #9, non-inverted
48	t.b.l.o.		to be left open
49	$V_{EE}$		Ground
50	$V_{EE}$		Ground
51	DI10N	Data In	Data Input #10, inverted
52	DI10P	Data In	Data Input #10, non-inverted
53	$V_{EE}$		Ground
54	$V_{EE}$		Ground
55	DI11N	Data In	Data Input #11, inverted
56	DI11P	Data In	Data Input #11, non-inverted
57	$V_{EE}$		Ground
58	$V_{EE}$		Ground
59	DI12N	Data In	Data Input #12, inverted
60	DI12P	Data In	Data Input #12, non-inverted
61	$V_{EE}$		Ground
62	$V_{IN}$		Input $V_{IN}$ rail. CML: $V_{IN}$ = Reference supply (e.g. $V_{CC}$ ). LVPECL, LVDS: $V_{IN}$ = $V_{EE}$ .
63	t.b.l.o.		to be left open
64	–RESET	LVC MOS In	High = laser diode array is active. Low = switches laser diode array off. This input has an internal pull-down to ensure laser safety switch off in case of unconnected –RESET input.
65	$V_{EE}$		Ground
66	$V_{EE}$		Ground

## Pin Configuration

### Pin Description Transmitter (cont'd)

Pin No.	Symbol	Level/Logic	Description
67	LE	LVC MOS In	Laser ENABLE. High active. High = laser array is on if –LE is also active. Low = laser array is off. This input has an internal pull-up, therefore can be left open.
68	–LE		Laser ENABLE. Low active. Low = laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.
69	t.b.l.o.		to be left open
70	t.b.l.o.		to be left open
71	t.b.l.o.		to be left open
72	V <sub>CC</sub>		Power supply voltage of laser driver

**Pin Description Receiver**

Pin No.	Symbol	Level/Logic	Description
1	$V_{EE}$		Ground
2	$V_{CC}$		Power supply voltage of preamplifier and analog circuitry
3	$V_{CC}$		Power supply voltage of preamplifier and analog circuitry
4	t.b.l.o.		to be left open
5	OEN	LVC MOS In	Output Enable. High = normal operation. Low = sets all Data Outputs to low. This input has an internal pull-up which pulls to high level when this input is left open.
6	SD1	LVC MOS Out	Signal Detect on fiber #1. High = signal of sufficient AC power is present on fiber #1. Low = signal on fiber #1 is insufficient.
7	$V_{CCO}$		Power supply voltage of output stages
8	$V_{EE}$		Ground
9	t.b.l.o.		to be left open
10	$V_{EE}$		Ground
11	$V_{EE}$		Ground
12	$V_{EE}$		Ground
13	DO01P	LVDS Out	Data Output #1, non-inverted
14	DO01N	LVDS Out	Data Output #1, inverted
15	$V_{EE}$		Ground
16	$V_{EE}$		Ground
17	DO02P	LVDS Out	Data Output #2, non-inverted
18	DO02N	LVDS Out	Data Output #2, inverted
19	$V_{EE}$		Ground
20	$V_{EE}$		Ground
21	DO03P	LVDS Out	Data Output #3, non-inverted
22	DO03N	LVDS Out	Data Output #3, inverted
23	$V_{EE}$		Ground

**Pin Configuration**
**Pin Description Receiver (cont'd)**

<b>Pin No.</b>	<b>Symbol</b>	<b>Level/Logic</b>	<b>Description</b>
24	$V_{EE}$		Ground
25	t.b.l.o.		to be left open
26	DO04P	LVDS Out	Data Output #4, non-inverted
27	DO04N	LVDS Out	Data Output #4, inverted
28	$V_{EE}$		Ground
29	DO05P	LVDS Out	Data Output #5, non-inverted
30	DO05N	LVDS Out	Data Output #5, inverted
31	$V_{EE}$		Ground
32	$V_{EE}$		Ground
33	DO06P	LVDS Out	Data Output #6, non-inverted
34	DO06N	LVDS Out	Data Output #6, inverted
35	$V_{EE}$		Ground
36	$V_{EE}$		Ground
37	DO07P	LVDS Out	Data Output #7, non-inverted
38	DO07N	LVDS Out	Data Output #7, inverted
39	$V_{EE}$		Ground
40	$V_{EE}$		Ground
41	DO08P	LVDS Out	Data Output #8, non-inverted
42	DO08N	LVDS Out	Data Output #8, inverted
43	$V_{EE}$		Ground
44	$V_{EE}$		Ground
45	$V_{EE}$		Ground
46	DO09P	LVDS Out	Data Output #9, non-inverted
47	DO09N	LVDS Out	Data Output #9, inverted
48	t.b.l.o.		to be left open
49	$V_{EE}$		Ground
50	$V_{EE}$		Ground
51	DO10P	LVDS Out	Data Output #10, non-inverted
52	DO10N	LVDS Out	Data Output #10, inverted
53	$V_{EE}$		Ground



**Pin Description Receiver (cont'd)**

Pin No.	Symbol	Level/Logic	Description
54	$V_{EE}$		Ground
55	DO11P	LVDS Out	Data Output #11, non-inverted
56	DO11N	LVDS Out	Data Output #11, inverted
57	$V_{EE}$		Ground
58	$V_{EE}$		Ground
59	DO12P	LVDS Out	Data Output #12, non-inverted
60	DO12N	LVDS Out	Data Output #12, inverted
61	$V_{EE}$		Ground
62	$V_{EE}$		Ground
63	$V_{EE}$		Ground
64	t.b.l.o.		to be left open
65	$V_{EE}$		Ground
66	$V_{CCO}$		Power supply voltage of output stages
67	-SD12	LVC MOS Out low active	Signal Detect on fiber #12. Low = signal of sufficient AC power is present on fiber #12. High = signal on fiber #12 is insufficient.
68	ENSD	LVC MOS In	Enable Signal Detect. High = SD1 and SD12 function enabled. Low = SD1 and SD12 are set to permanent active. This input has an internal pull-up which pulls to high level when this input is left open.
69	t.b.l.o.		to be left open
70	$V_{CC}$		Power supply voltage of preamplifier and analog circuitry
71	$V_{CC}$		Power supply voltage of preamplifier and analog circuitry
72	$V_{EE}$		Ground

## Description

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module. The transmitter supports LVDS, CML and LVPECL differential signals. The receiver module is described for the LVDS electrical output only. A specification for Infineon's adjustable CML output can be provided separately.

### Transmitter V23814-U1306-M136

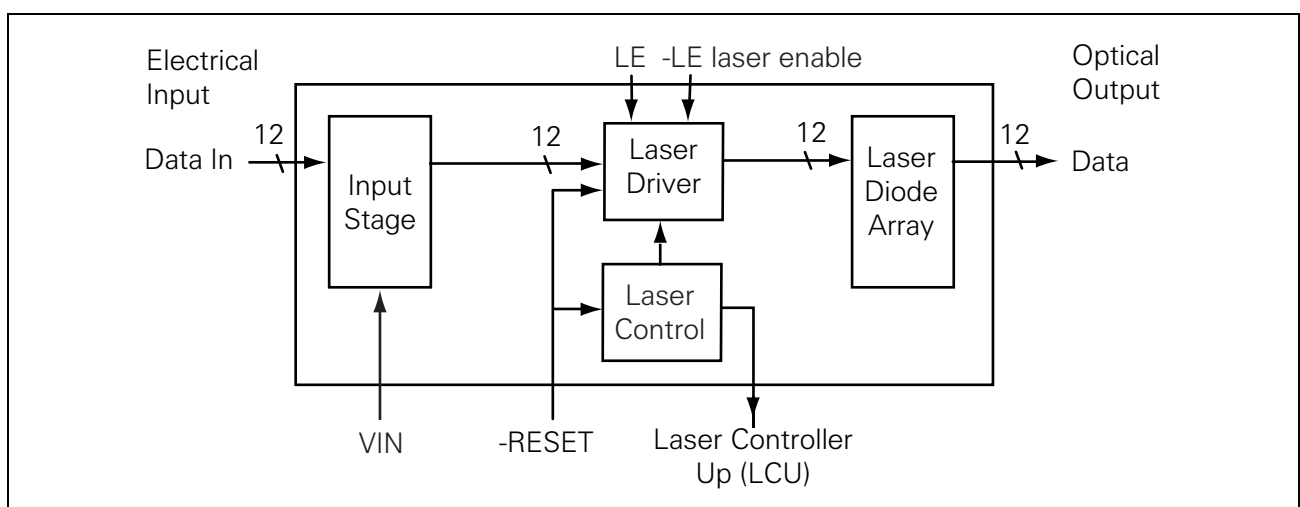
The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible; they also support LVPECL and CML because of the wide common input range). The electrical interface (LVDS, LVPECL or CML) is selected by the supply inputs  $V_{IN}$ . The data rate is up to 1600 Mbit/s for each channel. The transmitter module's min. data rate of 500 Mbit/s is specified for the CID<sup>1)</sup> worst case pattern (disparity 72) or any pattern with a lower disparity.

A logic low level at  $\text{-RESET}$  switches all laser outputs off. During power-up  $\text{-RESET}$  must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3.135 V level.

The Laser Controller Up (LCU) output is low if a laser fault is detected or  $\text{-RESET}$  is forced to low.

All non data signals have LVCMOS levels.

Transmission delay of the PAROLI system is  $\leq 1$  ns for the transmitter,  $\leq 1$  ns for the receiver and approximately 5 ns per meter for the fiber optic cable.



**Figure 2 Transmitter Block Diagram**

<sup>1)</sup> Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

### Receiver V23815-U1306-M136

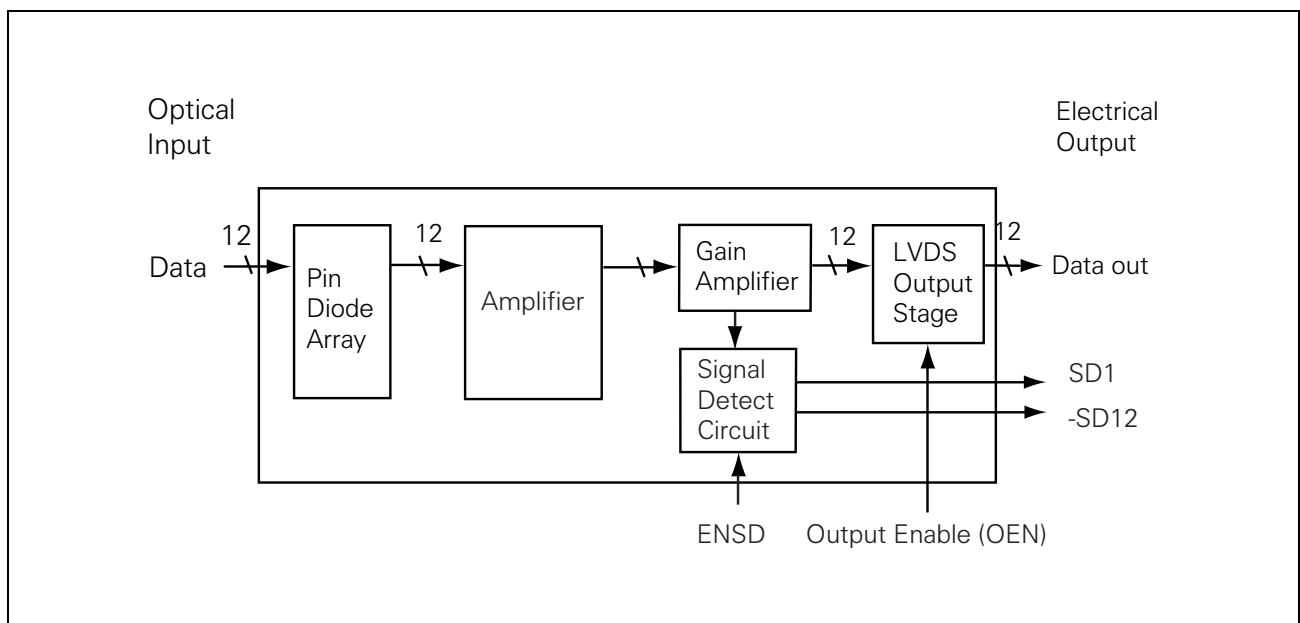
The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, transimpedance amplifiers, and gain amplifiers. There are two different modules available for LVDS and Infineon's adjustable CML output. This description only refers to a module with LVDS output. A module description for CML output can be provided separately.

The data rate is up to 1600 Mbit/s for each channel. The receiver module's min. data rate of 500 Mbit/s is specified for the CID<sup>1)</sup> worst case pattern (disparity 72) or any pattern with a lower disparity.

Additional Signal Detect outputs (SD1 active high / SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at LVDS Output Enable (OEN) sets all data outputs to logic low. SD outputs will not be effected.

All non data signals have LVCMOS levels. Transmission delay of the PAROLI system is at a maximum 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.



**Figure 3 Receiver Block Diagram**

<sup>1)</sup> Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

## Laser Safety

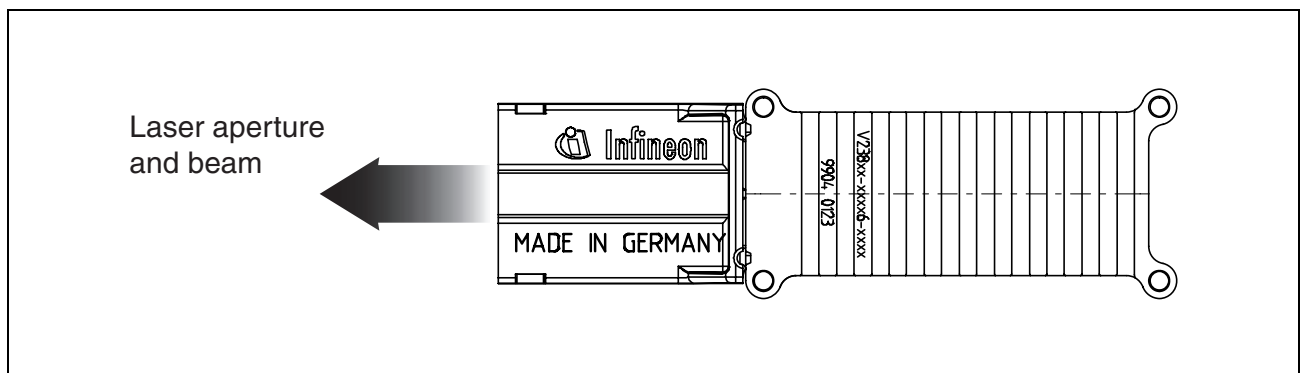
The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an IEC 60825-1 Amend. 2 Class 1M laser product. It complies with FDA performance standards (21 CFR 1040.10 and 1040.11) for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (the supply voltage range can be adjusted between 3.0 V and 3.6 V) under any circumstances to ensure laser safety.

### Class 1M Laser Product

**Attention: Invisible laser radiation. Do not view directly with optical instruments.**

*Note: Any modification of the module will be considered an act of “manufacturing”, and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).*



**Figure 4 Laser Emission**

## Laser Safety Design Considerations

To ensure laser safety for all input data patterns each channel is controlled internally and will be switched off if the laser safety limits are exceeded.

A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57%. The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.

The minimum alerter response time is 1  $\mu$ s with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1  $\mu$ s, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.

All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

## Technical Data

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

## Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply Voltage	$V_{CC}-V_{EE}$	-0.3	4.5	V
Data/Control Input Levels <sup>1)</sup>	$V_{IN}$	-0.5	$V_{CC}+0.5$	V
Data Input Differential Voltage <sup>2)</sup>	$ V_{ID} $		2.0	V
Operating Case Temperature <sup>3)</sup>	$T_{CASE}$	0	80	°C
Storage Ambient Temperature	$T_{STG}$	-20	100	°C
Operating Moisture		20	85	%
Storage Moisture		20	85	%
ESD Resistance (all pins to $V_{EE}$ , human body model) <sup>4)</sup>			1	kV

<sup>1)</sup> At Data and LVCMOS inputs.

<sup>2)</sup>  $|V_{ID}| = |(\text{input voltage of non-inverted input minus input voltage of inverted input})|$ .

<sup>3)</sup> Measured at case temperature reference point (see Package Outlines **Figure 15**).

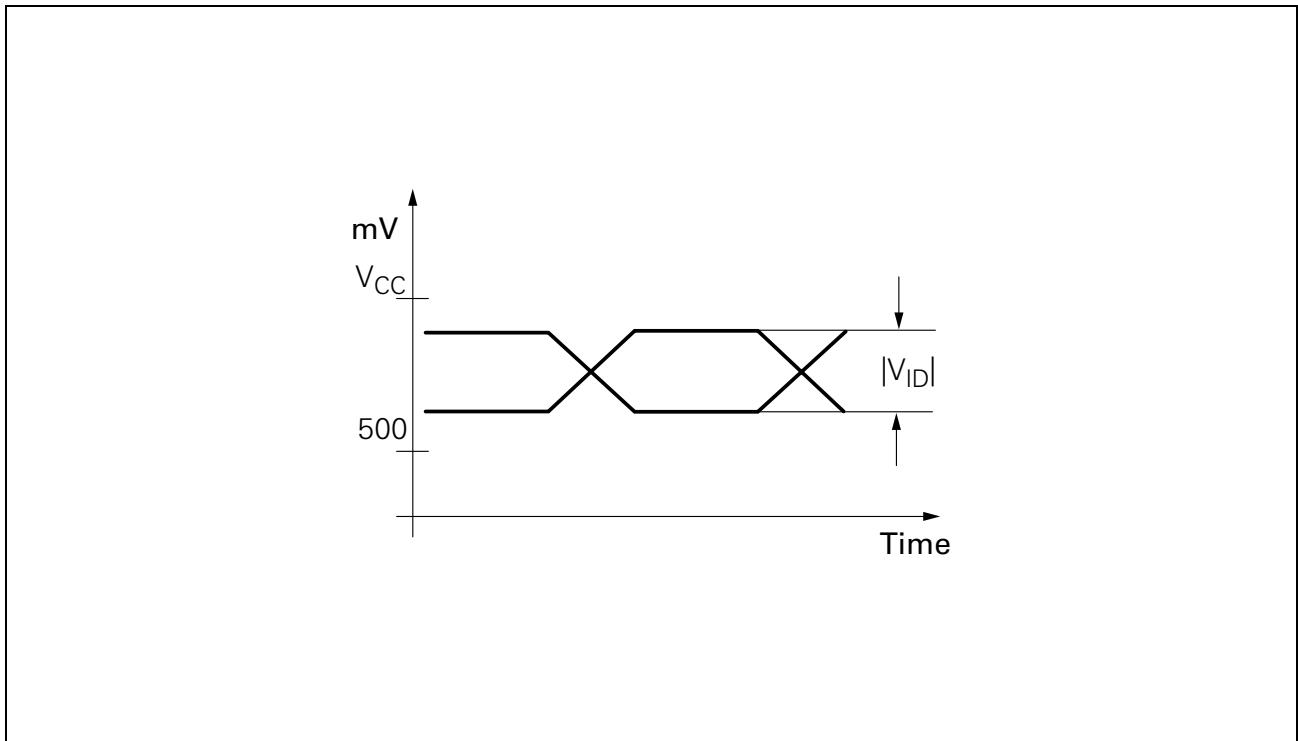
<sup>4)</sup> To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

**Recommended Operating Conditions**

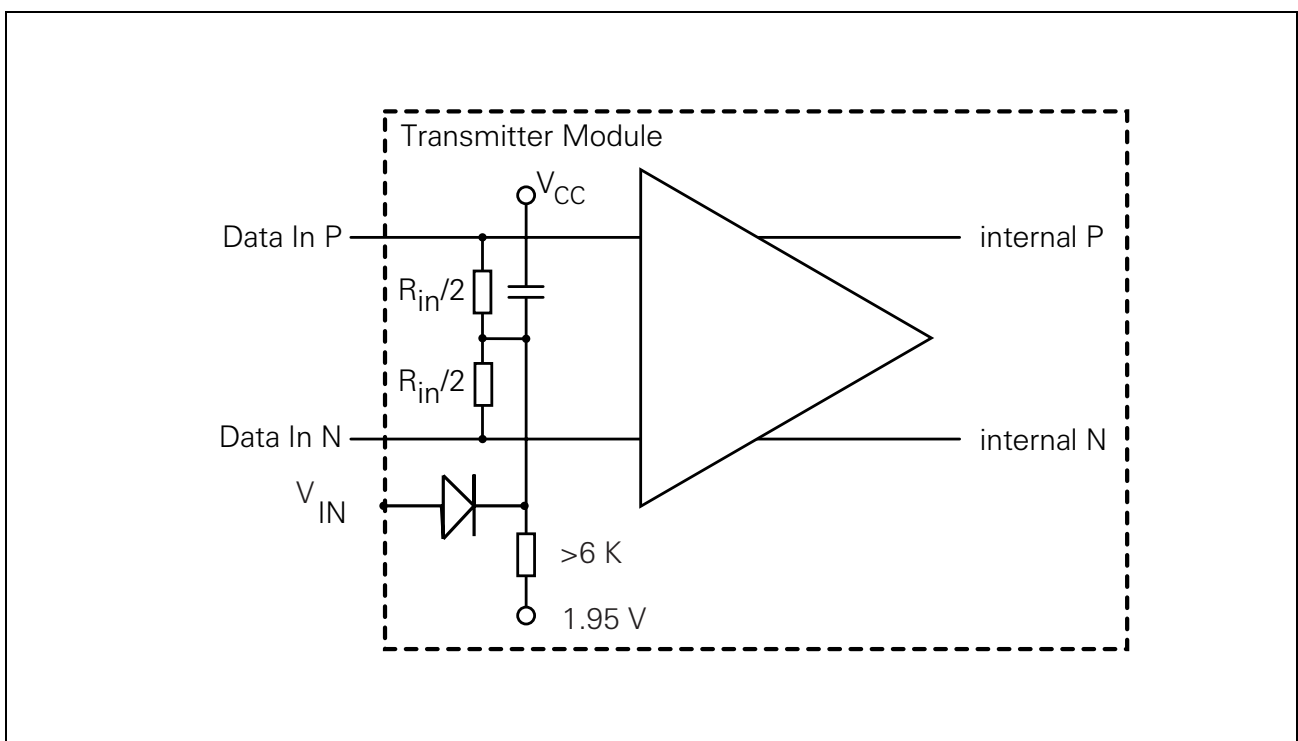
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Transmitter				
Power Supply Voltage	$V_{CC}$	3.135	3.6	V
Noise on Power Supply <sup>1)</sup>	$N_{PS1}$		50	mV
Noise on Power Supply <sup>2)</sup>	$N_{PS2}$		100	mV
Data Input Voltage Range <sup>3), 4)</sup>	$V_{DATAI}$	500	$V_{CC}$	mV
Data Input Differential Voltage <sup>4), 5)</sup>	$ V_{ID} $	80	1000	mV
Data Input Skew <sup>6)</sup>	$t_{SPN}$		$0.5 \times t_R, t_F$	ps
Data Input Rise/Fall Time <sup>7)</sup>	$t_R, t_F$	50	300	ps
LVC MOS Input High Voltage	$V_{LVCMOSIH}$	2.0	$V_{CC}$	V
LVC MOS Input Low Voltage	$V_{LVCMOSIL}$	$V_{EE}$	0.8	V
LVC MOS Input Rise/Fall Time <sup>8)</sup>	$t_R, t_F$		20	ns
Receiver				
Power Supply Voltage	$V_{CC}$	3.0	3.6	V
Noise on Power Supply <sup>1)</sup>	$N_{PS1}$		50	mV
Noise on Power Supply <sup>2)</sup>	$N_{PS2}$		100	mV
Differential LVDS Termination Impedance	$R_t$	80	120	$\Omega$
LVC MOS Input High Voltage	$V_{LVCMOSIH}$	2.0	$V_{CC}$	V
LVC MOS Input Low Voltage	$V_{LVCMOSIL}$	$V_{EE}$	0.8	V
LVC MOS Input Rise/Fall Time <sup>8)</sup>	$t_R, t_F$		20	ns
Optical Input Rise/Fall Time <sup>9)</sup>	$t_R, t_F$		320	ps
Input Extinction Ratio	ER	6.0		dB
Input Center Wavelength	$\lambda_C$	830	860	nm

Voltages refer to  $V_{EE} = 0$  V.

- <sup>1)</sup> Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.  
<sup>2)</sup> Noise frequency is > 10 MHz. Voltage is peak-to-peak value.  
<sup>3)</sup> This implies that the input stage can be AC coupled.  
<sup>4)</sup> Input level diagram: see **Figure 5**.  
<sup>5)</sup>  $|V_{ID}| = |(\text{input voltage of non-inverted input minus input voltage of inverted input})|$ .  
<sup>6)</sup> Skew between positive and negative inputs measured at 50% level.  
<sup>7)</sup> 20% - 80% level.  
<sup>8)</sup> Measured between 0.8 V and 2.0 V.  
<sup>9)</sup> 20% - 80% level. Non filtered values.



**Figure 5** Input Level Diagram



**Figure 6** Input Stage

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

**Transmitter Electrical Characteristics**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply Current	$I_{CC}$		350	450	mA
Power Consumption	$P$		1.2	1.6	W
Data Rate per Channel	DR	500 <sup>1)</sup>		1600	Mbit/s
LVC MOS Output Voltage Low	$V_{LVC MOSOL}$			0.4	V
LVC MOS Output Voltage High	$V_{LVC MOSOH}$	2.5			V
LVC MOS Input Current High/Low	$I_{LVC MOSI}$	−500		500	μA
LVC MOS Output Current High <sup>2)</sup>	$I_{LVC MOSOH}$			0.5	mA
LVC MOS Output Current Low <sup>3)</sup>	$I_{LVC MOSOL}$			4.0	mA
Data Differential Input Impedance <sup>4)</sup>	$R_{IN}$	80		120	Ω
Data Input Differential Current	$ I_I $			5.5	mA

<sup>1)</sup> Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.

<sup>2)</sup> Source current.

<sup>3)</sup> Sink current.

<sup>4)</sup> Data input stage.



**Transmitter Electro-Optical Characteristics**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Optical Rise Time <sup>1)</sup>	$t_R$			200	ps
Optical Fall Time <sup>1)</sup>	$t_F$			200	ps
Total Jitter <sup>2)</sup>	$J_T$			0.284	UI
Deterministic Jitter	$J_D$			0.1	UI
Channel-to-channel skew <sup>3)</sup>	$t_{CSK}$			100	ps
Launched Average Power	$P_{AVG}$	-9.0	-5.0	-3.0	dBm
Launched Power Shutdown	$P_{SD}$			-30.0	dBm
Center Wavelength	$\lambda_C$	830		860	nm
Spectral Width (FWHM)	$\Delta\lambda$			2	nm
Spectral Width (rms)	$\Delta\lambda$			0.85	nm
Relative Intensity Noise	RIN			-117	dB/Hz
Extinction Ratio (dynamic)	ER	6.0			dB
Optical Modulation Amplitude <sup>4)</sup>	OMA	0.15 <sup>5)</sup>	0.46 <sup>6)</sup>		mW
Eye mask compliance		to be defined <sup>7)</sup>			

Optical parameters valid for each channel.

<sup>1)</sup> 20% - 80% level, non filtered values.

<sup>2)</sup> Measured using a filter as defined in IEEE 802.3 (2000-edition) Gigabit Ethernet specification, section 38.6.5.

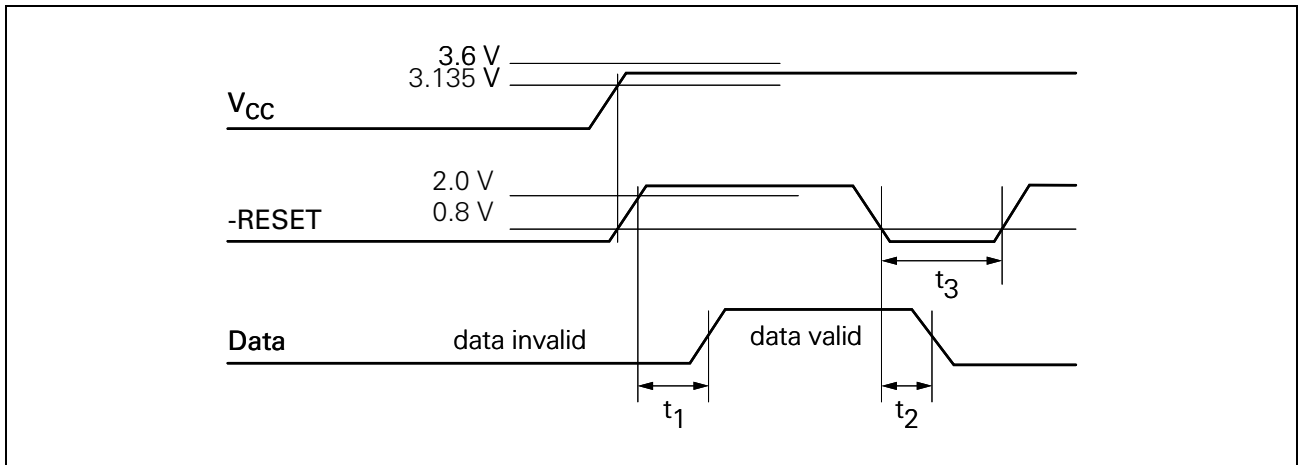
<sup>3)</sup> With input channel-to-channel skew 0 ps and a maximum data channel-to-channel average deviation and swing deviation of 5%.

<sup>4)</sup> Peak to peak values.

<sup>5)</sup> Corresponds to a minimum extinction ratio of 6 dB.

<sup>6)</sup> Corresponds to a typical extinction ratio of 8 dB.

<sup>7)</sup> GBE mask (IEEE 802.3, sec. 38.6.5.) adopted for data rate available.



**Figure 7**      **Timing Diagram**

Parameter	Symbol	Limit Values		Unit
		min.	max.	
–RESET on Delay Time	$t_1$		100	ms
–RESET off Delay Time	$t_2$		50	μs
–RESET Low Duration <sup>1)</sup>	$t_3$	10		μs

<sup>1)</sup> Only when not used as power on reset. At any failure recovery, –RESET must be brought to low level for at least  $t_3$ .

## Receiver Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply Current	$I_{CC}$		250	350	mA
Power Consumption	$P$		0.8	1.3	W
LVDS Output Low Voltage <sup>1), 2)</sup>	$V_{LVDSOL}$	925			mV
LVDS Output High Voltage <sup>1), 2)</sup>	$V_{LVDSOH}$			1475	mV
LVDS Output Differential Voltage <sup>1), 2), 3)</sup>	$ V_{OD} $	250		400	mV
LVDS Output Offset Voltage <sup>1), 2), 4)</sup>	$V_{OS}$	1125		1275	mV
LVDS Rise/Fall Time <sup>5)</sup>	$t_R, t_F$			400	ps
LVC MOS Output Voltage Low	$V_{LVC MOSOL}$			400	mV
LVC MOS Output Voltage High	$V_{LVC MOSOH}$	2500			mV

## Receiver Electrical Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LVC MOS Input Current High/Low	$I_{\text{LVC MOSI}}$	-500		500	$\mu\text{A}$
LVC MOS Output Current High <sup>6)</sup>	$I_{\text{LVC MOSOH}}$			0.5	mA
LVC MOS Output Current Low <sup>7)</sup>	$I_{\text{LVC MOSOL}}$			4.0	mA
Total Jitter <sup>8), 9)</sup>	$J_{\text{T}}$			0.39	UI
Deterministic Jitter <sup>8)</sup>	$J_{\text{D}}$			0.12	UI
Channel-to-channel skew <sup>10)</sup>	$t_{\text{CSK}}$			100	ps

<sup>1)</sup> Output level diagram: see **Figure 8**.

<sup>2)</sup> LVDS output must be terminated differentially with  $R_{\text{t}}$ .

<sup>3)</sup>  $|V_{\text{OD}}| = |(\text{output voltage of non-inverted output minus output voltage of inverted output})|$ .

<sup>4)</sup>  $V_{\text{OS}} = 1/2 (\text{output voltage of inverted output} + \text{output voltage of non-inverted output})$ .

<sup>5)</sup> Measured between 20% and 80% level with a maximum capacitive load of 5 pF.

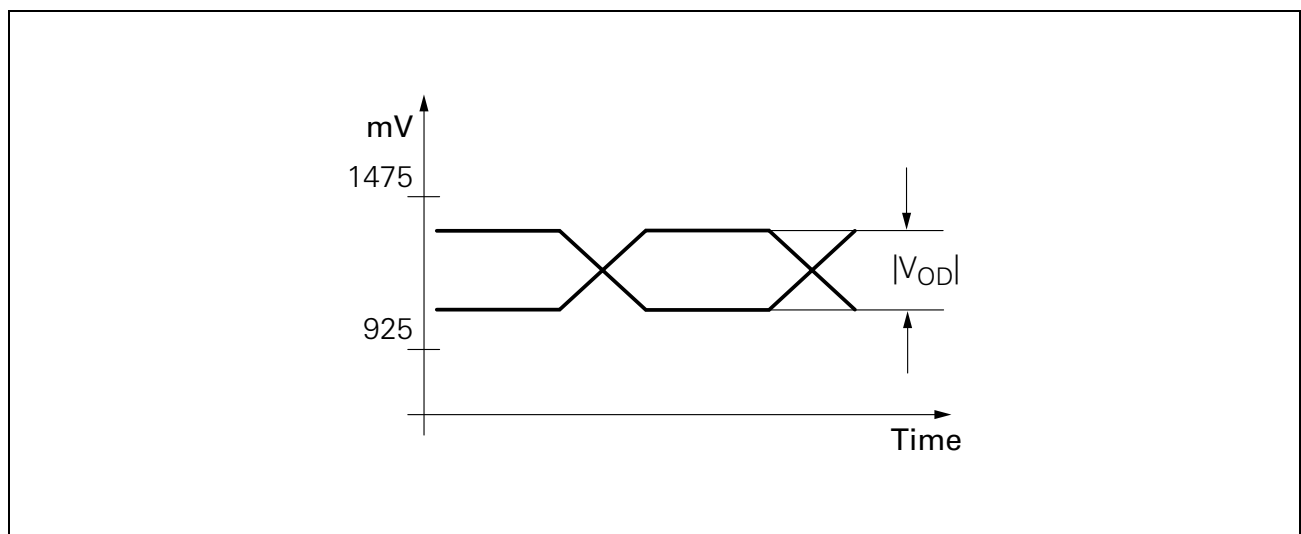
<sup>6)</sup> Source current.

<sup>7)</sup> Sink current.

<sup>8)</sup> With no optical input jitter.

<sup>9)</sup> At sensitivity limit of 0.032 mW OMA.

<sup>10)</sup> With input channel-to-channel skew 0 ps.



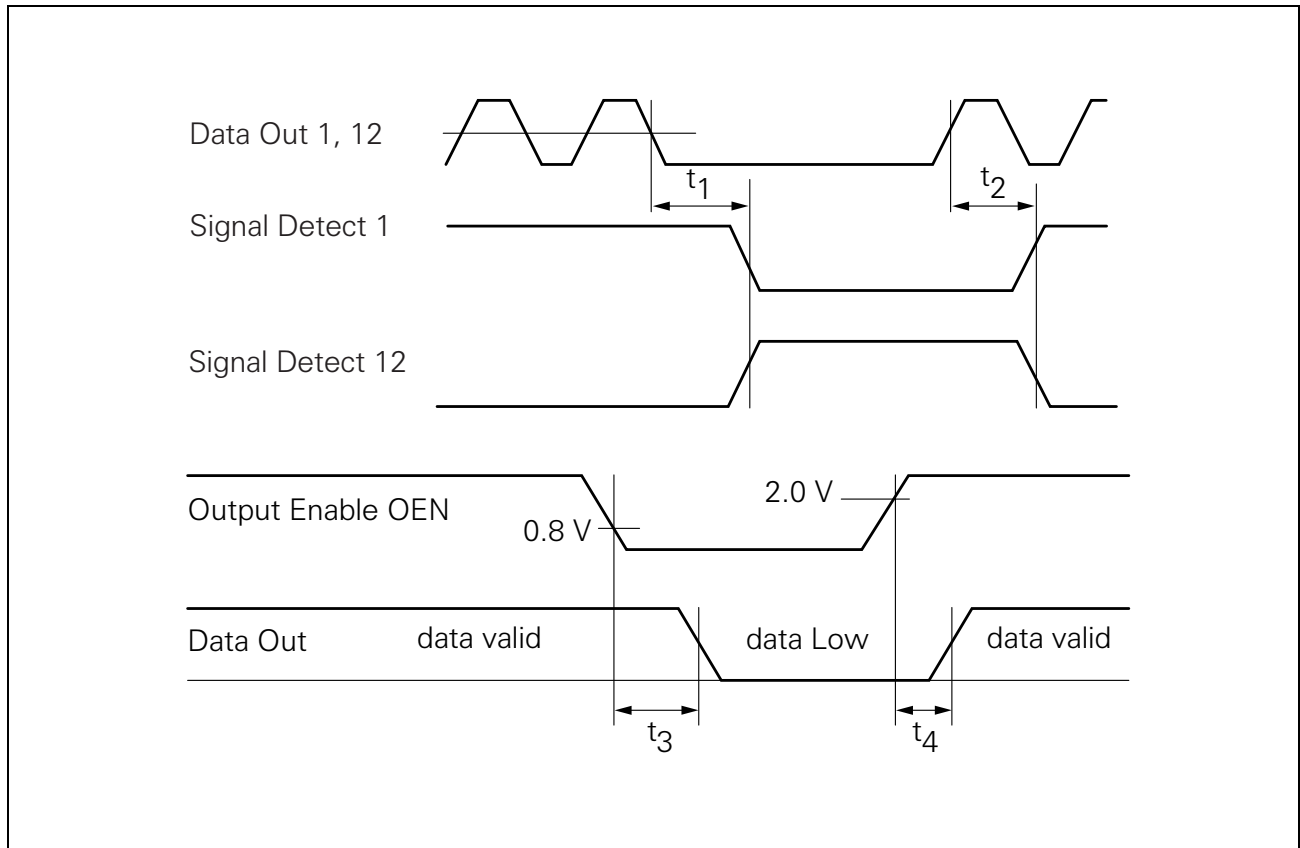
**Figure 8** Output Level Diagram

**Receiver Electro-Optical Characteristics**

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Data Rate per Channel	DR	500 <sup>1)</sup>	1600	Mbit/s
Sensitivity (Average Power) <sup>2)</sup>	$P_{IN}$		-18.0	dBm
Optical Modulation Amplitude <sup>3)</sup>	OMA	0.032 <sup>4)</sup>		mW
Saturation (Average Power)	$P_{SAT}$	-3.0		dBm
Signal Detect Assert Level <sup>5)</sup>	$P_{SDA}$		-19.0	dBm
Signal Detect Deassert Level <sup>5)</sup>	$P_{SDD}$	-29.0		dBm
Signal Detect Hysteresis <sup>5)</sup>	$P_{SDA}$ $-P_{SDD}$	1.0	4.0	dB
Return Loss of Receiver	$A_{RL}$	12		dB

Optical parameters valid for each channel.

- <sup>1)</sup> Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
- <sup>2)</sup> BER =  $10^{-12}$ , Extinction ratio = infinite, Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
- <sup>3)</sup> Peak to peak value.
- <sup>4)</sup> Corresponds to a maximum sensitivity (average power) of -18.0 dBm at an infinite extinction ratio.
- <sup>5)</sup> Extinction ratio = infinite,  
 $P_{SDA}$ : Average optical power when SD switches from inactive to active.  
 $P_{SDD}$ : Average optical power when SD switches from active to inactive.



**Figure 9**      **Timing Diagrams**

Parameter	Symbol	Max.	Unit
Signal Detect Deassert Time	$t_1$	10	$\mu\text{s}$
Signal Detect Assert Time	$t_2$	10	$\mu\text{s}$
LVDS Output Enable off Delay Time	$t_3$	20	ns
LVDS Output Enable on Delay Time	$t_4$	20	ns

## Assembly

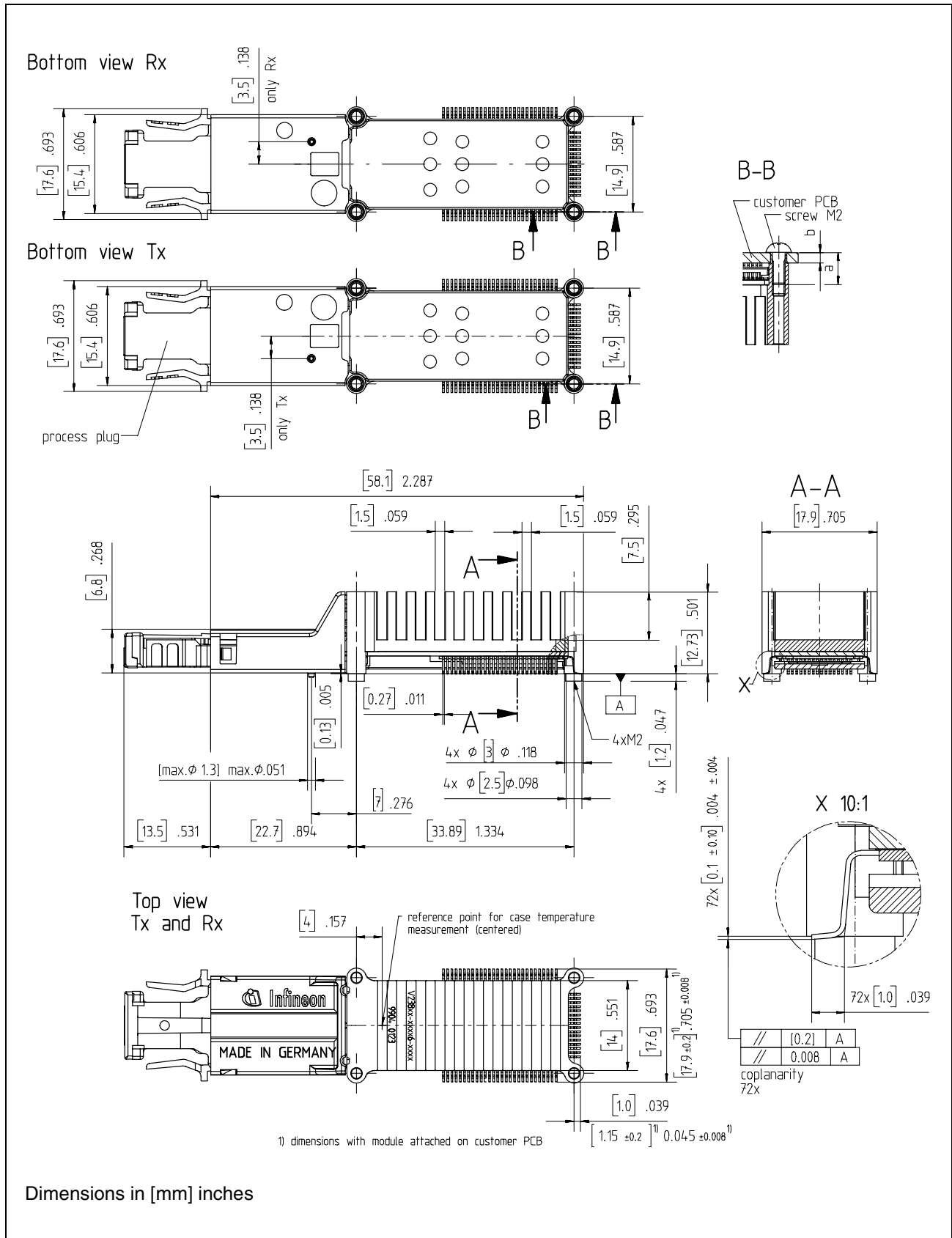
On the next pages are some figures to assist the customer in designing his printed circuit board (PCB). **Figure 10** shows the mechanical dimensions of the PAROLI transmitter and receiver modules and **Figure 11** to **Figure 13** give the dimensions of the holes and solder pads on a customer PCB that are necessary to mount the modules on this PCB. Keeping the tolerances for the PCB given in **Figure 11** to **Figure 13** is required to properly attach the PAROLI transmitter and receiver module to the PCB.

Attachment to the customer PCB should be done with four M2 screws torqued to 0.25 Nm +0.05 Nm (see **Figure 10**, cross section B-B). The screw length  $a$  should be 3 to 4 mm plus the thickness  $b$  of the customer PCB.

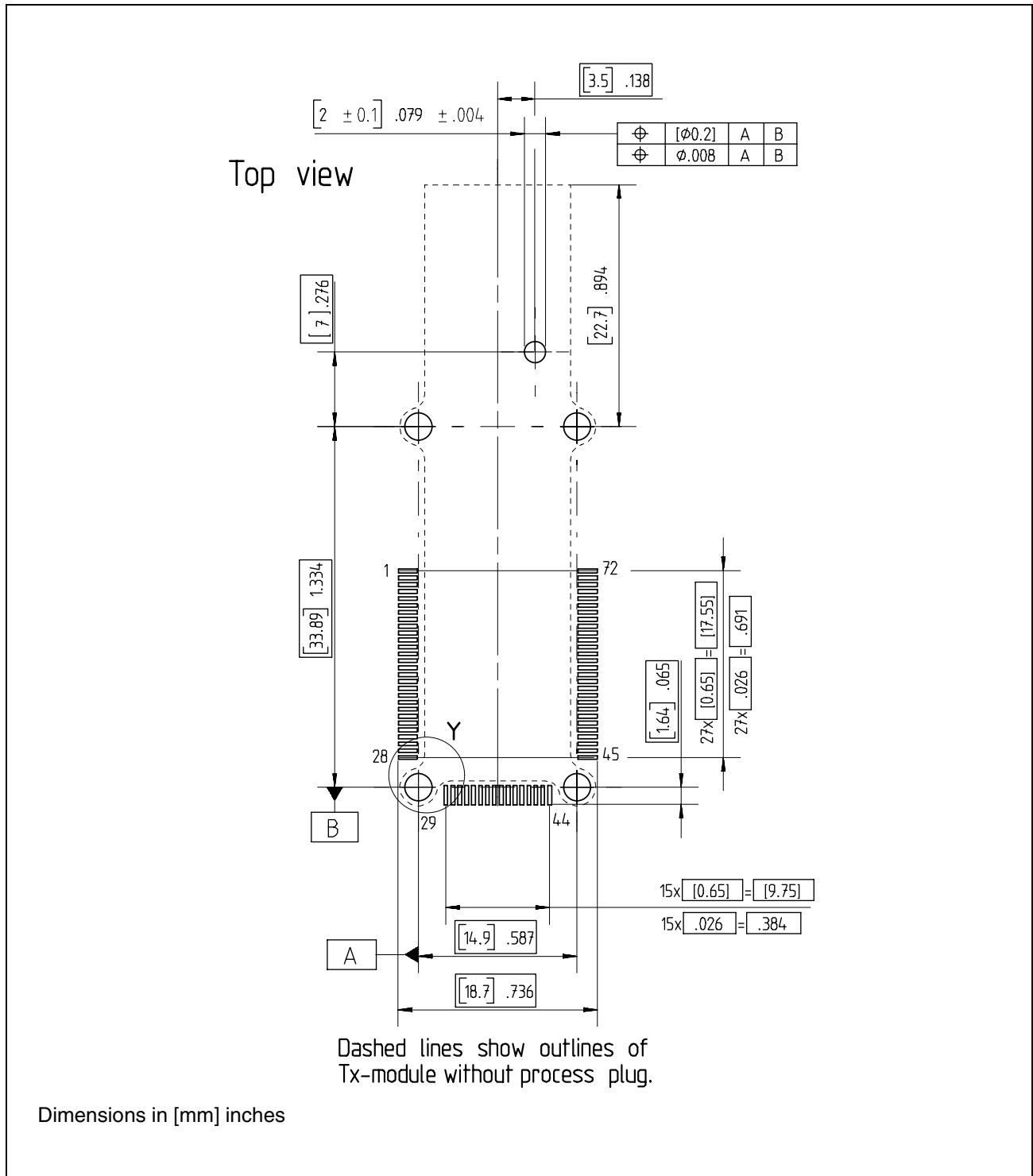
Special care must be taken to remove residues from the soldering and washing process which can impact the mechanical function. Avoid the use of aggressive organic solvents like ketones, ethers, etc. Consult the supplier of the PAROLI modules and the supplier of the solder paste and flux for recommended cleaning solvents.

The following common cleaning solvents will not affect the module: deionized water, ethanol, and isopropyl alcohol. Air-drying is recommended to a maximum temperature of 150°C. Do not use ultrasonics.

During soldering, heat must be applied to the leads only, to ensure that the case temperature never exceeds 150°C. The module must be mounted with a hot-air or hot-bar soldering process using a SnPb solder type, e.g. Sn62Pb36Ag2, in accordance with ISO 9435.

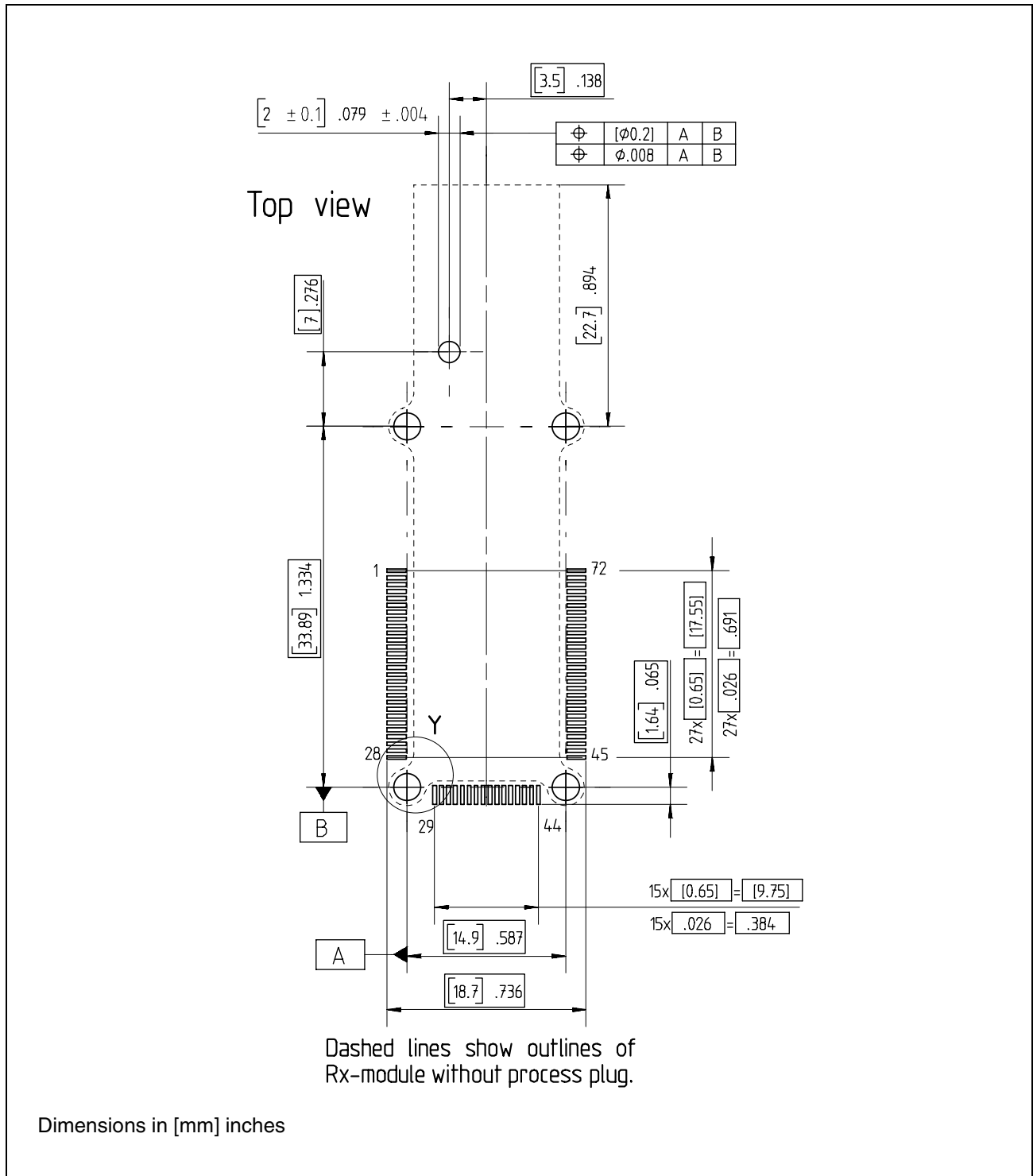


**Figure 10 Drawing of the PAROLI Transmitter and Receiver Module**



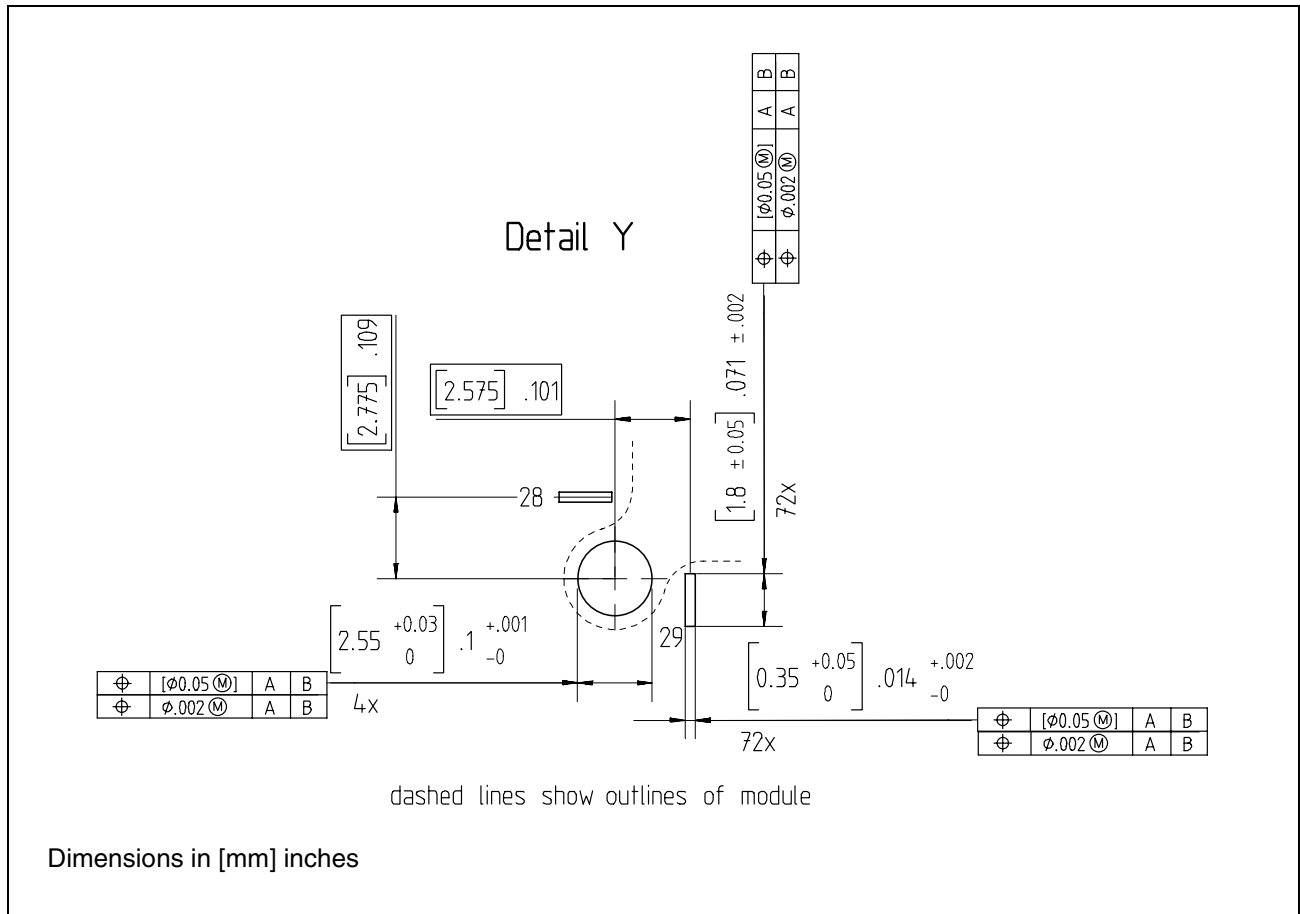
**Figure 11 Recommended Circuit Board Layout: Transmitter**



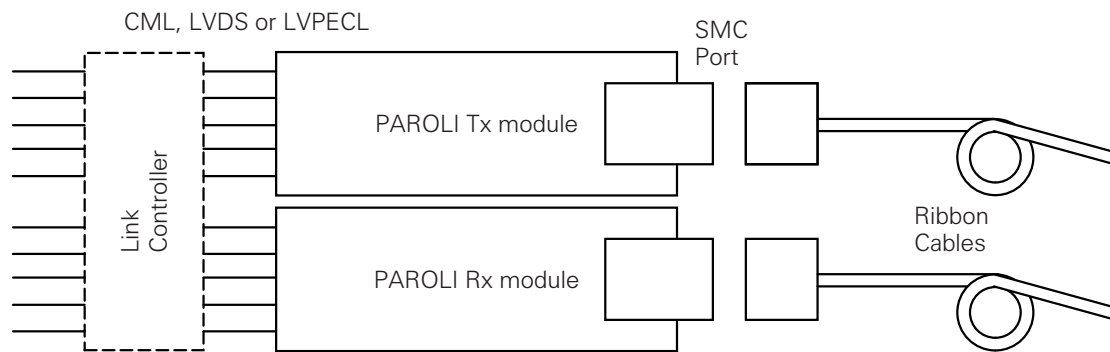


**Figure 12 Recommended Circuit Board Layout: Receiver**

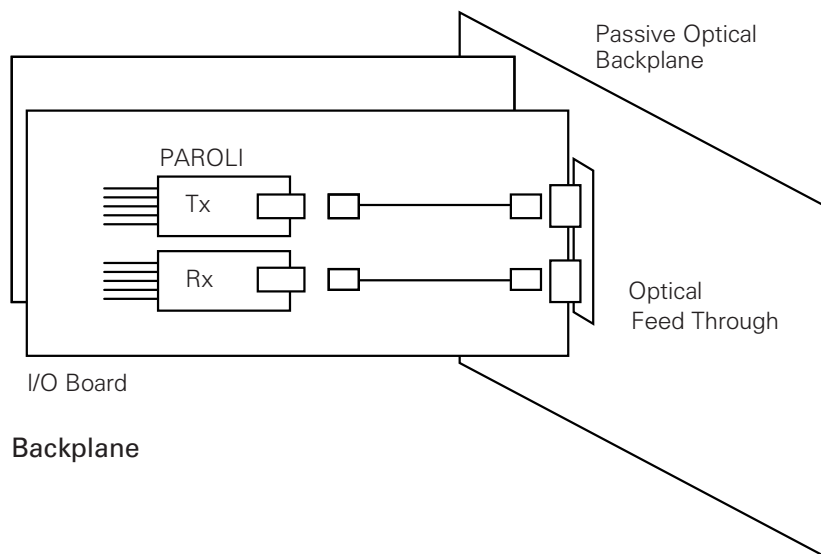
No electronic components are allowed on the customer PCB within the area covered by the PAROLI module and the jumper used to attach a ribbon fiber cable.



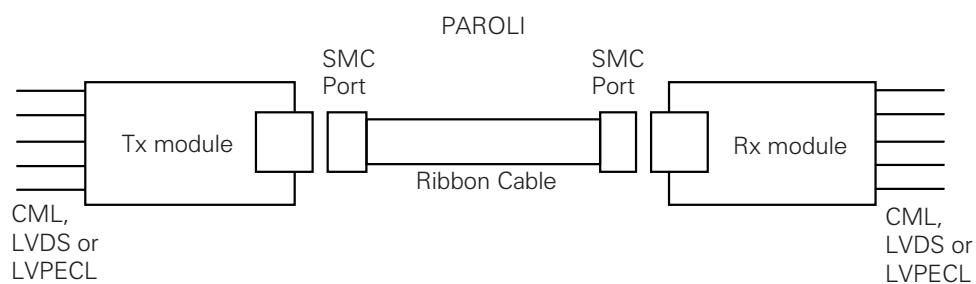
**Figure 13 Mounting Hole, Detail Y (see Figure 11 and Figure 12)**



Board-to-Board



Backplane



Point-to-Point

**Figure 14 Applications**

## Package Outlines

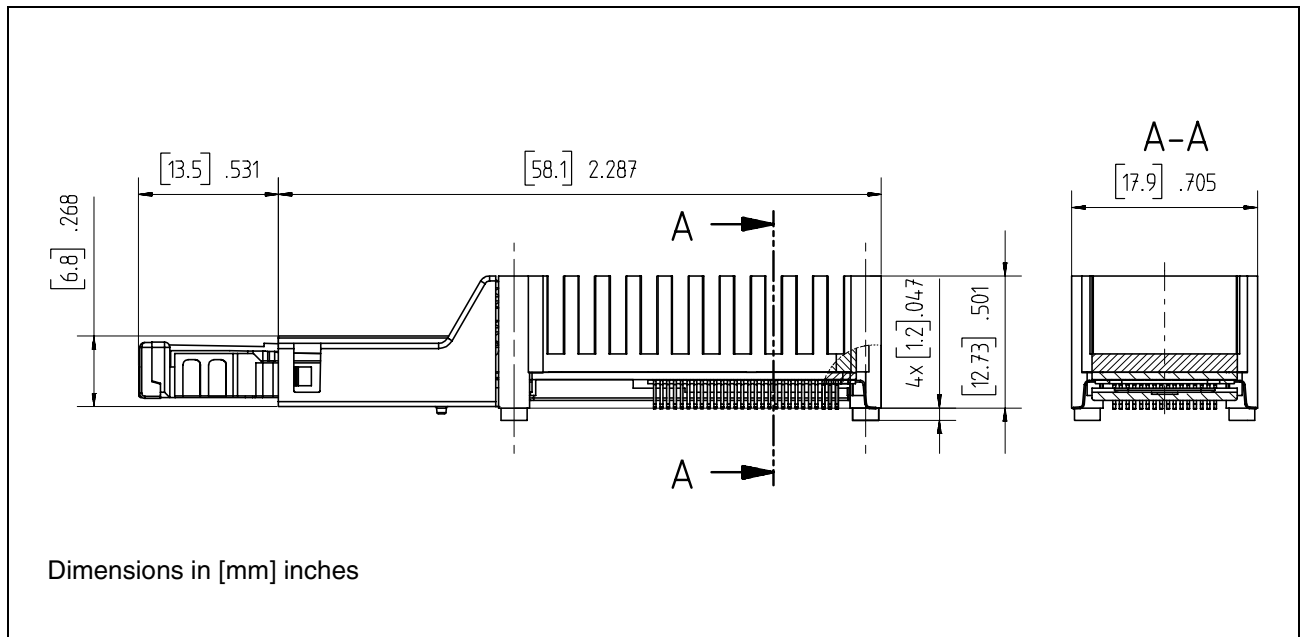


Figure 15

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**V23814-U1306-M136**

**V23815-U1306-M136**

**Revision History: 2002-05-14**

**DS1**

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Previous Version: 2001-12-01

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<b>Page</b>	<b>Subjects (major changes since last revision)</b>
12	Class 1 Laser Product changed to Class 1M Laser Product; Caution: ... added

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