

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

# TB62715FNG

## 8 BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

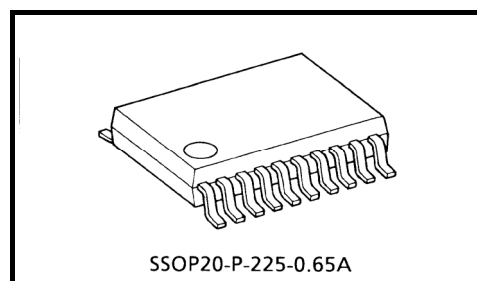
The TB62715FNG is specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output circuits is able to set up external resistor ( $I_{OUT} = 2 \sim 150 \text{ mA}$ ).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 8 bit shift register, latch, AND-GATE & Constant Current Drivers.

The TB62715FNG complies with RoHS regulation.



Weight: 0.14 g (typ.)

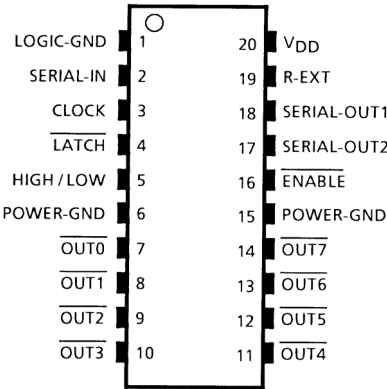
## FEATURES

- Constant Current Output: Can set up all output current with one resistor for 2 to 150 mA.
- Constant Output Current Matching : ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ )

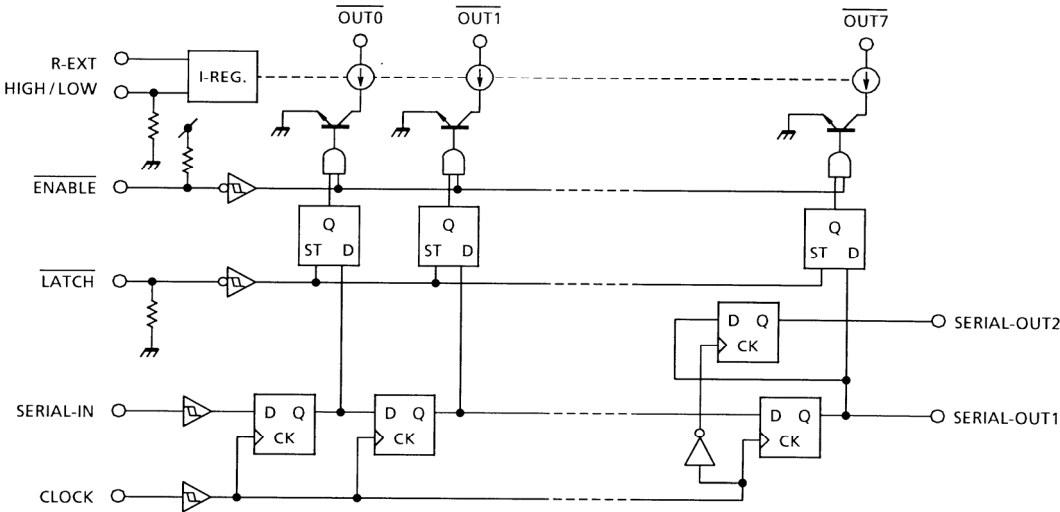
HIGH / LOW	OUTPUT-GND VOLTAGE	CURRENT MATCHING (BIT)	CURRENT MATCHING (LOT)	OUTPUT CURRENT (MAX.)
"L"	$\geq 0.7 \text{ V}$	$\pm 6.0 \%$	$\pm 15.0 \%$	2~70 mA
"H"	$\geq 1.0 \text{ V}$	$\pm 6.0 \%$	$\pm 15.0 \%$	50~150 mA

- Maximum Clock Frequency:  $f_{CLK} = 15 \text{ MHz}$   
(Cascade Connected Operate,  $T_{opr} = 25^\circ\text{C}$ )
- 5 V - CMOS Compatible Input
- Package: SSOP20-P-225-0.65A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

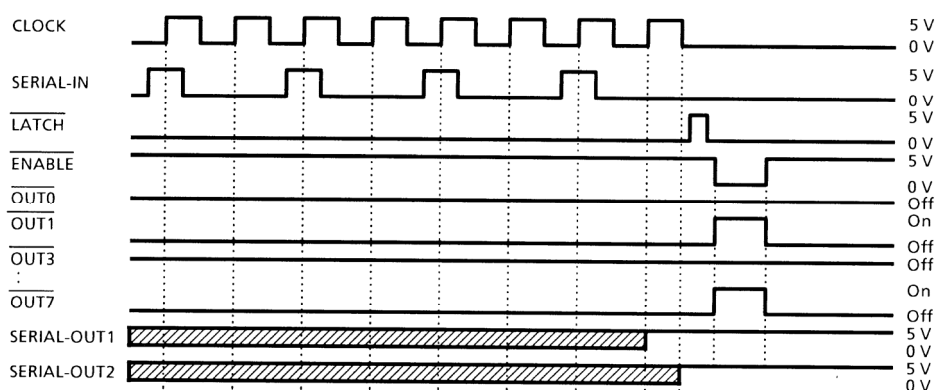


TRUTH TABLE

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ... OUT5 ... OUT7	SERIAL-OUT
UP	H	L	$D_n$	$D_n \cdots D_{n-5} \cdots D_{n-7}$	$D_{n-7}$
UP	L	L	$D_{n+1}$	No Change	$D_{n-6}$
UP	H	L	$D_{n+2}$	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	$D_{n-5}$
DOWN	X	L	$D_{n+3}$	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	$D_{n-5}$
DOWN	X	H	$D_{n+3}$	Off	$D_{n-5}$

Note:  $\overline{\text{OUT0}} \sim \overline{\text{OUT7}} = \text{on}$  in case of  $D_n = \text{H level}$  and  $\overline{\text{OUT0}} \sim \overline{\text{OUT7}} = \text{off}$  in case of  $D_n = \text{level}$ .  
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

## TIMING DIAGRAM



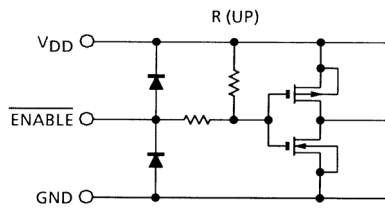
Note: Latches are level sensitive, not rising edge sensitive and not synchronous to CLOCK.  
Input of **LATCH** –terminal to H Level, data passes latches, and input to L level, data hold latches.  
Input of **ENABLE** –terminal to H level, all output ( **OUT0 ~ 7** ) do off.

## TERMINAL DISCRIPTION

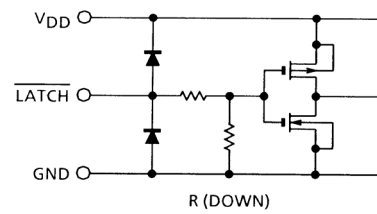
PIN No.	PIN NAME	FUNCTION
5	HIGH / LOW	It is the terminal which does switching for the big current / low current.
6, 15	POWER-GND	GND terminal for current output.
1	LOGIC-GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
7~10, 11~14	OUT0 ~ 7	Output terminals.
16	ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-terminal, and do on with "L" level input.
18	SERIAL-OUT1	Output terminal of serial-data
17	SERIAL-OUT2	Output terminal of a serial-data for next SERIAL-IN terminal.
19	R-EXT	Input terminal of connects with a resistor for to set up all output current.
20	VDD	5 V Supply voltage terminal.

## EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

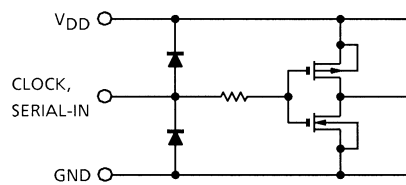
### 1. $\overline{\text{ENABLE}}$ terminal



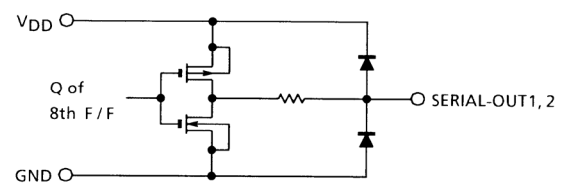
### 2. $\overline{\text{LATCH}}$ terminal



### 3. CLOCK, SERIAL-IN terminal



### 4. SERIAL-OUT terminal



**ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	0 ~ +7.0	V
Input Voltage	V <sub>IN</sub>	-0.4 ~ V <sub>DD</sub> +0.4	V
Output Current	I <sub>OUT</sub>	+150 (HIGH / LOW = "H")	mA / ch
		+70 (HIGH / LOW = "L")	
Output Voltage	V <sub>OUT</sub>	-0.5 ~ +17.0	V
Clock Frequency	f <sub>CLK</sub>	15	MHz
Power Dissipation	P <sub>D1</sub>	0.71 (FREE AIR)	W
	P <sub>D2</sub>	0.96 (ON PCB)	
Thermal Resistance	R <sub>th (j-a)</sub> 1	175 (FREE AIR)	°C / W
	R <sub>th (j-a)</sub> 2	130 (ON PCB)	
Operating Temperature	T <sub>opr</sub>	-40 ~ +85	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +150	°C
Junction temperature	T <sub>j</sub>	150	°C

Note: Ambient temperature delated above 25°C in the proportion of 7.69 mW / °C  
Condition = On PCB (50 × 50 × 1.6 mm Cu = 40%)

**RECOMMENDED OPERATING CONDITION (Ta = 25°C unless otherwise noted)**

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
Output Voltage	V <sub>OUT</sub>		—	—	15.0	V
Output Current	I <sub>OUT1</sub>	DC 1 circuit (HIGH / LOW = "H")	50	—	130	mA / ch
	I <sub>OUT2</sub>	DC 1 circuit (HIGH / LOW = "L")	2	—	60	
	I <sub>OH</sub>	SERIAL-OUT1, 2	—	—	-1.0	mA
	I <sub>OL</sub>	SERIAL-OUT1, 2	—	—	1.0	
Input Voltage	V <sub>IH</sub>	V <sub>DD</sub> = 4.5~5.5 V	0.7 V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V
	V <sub>IL</sub>		-0.3	—	0.3 V <sub>DD</sub>	
$\overline{\text{LATCH}}$ Pulse Width	t <sub>w</sub> $\overline{\text{LAT}}$		100	—	—	ns
CLOCK Pulse Width	t <sub>w</sub> CLK		50	—	—	ns
$\overline{\text{ENABLE}}$ Pulse Width	t <sub>w</sub> $\overline{\text{EN}}$		1000	—	—	ns
Set-up Time for DATA	t <sub>setup</sub> (D)		60	—	—	ns
Hold Time for DATA	t <sub>hold</sub> (D)		20	—	—	ns
Set-up Time for $\overline{\text{LATCH}}$	t <sub>setup</sub> (L)		100	—	—	ns
Hold Time for $\overline{\text{LATCH}}$	t <sub>hold</sub> (L)		60	—	—	ns
Clock Frequency	f <sub>CLK</sub>	V <sub>DD</sub> = 4.5~5.5 V, Cascade Operation	10.0	—	—	MHz
Power Dissipation	P <sub>D</sub>	Ta = 85°C (On PCB)	—	—	0.50	W

## ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

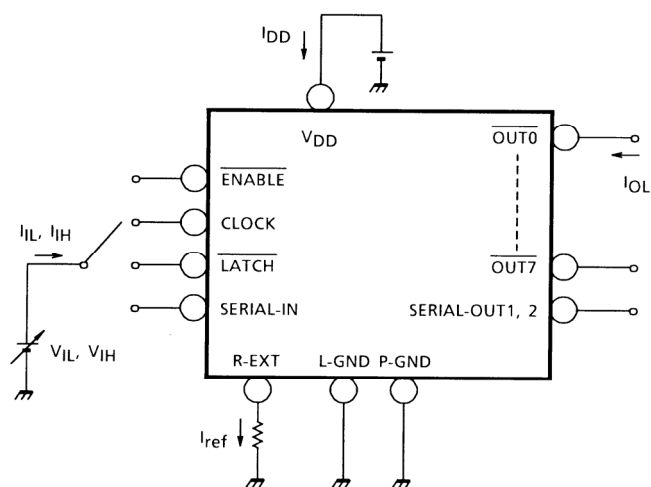
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V <sub>IH</sub>	1	—	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V
	"L" Level	V <sub>IL</sub>		—	GND	—	0.3 V <sub>DD</sub>	
Output Leakage Current		I <sub>OH</sub>	1	V <sub>OH</sub> = 15.0 V	—	—	10	μA
Output Voltage	SERIAL-OUT 1, 2	V <sub>OH</sub>	1	I <sub>OL</sub> = -1.0 mA	—	—	0.4	V
		V <sub>OL</sub>		I <sub>OL</sub> = +1.0 mA	4.6	—	—	
Output Current 1		I <sub>OL1</sub>	1	V <sub>CE</sub> = 0.7 V R <sub>EXT</sub> = 520 Ω, HIGH / LOW = "L"	31.7	37.5	43.1	mA
	Current Skew	dI <sub>OL1</sub>			—	±1.5	±6.0	
Output Current 2		I <sub>OL2</sub>	1	V <sub>CE</sub> = 1.0 V R <sub>EXT</sub> = 160 Ω, HIGH / LOW = "H"	104.0	123.0	141.4	mA
	Current Skew	dI <sub>OL2</sub>			—	±1.5	±6.0	
Supply Voltage Regulation		% / V <sub>DD</sub>	1	Ta = -40~ +85°C	—	+1.5	+5.0	% / V
Pull-up Resistor		R <sub>IN</sub> (up)	1		100	200	400	kΩ
Pull-down Resistor		R <sub>IN</sub> (down)			100	200	400	
Supply Current	"OFF"	I <sub>DD</sub> (off) 1	1	R <sub>EXT</sub> = OPEN $\overline{\text{OUT0}} \sim \overline{7}$ = off	—	1.0	2.0	mA
		I <sub>DD</sub> (off) 2		R <sub>EXT</sub> = 260 Ω $\overline{\text{OUT0}} \sim \overline{7}$ = off	—	10.0	15.0	
		I <sub>DD</sub> (off) 3		R <sub>EXT</sub> = 160 Ω $\overline{\text{OUT0}} \sim \overline{7}$ = off	—	16.0	21.0	
	"ON"	I <sub>DD</sub> (on) 1		R <sub>EXT</sub> = 260 Ω $\overline{\text{OUT0}} \sim \overline{7}$ = on	—	23.1	40.5	
		I <sub>DD</sub> (on) 2		R <sub>EXT</sub> = 160 Ω $\overline{\text{OUT0}} \sim \overline{7}$ = on	—	33.0	62.1	

## SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" To "H")	SIN- $\overline{\text{OUTn}}$	$t_{\text{pLH}}$	2	$V_{\text{DD}} = 5.0 \text{ V}$ $V_{\text{CE}} = 1.0 \text{ V}$ $V_{\text{IH}} = V_{\text{DD}}$ , $V_{\text{IL}} = \text{GND}$ $R_{\text{EXT}} = 260 \, \Omega$ , $R_{\text{L}} = 32 \, \Omega$ $I_{\text{OUT}} = 125 \text{ mA}$ , $C_{\text{L}} = 10.5 \text{ pF}$ $t_{\text{or}} : 10\% \text{ to } 90\%$ $t_{\text{of}} : 90\% \text{ to } 10\%$ $t_{\text{pLH}} : 50\% \text{ to } 10\%$ $t_{\text{pHL}} : 50\% \text{ to } 90\%$	—	500	1000	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				—	500	1000	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				—	500	1000	
	CLK-SOUTn				—	30	70	
Propagation Delay Time ("H" To "L")	SIN- $\overline{\text{OUTn}}$	$t_{\text{pHL}}$	2		—	500	1000	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				—	500	1000	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				—	500	1000	
	CLK-SOUTn				—	30	70	
Pulse Width	CLK	$t_{\text{w CLK}} / \text{CLK}$	2		—	20	30	ns
	$\overline{\text{LATCH}}$	$t_{\text{w LAT}} / \text{LAT}$			—	10	25	
Set-Up Time for LATCH / SIN	L-H	$t_{\text{setup LAT}}$ & SIN	2		—	25	50	ns
	H-L				—	25	50	
Hold Time for LATCH / SIN	L-H	$t_{\text{hold LAT}} / \text{SIN}$	2	—	0	15	ns	
	H-L			—	0	15		
Maximum CLOCK Rise Time		$t_{\text{r}}$	2	—	—	10	$\mu\text{s}$	
Maximum CLOCK Fall Time		$t_{\text{f}}$	2	—	—	10	$\mu\text{s}$	
Output Rise Time		$t_{\text{or}}$	2	300	600	1000	ns	
Output Fall Time		$t_{\text{of}}$	2	300	600	1000	ns	

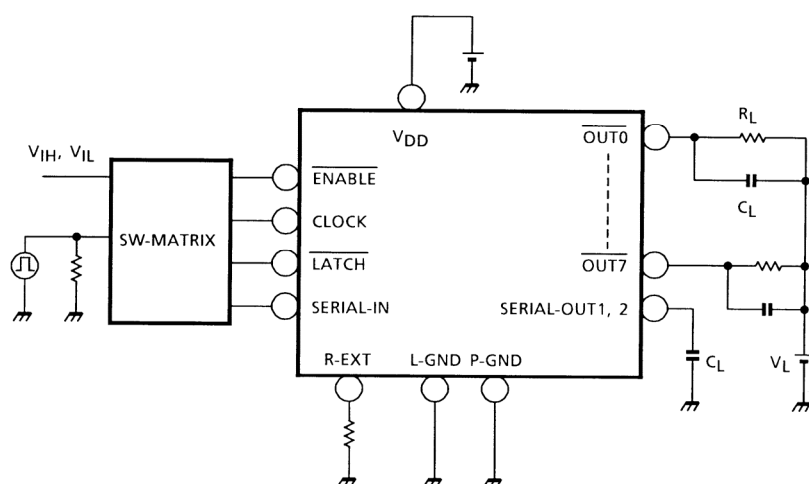
## TEST CIRCUIT

### DC characteristic



TEST CIRCUIT (1)

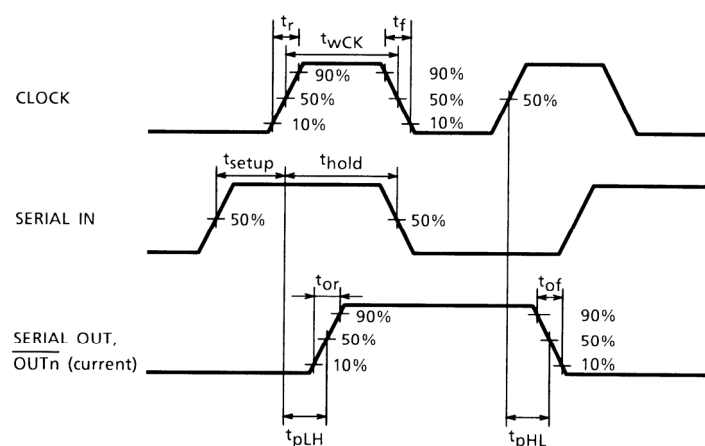
### AC characteristic



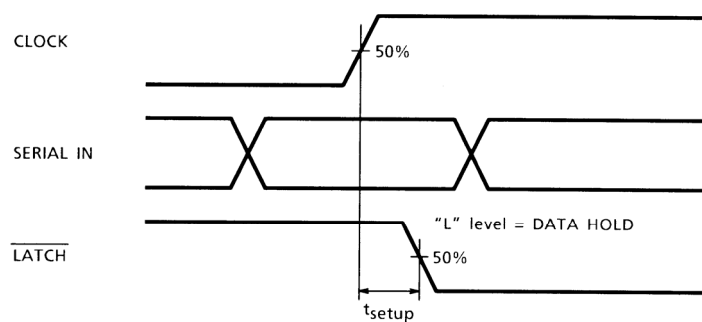
TEST CIRCUIT (2)

## TIMING WAVEFORM

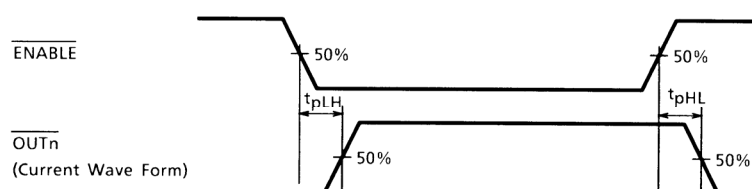
### 1. CLOCK-SERIAL OUT, $\overline{\text{OUTn}}$



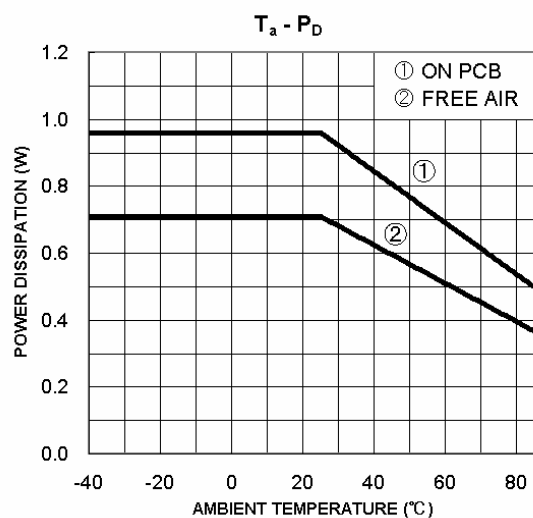
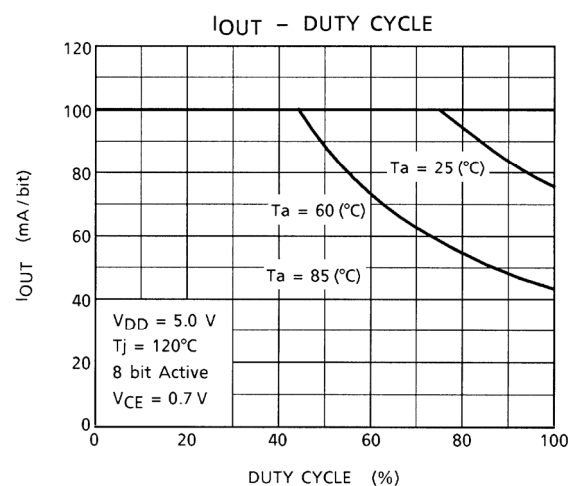
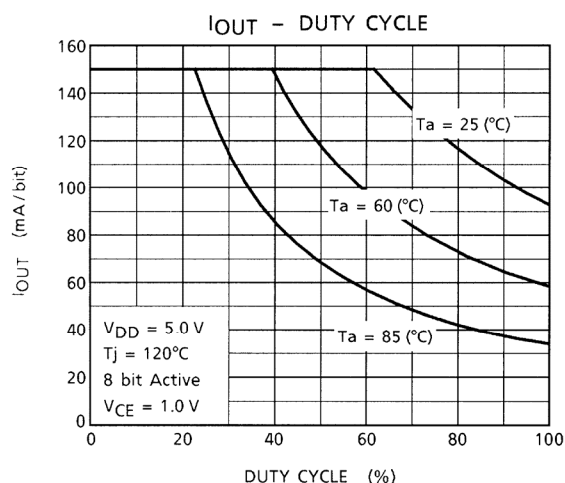
### 2. CLOCK-LATCH



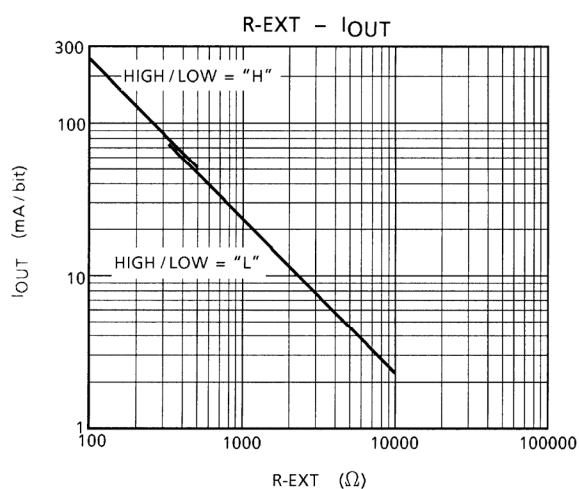
### 3. $\overline{\text{ENABLE}}$ - $\overline{\text{OUTn}}$





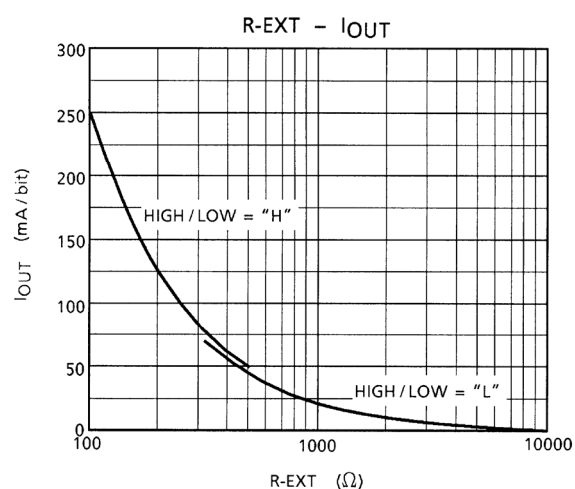


## LED DRIVER TB6270X SERIES APPLICATION NOTE



$$I_{OUT} = \{1.26 \text{ (V)} / R_{EXT} \text{ (}\Omega\text{)}\} \times 15.5 \quad (\text{HIGH/LOW} = \text{"L"})$$

$$I_{OUT} = \{1.26 \text{ (V)} / R_{EXT} \text{ (}\Omega\text{)}\} \times 15.6 \quad (\text{HIGH/LOW} = \text{"H"})$$



## TOTAL SUPPLY VOLTAGE (V<sub>LED</sub>)

This device can operate 0.7 V (V<sub>O</sub>).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

$$V_{LED} \text{ (total supply voltage)} = V_{CE} \text{ (Tr } V_{sat}) + V_f \text{ (LED Forward voltage)} + V_O \text{ (IC supply voltage)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage.

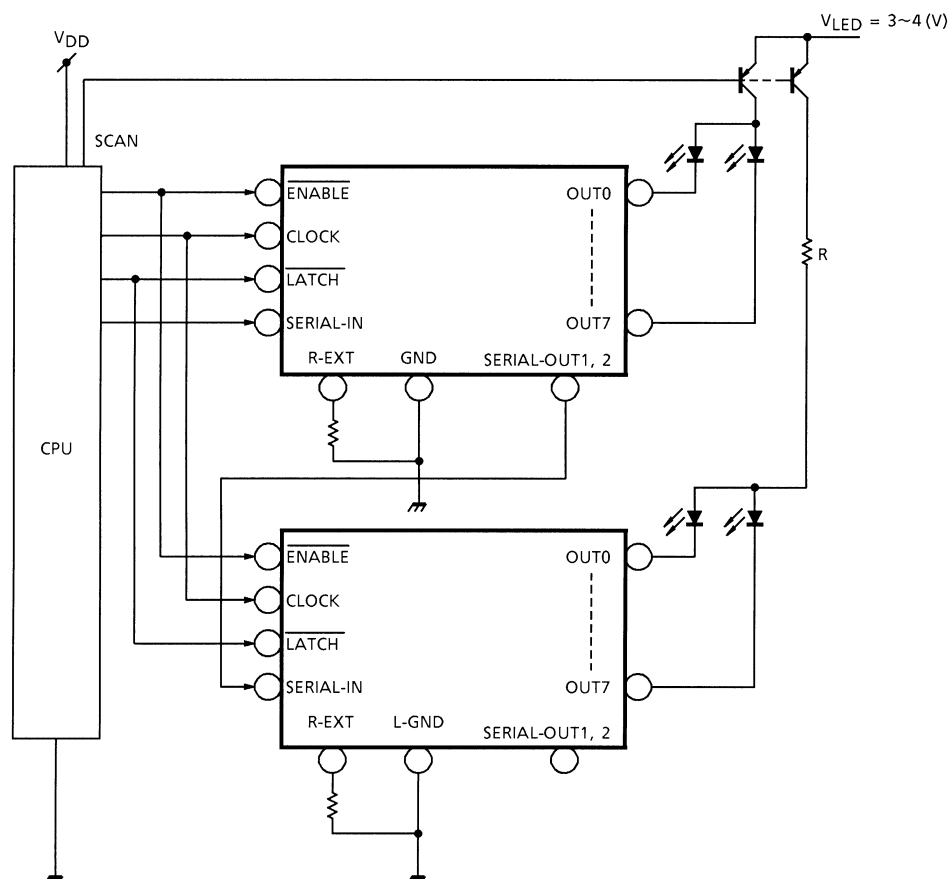
$$R = \frac{V_{LED} - V_f \text{ (LED)} - V_O \text{ (Min.)}}{I_O \text{ (Max.)} \times \text{BIT (Max.)}}$$

## PATTERN LAYOUT

This device owns only one ground pin that means signal ground pin power ground pin are common. If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may malfunction.

So we would like you to pay attention to pattern layout to minimize inductance.

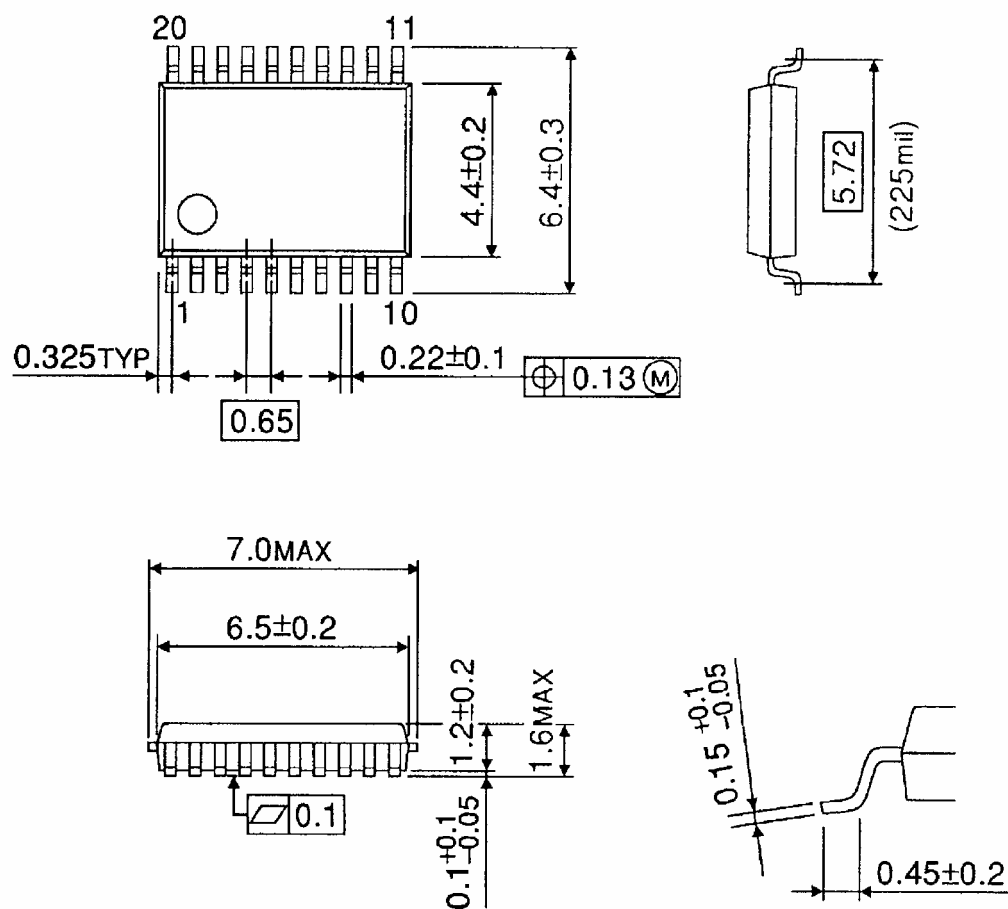
## APPLICATION CIRCUIT



## Package Dimensions

SSOP20-P-225-0.65A

Unit : mm



Weight: 0.14 g (typ.)

**Notes on Contents****1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

**2. Equivalent Circuits**

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**3. Timing Charts**

Timing charts may be simplified for explanatory purposes.

**4. Application Circuits**

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

**5. Test Circuits**

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## **IC Usage Considerations**

### **Notes on Handling of ICs**

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.  
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.  
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.  
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.  
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.  
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

### **Points to Remember on Handling of ICs**

- (1) **Heat Radiation Design**  
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- (2) **Back-EMF**  
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability

- (1) Use of Sn-37Pb solder Bath

- solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

- (2) Use of Sn-3.0Ag-0.5Cu solder Bath

- solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

## RESTRICTIONS ON PRODUCT USE

20070701-EN

- The information contained herein is subject to change without notice.
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