

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A and 10 A, 350 V – 400 V

$r_{DS(on)} = 0.55 \Omega$ and 0.8Ω

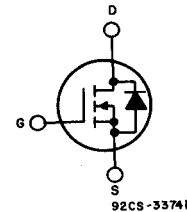
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRF740, IRF741, IRF742, and IRF743 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

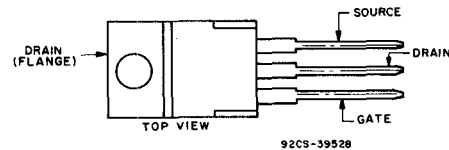
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



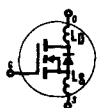
JEDEC TO-220AB

Absolute Maximum Ratings

Parameter	IRF740	IRF741	IRF742	IRF743	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	10	10	8.0	8.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM} Pulsed Drain Current ③	40	40	32	32	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/°C
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
	40	40	32	32	
T_J Operating Junction and Storage Temperature Range	-55 to 150				°C
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF740, IRF741, IRF742, IRF743

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	IRF740 IRF742	400	—	—	V	V _{GS} = 0V	
	IRF741 IRF743	350	—	—	V	I _D = 250 μ A	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250 μ A	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	~500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μ A	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μ A	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	IRF740 IRF741	10	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = 10V	
	IRF742 IRF743	8.0	—	—	A		
	ALL	—	—	—	—		
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF740 IRF741	—	0.47	0.55	Ω	V _{GS} = 10V, I _D = 5.0A	
	IRF742 IRF743	—	.68	.80	Ω		
	ALL	—	—	—	—		
g _{fs} Forward Transconductance ②	ALL	4.0	7.0	—	S (S)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 5.0A	
C _{iss} Input Capacitance	ALL	—	1250	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	300	—	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	80	—	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	17	35	ns	V _{DD} = 175V, I _D = 5.0A, Z _o = 4.7 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	5.0	15	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	45	90	ns		
t _f Fall Time	ALL	—	16	35	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	41	60	nC	V _{GS} = 10V, I _D = 12A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	18	27	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	23	35	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	1.0	°C/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF740 IRF741	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF742 IRF743	—	—	8.0	A	
	ALL	—	—	—	—	
I _{SM} Pulse Source Current (Body Diode) ③	IRF740 IRF741	—	—	40	A	T _C = 25°C, I _S = 10A, V _{GS} = 0V
	IRF742 IRF743	—	—	32	A	
	ALL	—	—	—	—	
V _{SD} Diode Forward Voltage ②	IRF740 IRF741	—	—	2.0	V	T _C = 25°C, I _S = 8.0A, V _{GS} = 0V
	IRF742 IRF743	—	—	1.9	V	
t _{rr} Reverse Recovery Time	ALL	—	800	—	ns	T _J = 150°C, I _F = 10A, dI _F /dt = 100 A/ μ s
Q _{RR} Reverse Recovered Charge	ALL	—	5.7	—	μ C	T _J = 150°C, I _F = 10A, dI _F /dt = 100 A/ μ s
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width < 300 μ s, Duty Cycle < 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF740, IRF741, IRF742, IRF743

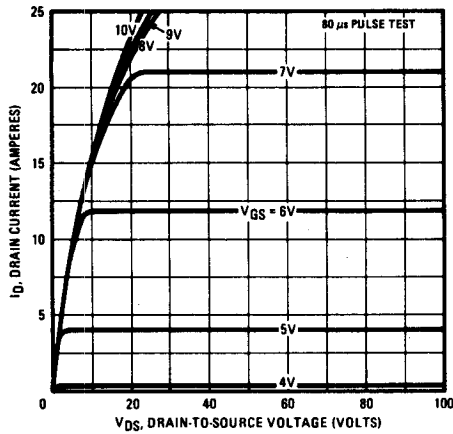


Fig. 1 - Typical Output Characteristics

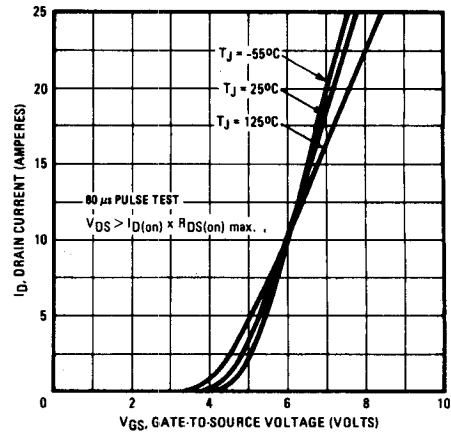


Fig. 2 - Typical Transfer Characteristics

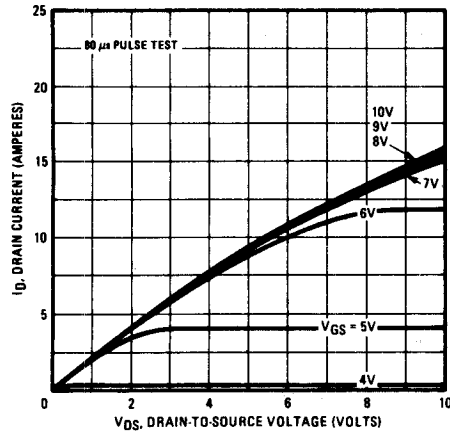


Fig. 3 - Typical Saturation Characteristics

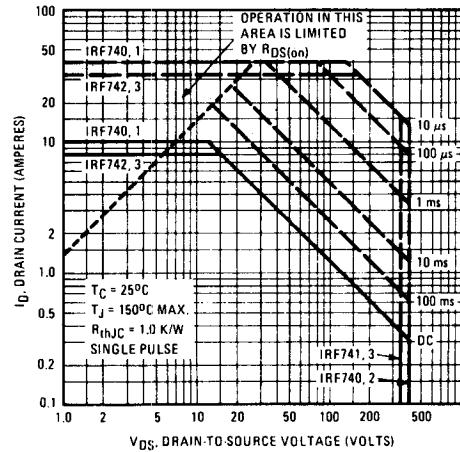


Fig. 4 - Maximum Safe Operating Area

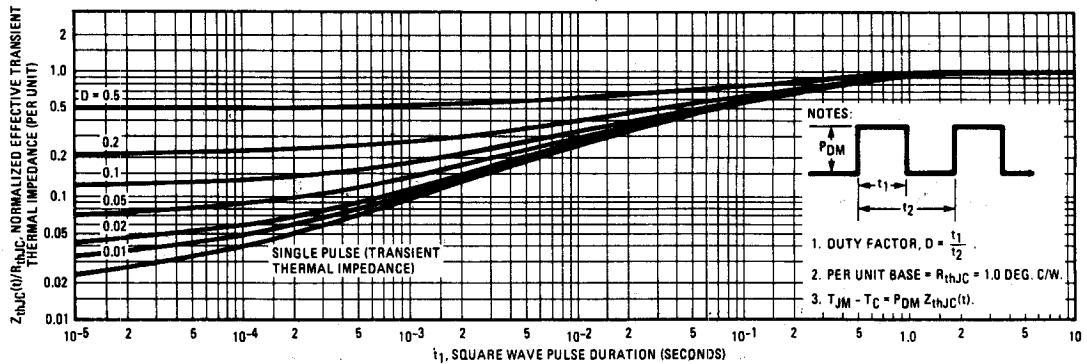


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF740, IRF741, IRF742, IRF743

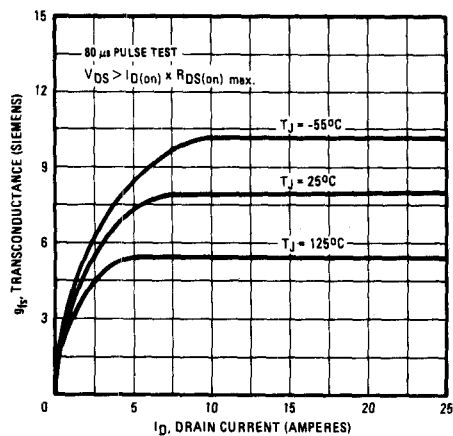


Fig. 6 - Typical Transconductance Vs. Drain Current

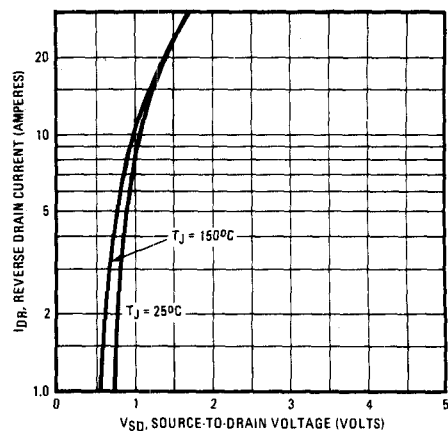


Fig. 7 - Typical Source-Drain Diode Forward Voltage

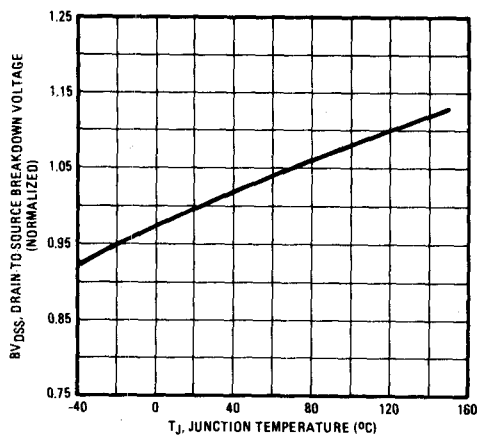


Fig. 8 - Breakdown Voltage Vs. Temperature

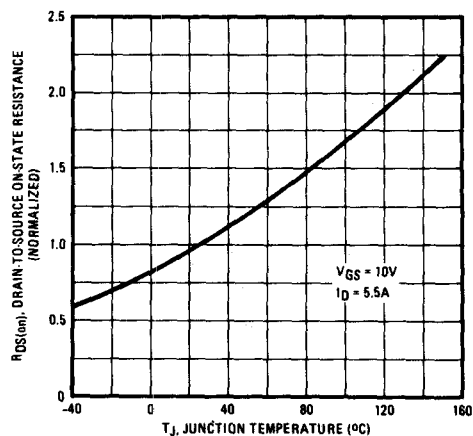


Fig. 9 - Normalized On-Resistance Vs. Temperature

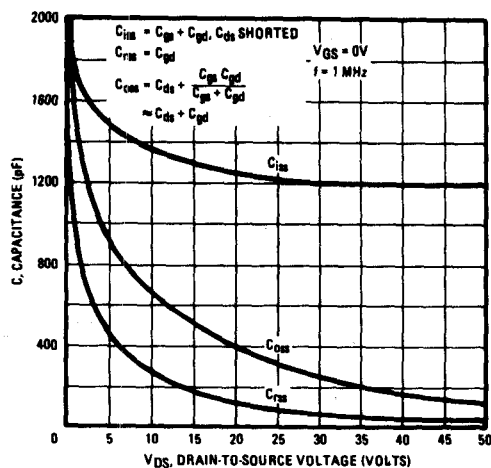


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

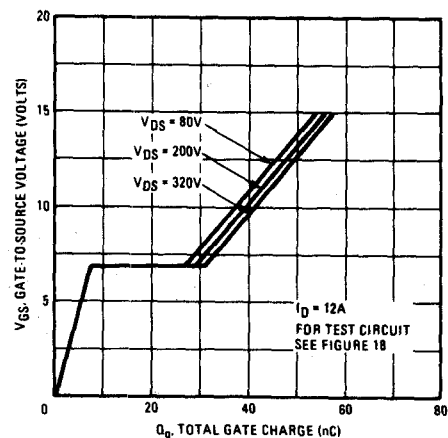


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRF740, IRF741, IRF742, IRF743

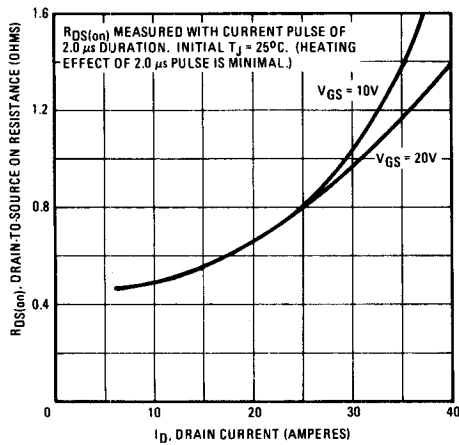


Fig. 12 – Typical On-Resistance Vs. Drain Current

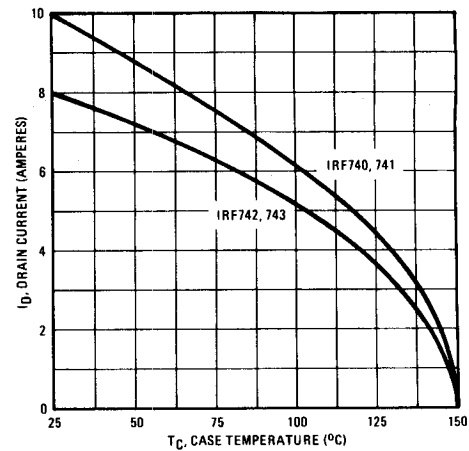


Fig. 13 – Maximum Drain Current Vs. Case Temperature

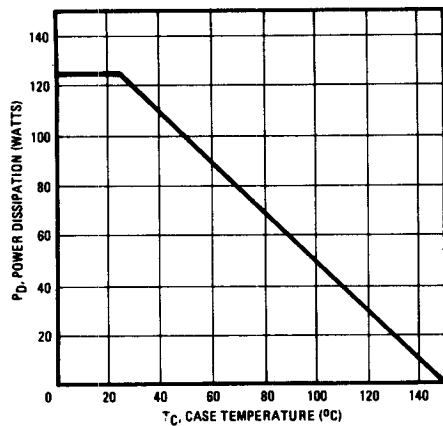


Fig. 14 – Power Vs. Temperature Derating Curve

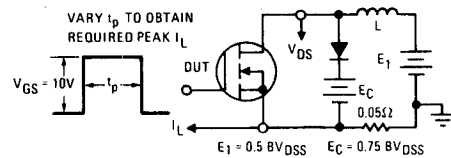


Fig. 15 – Clamped Inductive Test Circuit

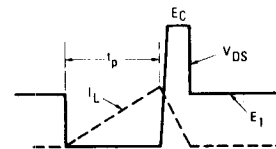


Fig. 16 – Clamped Inductive Waveforms

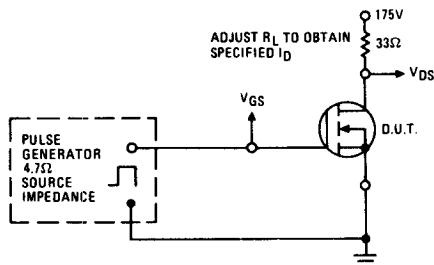


Fig. 17 – Switching Time Test Circuit

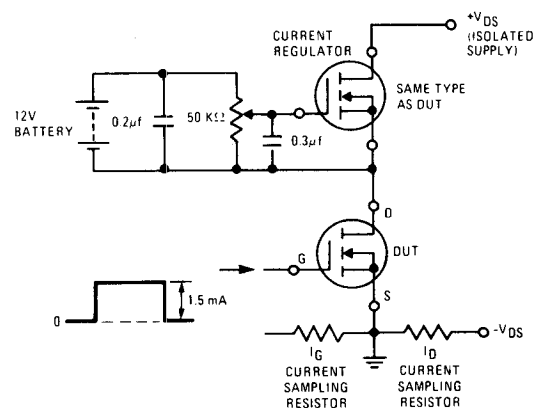


Fig. 18 – Gate Charge Test Circuit