
HM628512A Series

524288-word \times 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-640A (Z)

Rev. 1.0

Dec. 2, 1996

Description

The Hitachi HM628512A is a 4-Mbit static RAM organized 512-kword \times 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 μ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512A is suitable for battery backup system.

Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 50 mW/MHz (typ)
 - Standby: 10 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

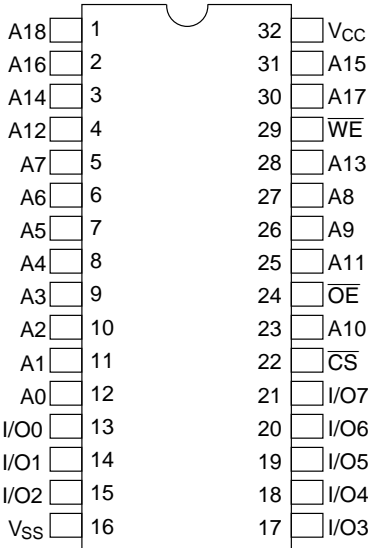
HM628512A Series

Ordering Information

Type No.	Access time	Package
HM628512ALP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512ALP-7	70 ns	
HM628512ALP-5SL	55 ns	
HM628512ALP-7SL	70 ns	
HM628512ALFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512ALFP-7	70 ns	
HM628512ALFP-5SL	55 ns	
HM628512ALFP-7SL	70 ns	
HM628512ALTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512ALTT-7	70 ns	
HM628512ALTT-5SL	55 ns	
HM628512ALTT-7SL	70 ns	
HM628512ALRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512ALRR-7	70 ns	
HM628512ALRR-5SL	55 ns	
HM628512ALRR-7SL	70 ns	

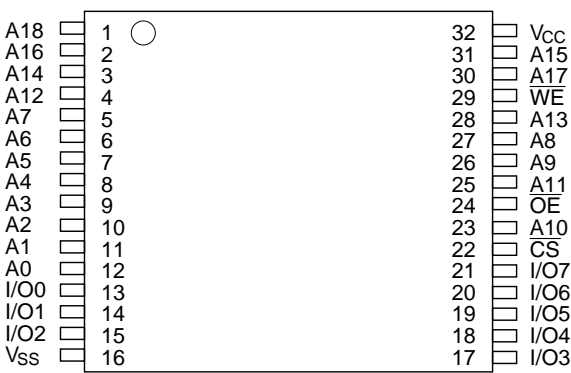
Pin Arrangement

HM628512ALP Series
HM628512ALFP Series



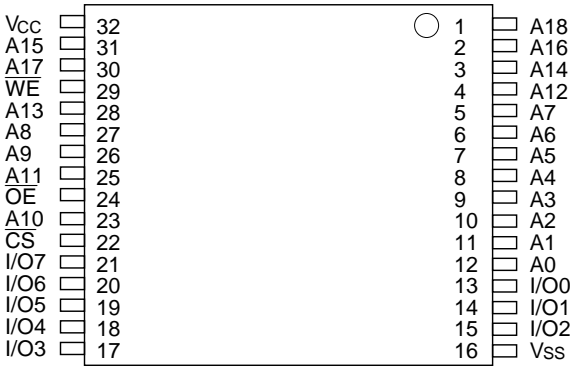
(Top view)

HM628512ALTT Series



(Top view)

HM628512ALRR Series

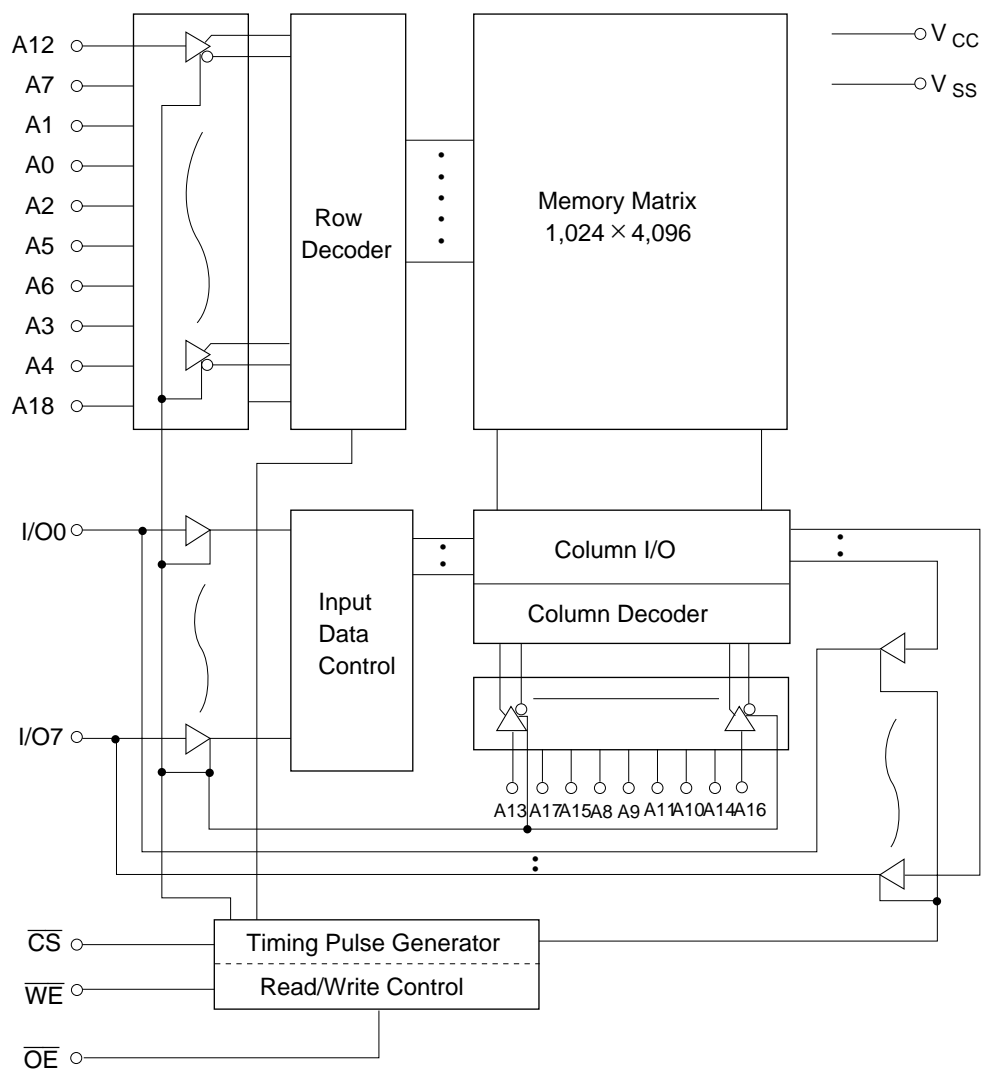


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

\overline{WE}	\overline{CS}	\overline{OE}	Mode	V_{CC} current	Dout pin	Ref. cycle
×	H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	−0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−10 to +85	°C

Notes: 1. −3.0 V for pulse half-width ≤ 30 ns

2. Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	−0.3* ¹	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10% , V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	8	15	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	HM628512A-5 I _{CC1}	—	45	70	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{I/O} = 0 mA
	HM628512A-7 I _{CC1}	—	40	60	mA	
Operating power supply current	I _{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100% I _{I/O} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} − 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I _{SB1}	—	2*2	100*2	μA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2*3	50*3	μA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = −1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance*1	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance*1	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512A-7)
1 TTL Gate + C_L (50 pF) (HM628512A-5)
(Including scope & jig)

Read Cycle

		HM628512A					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{CO}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	35	ns	
Chip selection to output in low-Z	t _{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	ns	

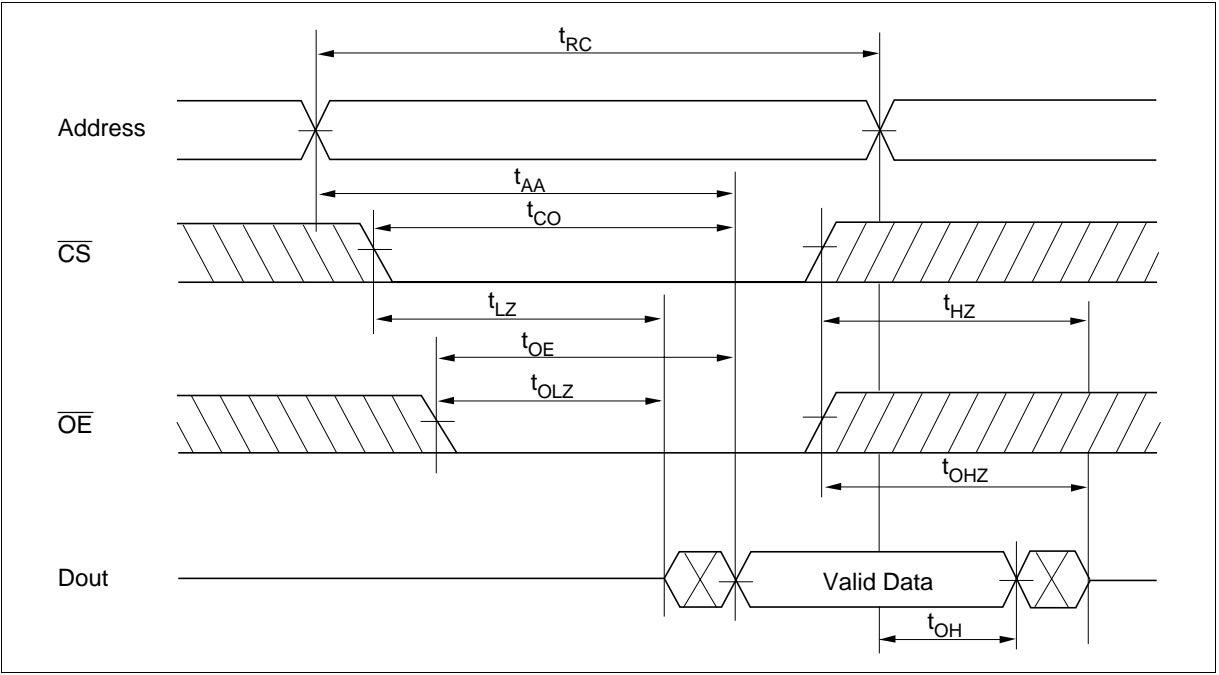
Write Cycle

		HM628512A					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	4
Address setup time	t _{AS}	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Write pulse width	t _{WP}	40	—	50	—	ns	3, 12
Write recovery time	t _{WR}	0	—	0	—	ns	6
\overline{WE} to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from output in high-Z	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 7

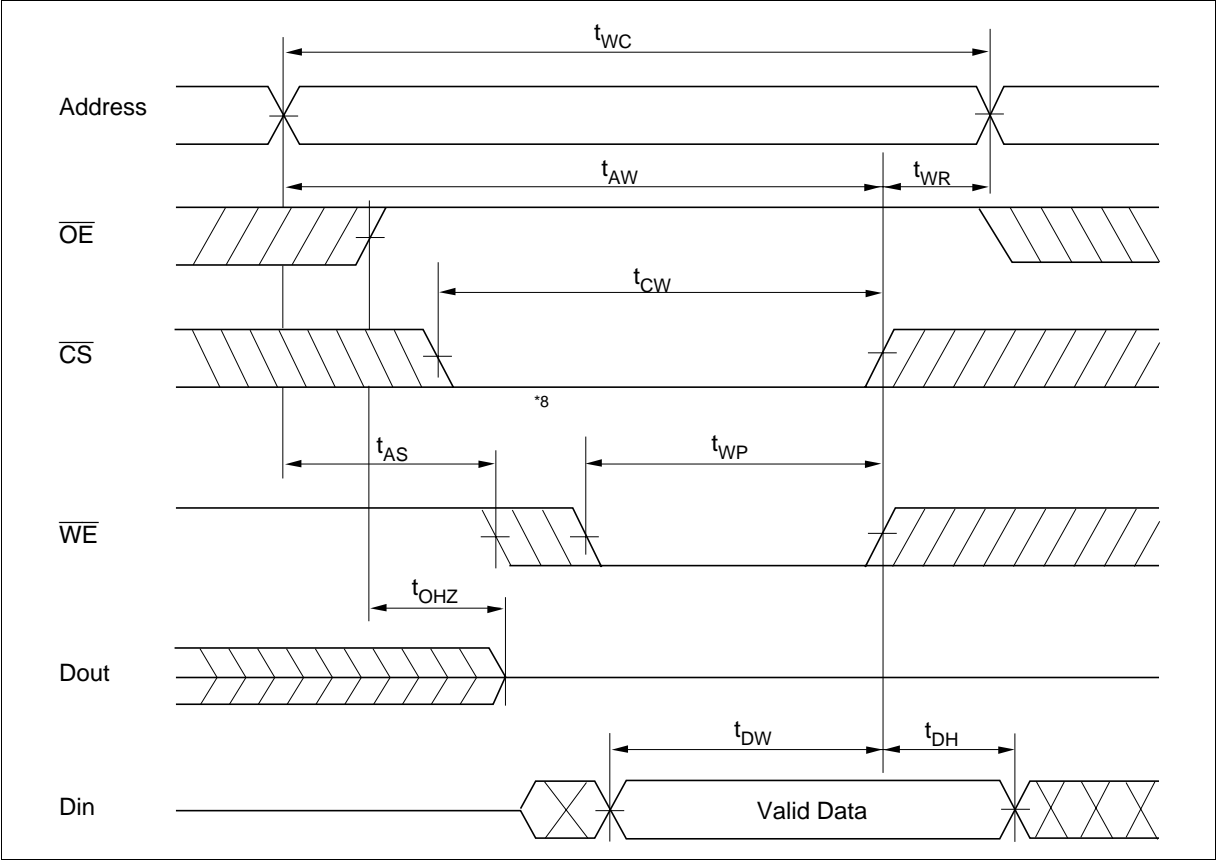
- Notes:
- 1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - 2. This parameter is sampled and not 100% tested.
 - 3. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 - 4. t_{CW} is measured from \overline{CS} going low to the end of write.
 - 5. t_{AS} is measured from the address valid to the beginning of write.
 - 6. t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.
 - 7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 - 8. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output remain in a high impedance state.
 - 9. Dout is the same phase of the write data of this write cycle.
 - 10. Dout is the read data of next address.
 - 11. If CS is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 - 12. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. t_{WP} ≥ t_{DW} min + t_{WHZ} max

Timing Waveforms

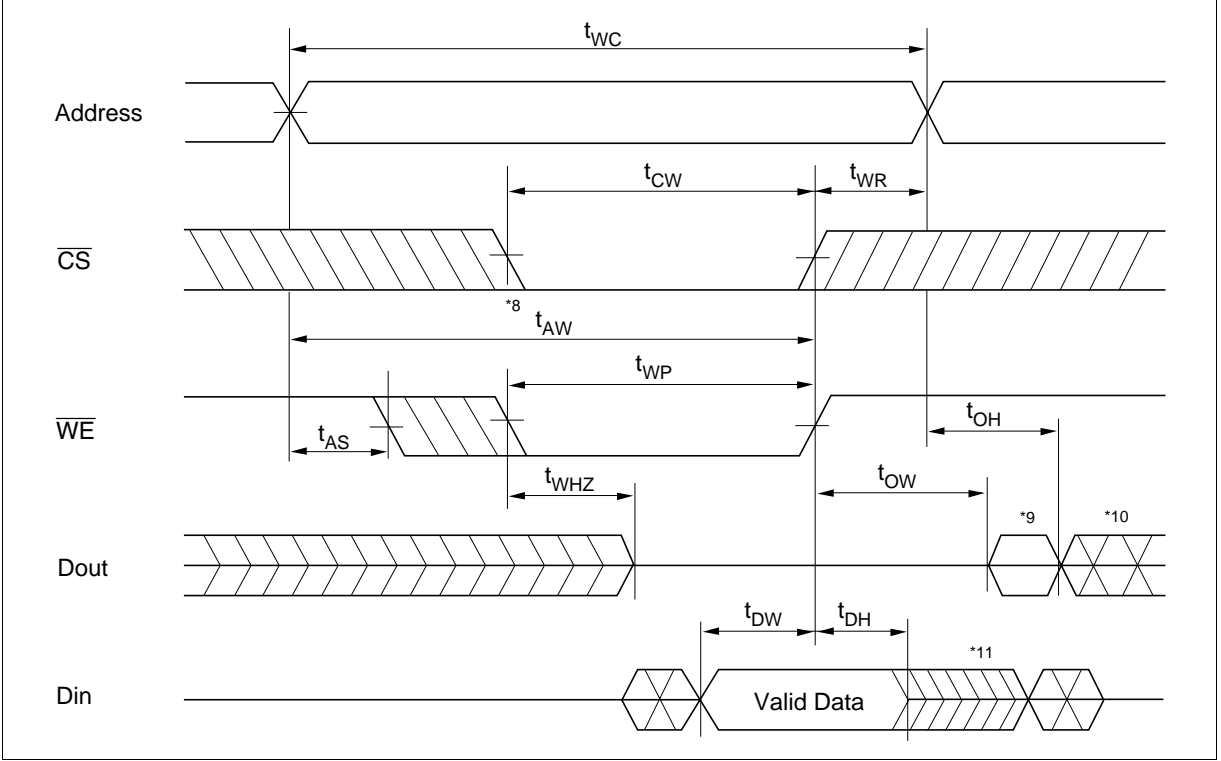
Read Timing Waveform ($\overline{WE} = V_{IH}$)



Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

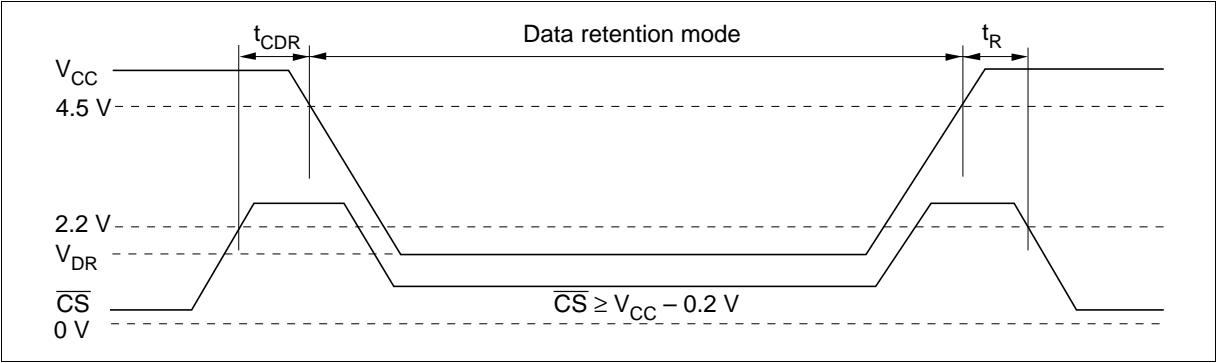


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*3
V _{CC} for data retention	V _{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, Vin ≥ 0 V
Data retention current	I _{CCDR}	—	1*4	50*1	μA	V _{CC} = 3.0 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	1*4	15*2	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5	—	—	ms	

Notes: 1. For L-version and 20 μA (max.) at Ta = 0 to 40°C.
2. For SL-version and 3 μA (max.) at Ta = 0 to 40°C.
3. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and Din buffer. In data retention mode, Vin levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
4. Typical values are at V_{CC} = 3.0 V, Ta = 25°C and specified loading, and not guaranteed.

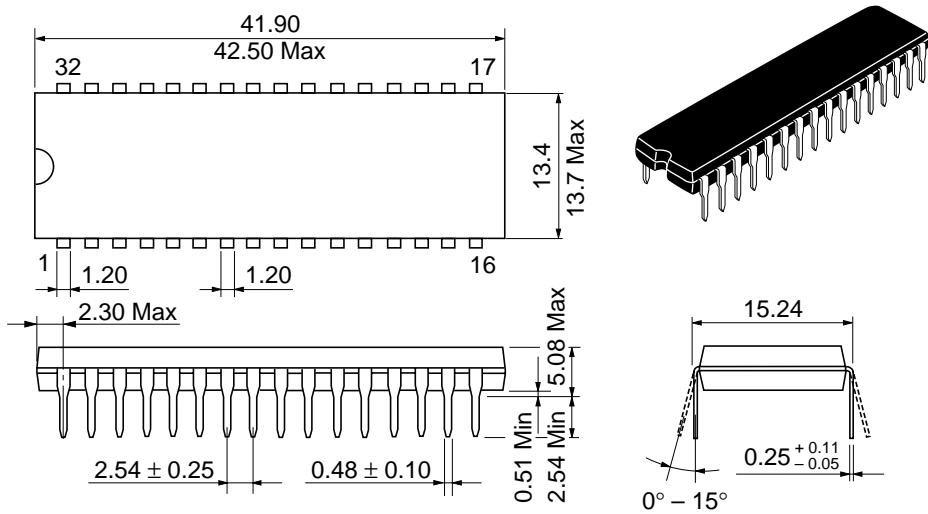
Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)



Package Dimensions

HM628512ALP Series (DP-32)

Unit: mm

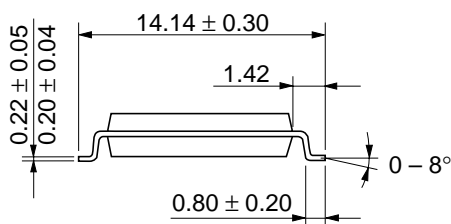
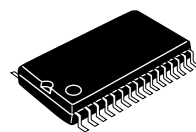
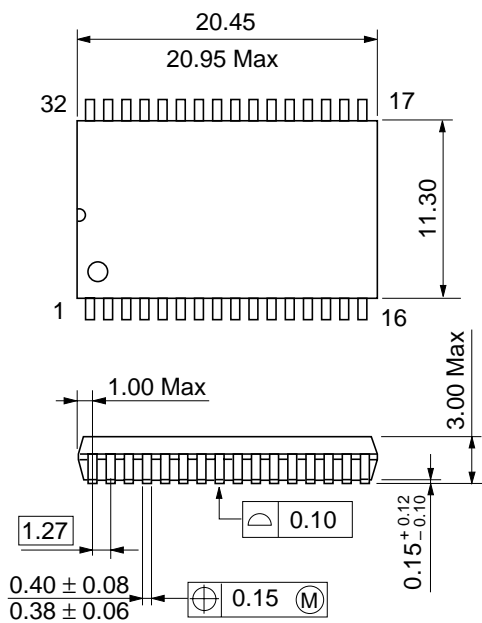


Hitachi Code	DP-32
JEDEC Code	—
EIAJ Code	SC-613
Weight	5.1 g

HM628512A Series

HM628512ALFP Series (FP-32D)

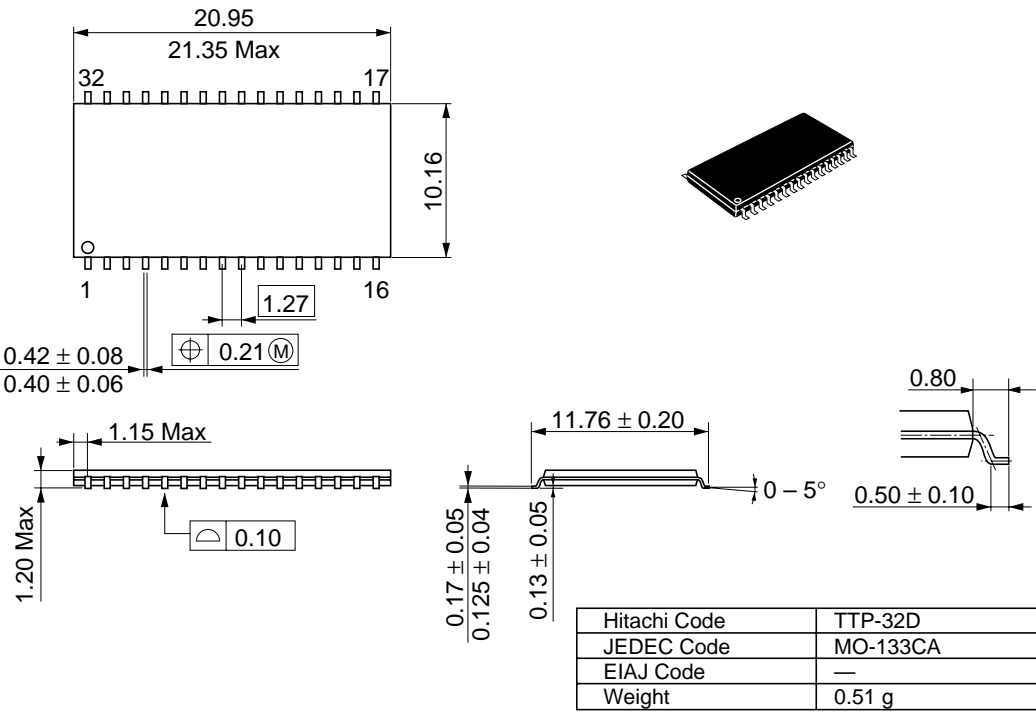
Unit: mm



Hitachi Code	FP-32D
JEDEC Code	—
EIAJ Code	—
Weight	1.3 g

HM628512ALTT Series (TTP-32D)

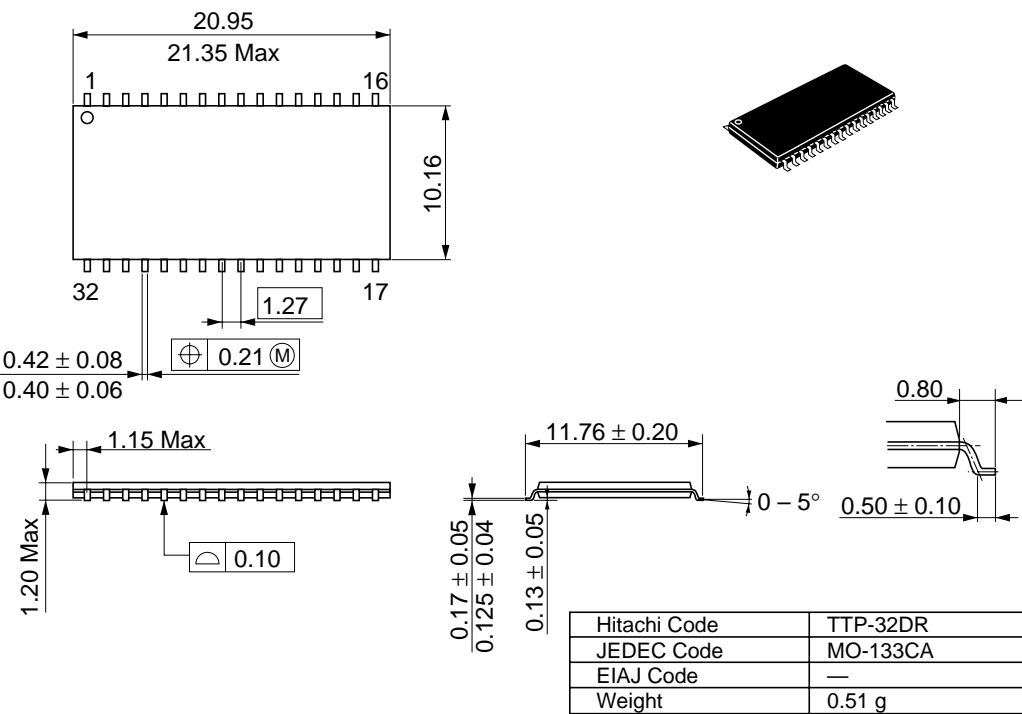
Unit: mm



HM628512A Series

HM628512ALRR Series (TTP-32DR)

Unit: mm



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Domacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 12, 1996	Initial issue	K. Imato	K. Imato
1.0	Dec. 2, 1996	Deletion of preliminary		