

# HD74LV157A

## Quad. 2-to-1 line Data Selectors / Multiplexers (Noninverted Outputs)

REJ03D0318-0200Z  
(Previous ADE-205-263 (Z))  
Rev.2.00  
Jun. 03, 2004

### Description

The HD74LV157A has four 2-input digital multiplexers with common select and strobe inputs. When the strobe input is low, a 4-bit word is selected from one of two sources and is routed to the four outputs.

The device provides true data.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}$  (Max.) =  $5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.3\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  (@  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV157AFPEL	SOP-16 pin(JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV157ARPEL	SOP-16 pin(JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV157ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

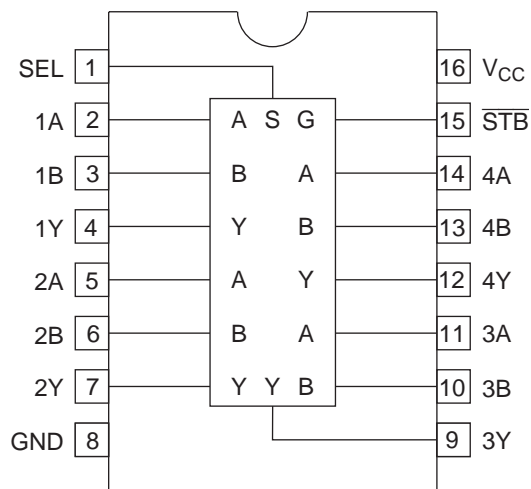
Note: Please consult the sales office for the above package availability.

### Function Table

Inputs				
STB	SEL	A	B	Output
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note: H: High level  
L: Low level  
X: Immaterial

## Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L $V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* <sup>3</sup>	$P_T$	785 500	mW	SOP TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

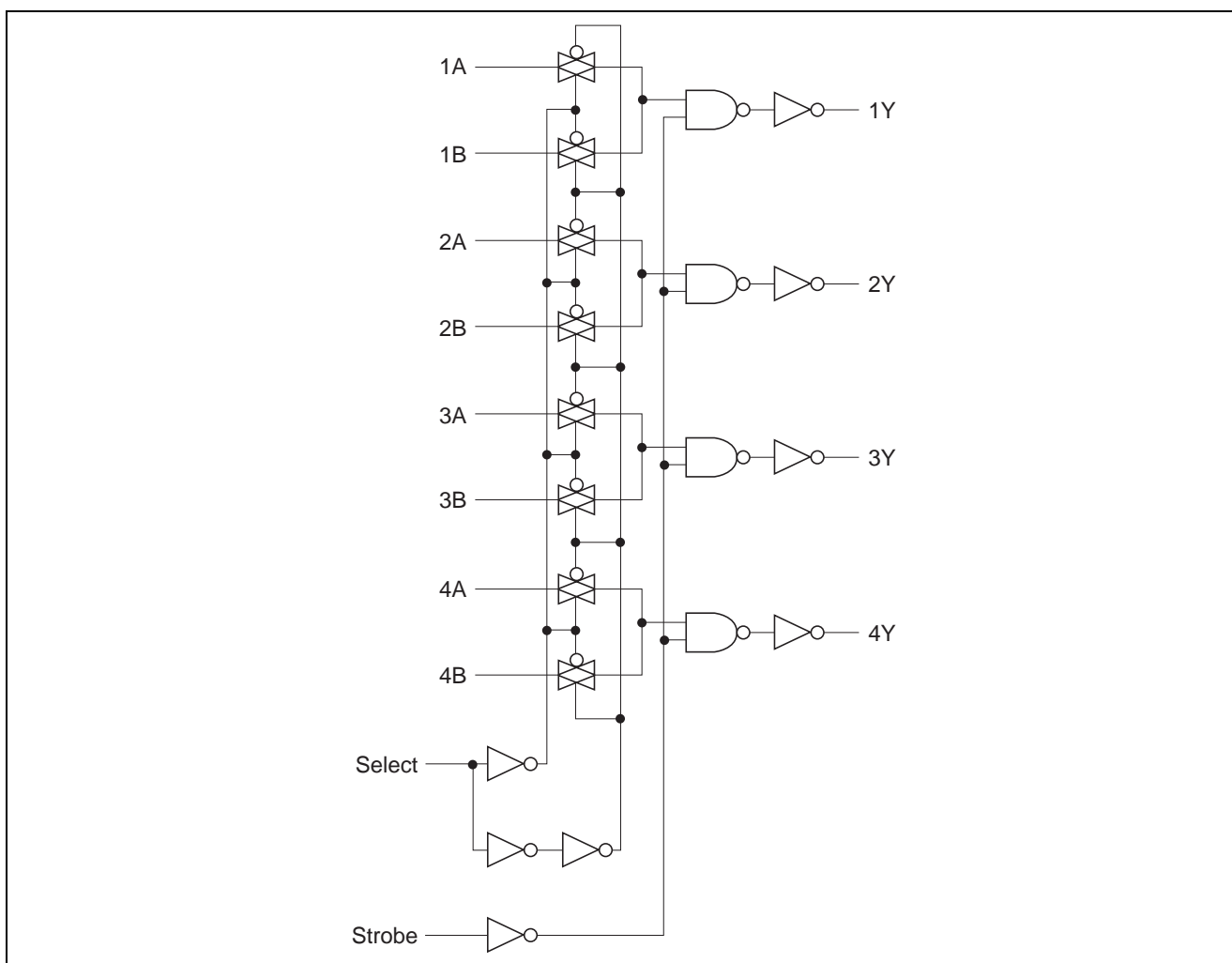
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

# Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	H or L
Output current	$I_{OH}$	—	−50	$\mu A$	$V_{CC} = 2.0 V$
		—	−2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	−6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	−12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	$I_{OL}$	—	50	$\mu A$	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t/\Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	$T_a$	−40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

# Logic Diagram



## DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V <sub>CC</sub> (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	V	
		2.3 to 2.7	V <sub>CC</sub> × 0.7	—	—		
		3.0 to 3.6	V <sub>CC</sub> × 0.7	—	—		
		4.5 to 5.5	V <sub>CC</sub> × 0.7	—	—		
	V <sub>IL</sub>	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V <sub>CC</sub> × 0.3		
		3.0 to 3.6	—	—	V <sub>CC</sub> × 0.3		
		4.5 to 5.5	—	—	V <sub>CC</sub> × 0.3		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> - 0.1	—	—	V	I <sub>OH</sub> = -50 μA
		2.3	2.0	—	—		I <sub>OH</sub> = -2 mA
		3.0	2.48	—	—		I <sub>OH</sub> = -6 mA
		4.5	3.8	—	—		I <sub>OH</sub> = -12 mA
	V <sub>OL</sub>	Min to Max	—	—	0.1		I <sub>OL</sub> = 50 μA
		2.3	—	—	0.4		I <sub>OL</sub> = 2 mA
		3.0	—	—	0.44		I <sub>OL</sub> = 6 mA
		4.5	—	—	0.55		I <sub>OL</sub> = 12 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1	μA	V <sub>I</sub> = 5.5 V or GND
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	20	μA	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
Output leakage current	I <sub>OFF</sub>	0	—	—	5	μA	V <sub>I</sub> or V <sub>O</sub> = 0 V to 5.5 V
Input capacitance	C <sub>IN</sub>	3.3	—	1.9	—	pF	V <sub>I</sub> = V <sub>CC</sub> or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

 $V_{CC} = 2.5 \pm 0.2 \text{ V}$ 

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}/t_{PHL}$	—	9.8	15.9	1.0	19.5	ns	$C_L = 15 \text{ pF}$	A or B	Y
		—	13.3	18.8	1.0	22.0		$C_L = 50 \text{ pF}$		
		—	15.5	19.4	1.0	23.5		$C_L = 15 \text{ pF}$	SEL	
		—	15.7	22.3	1.0	26.0		$C_L = 50 \text{ pF}$		
		—	15.8	19.8	1.0	24.0		$C_L = 15 \text{ pF}$	$\overline{\text{STB}}$	
		—	14.8	22.7	1.0	26.5		$C_L = 50 \text{ pF}$		

 $V_{CC} = 3.3 \pm 0.3 \text{ V}$ 

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}/t_{PHL}$	—	6.2	9.7	1.0	11.5	ns	$C_L = 15 \text{ pF}$	A or B	Y
		—	8.7	13.2	1.0	15.0		$C_L = 50 \text{ pF}$		
		—	8.4	13.2	1.0	15.5		$C_L = 15 \text{ pF}$	SEL	
		—	10.9	16.7	1.0	19.0		$C_L = 50 \text{ pF}$		
		—	8.7	13.6	1.0	16.0		$C_L = 15 \text{ pF}$	$\overline{\text{STB}}$	
		—	11.2	17.1	1.0	19.5		$C_L = 50 \text{ pF}$		

 $V_{CC} = 5.0 \pm 0.5 \text{ V}$ 

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}/t_{PHL}$	—	4.1	6.4	1.0	7.5	ns	$C_L = 15 \text{ pF}$	A or B	Y
		—	5.6	8.4	1.0	9.5		$C_L = 50 \text{ pF}$		
		—	5.3	8.1	1.0	9.5		$C_L = 15 \text{ pF}$	SEL	
		—	6.8	10.1	1.0	11.5		$C_L = 50 \text{ pF}$		
		—	5.6	8.6	1.0	10.0		$C_L = 15 \text{ pF}$	$\overline{\text{STB}}$	
		—	7.1	10.6	1.0	12.0		$C_L = 50 \text{ pF}$		

## Operating Characteristics

 $C_L = 50 \text{ pF}$ 

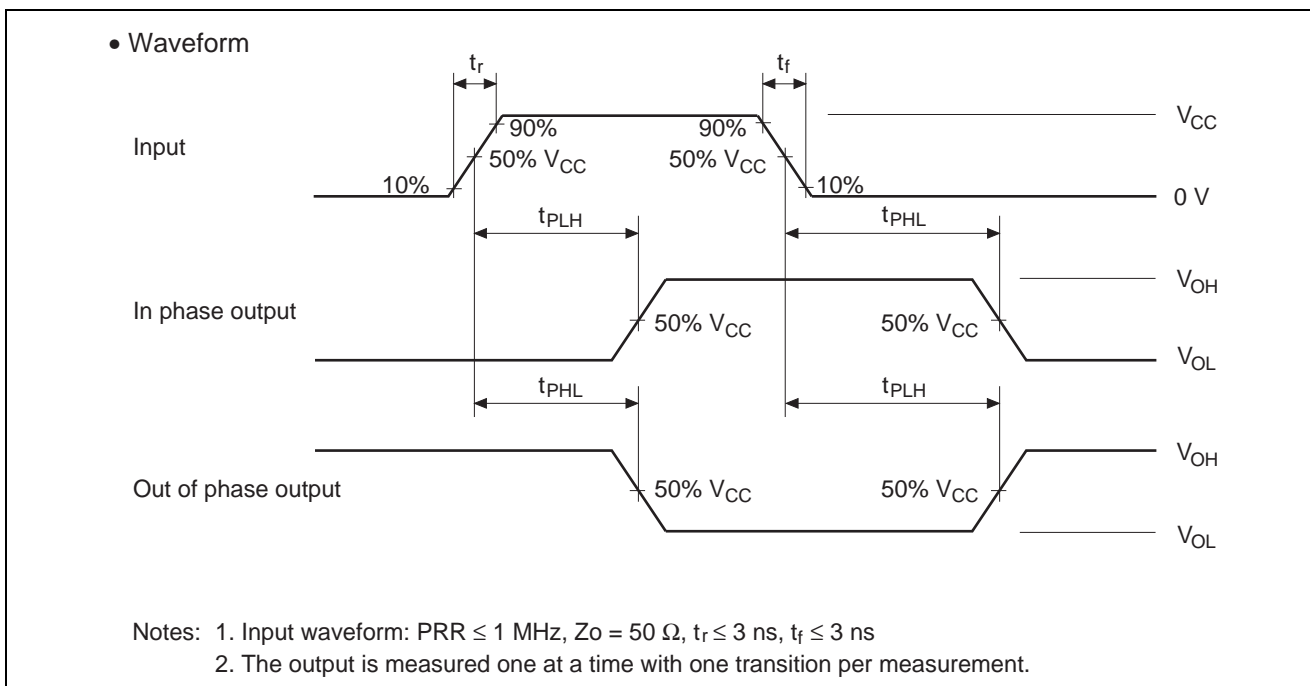
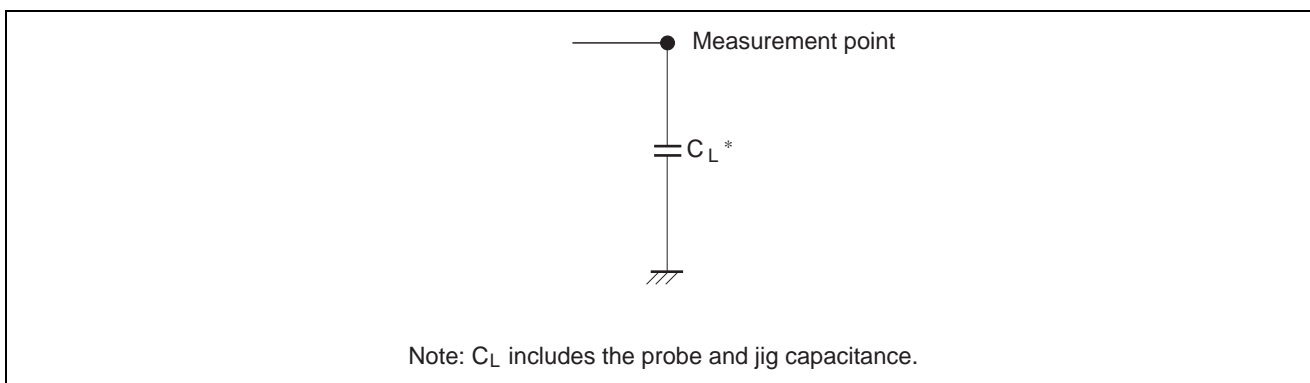
Item	Symbol	$V_{CC} \text{ (V)}$	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	3.3	—	10.0	—	pF	$f = 10 \text{ MHz}$
		5.0	—	12.0	—		

# Noise Characteristics

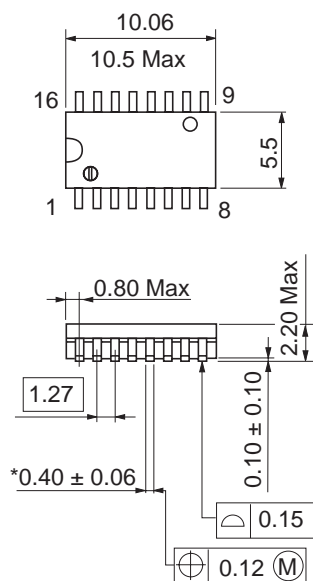
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic $V_{OL}$	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic $V_{OL}$	$V_{OL(V)}$	3.3	—	-0.2	-0.8	V	
Quiet output, minimum dynamic $V_{OH}$	$V_{OH(V)}$	3.3	—	3.0	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

## Test Circuit



Unit: mm



Technical drawing of the 7805C voltage regulator showing a top view and a side view with dimensions.

**Top View Dimensions:**

- Overall width:  $7.80^{+0.20}_{-0.30}$
- Pin pitch (distance between pins):  $1.15$
- Pin width:  $0.70 \pm 0.20$

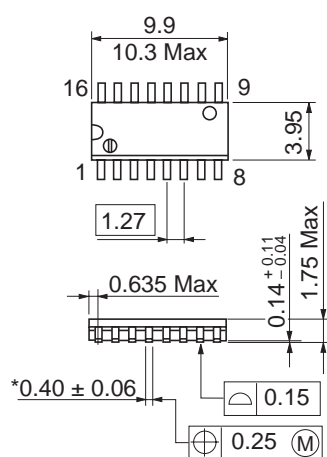
**Side View Dimensions:**

- Maximum height:  $0.20 \pm 0.05$
- Lead angle:  $0^\circ - 8^\circ$

An isometric view of the component is shown in the top right corner.

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

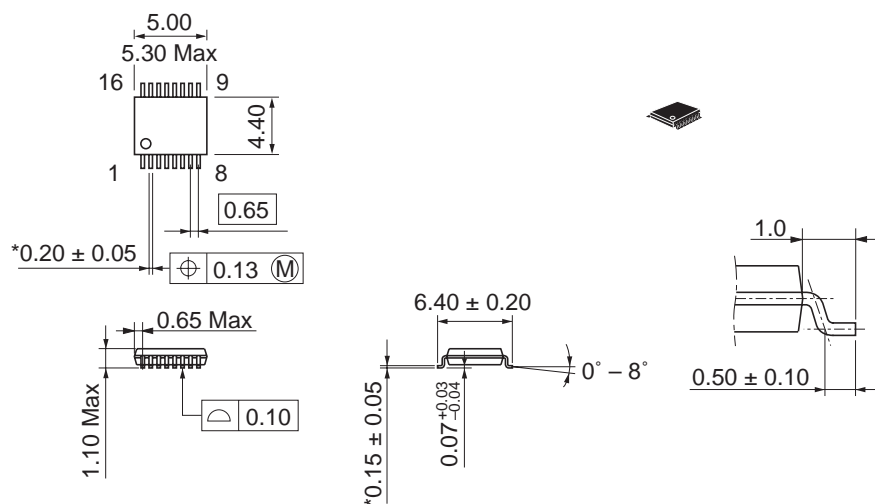
Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of January, 2003

Unit: mm



\*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g



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