AD1884A
High Definition Audio SoundMAX Codec

Data Sheet

DSH-202013B
February 2009

CONEXANT

Ordering Information

Device Set Order ID	Package Type	Package	Operating Temperature
AD1884AJCPZ*	QFN	48-Lead QFN	0°C to 70°C
*Lead-free (Pb Free) and RoHS compliant			

Revision History

Revision	Date	Description
A	February 25, 2009	Initial release
B	February 25, 2009	Revision B release: *Removed “Proprietary and Confidential” footer.

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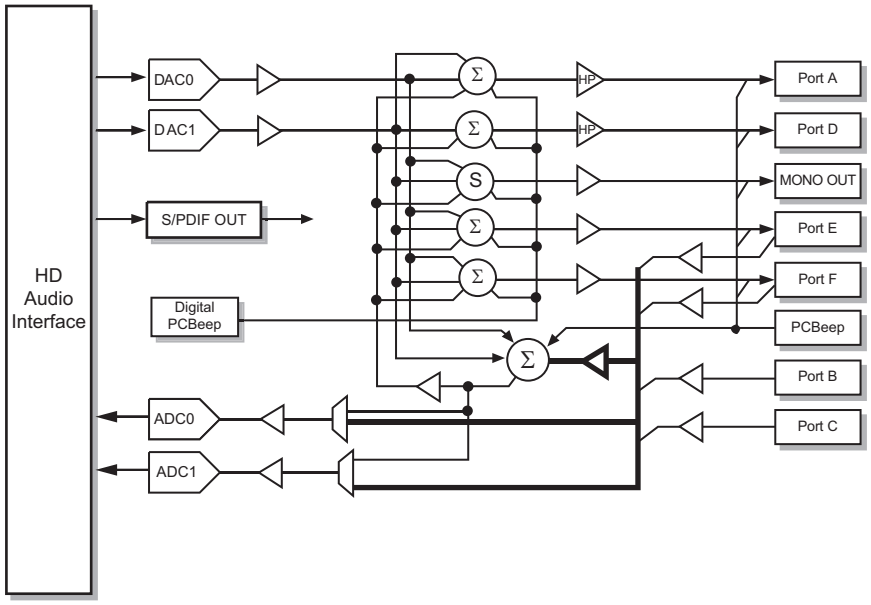
AD1884A

High Definition Audio SoundMAX Codec

The AD1884A audio codec and SoundMAX® software provide superior high definition audio quality that exceeds Vista Premium performance for notebooks. The AD1884A has two 192 kHz DAC pairs, two 192 kHz ADC pairs, an S/PDIF output, and digital and analog PCBeep. These features make the AD1884A the right choice for notebook PCs that meet Microsoft Vista Premium performance as well as desktop PCs that meet Microsoft Vista Basic performance.

The AD1884A is available in a 48-lead, RoHS compliant lead frame chip scale package in both reels and trays. See the Ordering Information table on the previous page.

Functional Block Diagram



Distinguishing Features

- Microsoft Vista Premium Logo for notebook
  - 90+ dB audio outputs, 85 dB audio inputs
  - WLP 3.0 and 4.0
- 2 stereo headphone amplifiers
- Internal 32-bit arithmetic for greater accuracy
- Impedance and presence detection on all jacks
- Full analog mixer with DAC inputs
- 3 independent microphone bias pins
- Digital and analog PCBeep
- 3 general-purpose digital I/O (GPIO) pins
- 3.3 V analog supply voltage
- 1.7 V to 1.9 V or 3.3 V digital supply voltages
- 1.5 V or 3.3 V HD Audio link signaling voltage
- Advanced power management modes
- 48-lead, RoHS compliant QFN package
- S/PDIF Output
  - Supports 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
  - 16-, 20-, and 24-bit data; PCM and AC3 formats
  - Digital PCM gain control
- 192 kHz DACs/ADCs
  - 2 independent stereo DAC/ADC pairs
  - Simultaneous record of 2 stereo channels
  - Simultaneous playback of 2 stereo channels
  - Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
  - 16-, 20-, and 24-bit resolution
  - Selectable stereo mixer on outputs
- Auxiliary Pins
  - Stereo CD/auxiliary I/O port with ground sense
  - Stereo auxiliary/dock I/O port
  - Mono out pin for internal speakers or telephony

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High Definition Audio SoundMAX Codec

This data sheet provides a general overview of the architecture and functionality of the AD1884A SoundMAX codec. Detailed widget information is available in the *AD1884A Programmers Reference Manual.* Please contact your local Conexant sales representative for more information.

1.1 Jack Configuration

Use the guidelines shown in Tables 1 through 3 when selecting ports for particular functions.

Table 1. Typical Desktop Configuration

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Microphone
Port D	Rear Panel Line-Out/Headphone
S/PDIF Out	Optical/RCA S/PDIF Output

Table 2. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port F	Internal Stereo Speakers
S/PDIF Out	Optical/RCA S/PDIF Output

Table 3. Typical Notebook Configuration with Dock Interface

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Dock Line-Out/Headphone
Port E	Dock Line-In/Microphone
Port F	Internal Stereo Speakers
S/PDIF Out	Optical/RCA S/PDIF Output

1.2 Specifications

Table 4. Test Conditions

Parameter	Test Condition
Temperature Digital Supply Analog Supply MIC_BIAS_IN (via Low-Pass Filter) Sample Rate f_S Input Signal (Frequency Sine Wave) Amplitude for THD + N Analog Output Pass Band	25°C 3.3 V 3.3 V 5.0 V 48 kHz 1008 Hz –3.0 dB Full Scale 20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

Table 5. Performance

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 kΩ Loads—DAC to Pin) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in Ref to f_S A-Weighted) Signal-to-Noise Ratio		 –84 90 90		 dB dB dB
Headphone Drive (32 Ω Loads—DAC to Pin) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in Ref to f_S A-Weighted) Signal-to-Noise Ratio		 –74 90 90		 dB dB dB
Microphone/Line-In (Pin to ADC, Mic Boost = 0 dB) Total Harmonic Distortion (THD + N) Dynamic Range (–60 dB in Ref to f_S A-Weighted) Signal-to-Noise Ratio		 –78 85 85		 dB dB dB

***Table 6. General Specifications** (1 of 4)*

Parameter	Min	Typ	Max	Unit
Digital Decimation and Interpolation Filters—f_S = 8 kHz to 192 kHz(1)				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection			–100	dB
Group Delay		+20		$1/f_S$
Group Delay Variation Over Pass Band		0		µs
Analog-to-Digital Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)(2)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error(1)			±5	mV
ADC Crosstalk(1)				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line_In to Other		–100	–80	dB
Digital to Analog Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)(1)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
Total Audible Out-of-Band Energy (Measured from 0.6 x f_s to 20 kHz)(1)		–85		dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)(1)		–95		dB
DAC Volumes				
Step Size		1.5		dB
Output Gain/Attenuation Range	–58.5		0	dB
Mute Attenuation of 0 dB Fundamental(1)		–80		dB

Table 6. General Specifications *(2 of 4)*

Parameter		Min	Typ	Max	Unit
ADC Volumes					
Step Size			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
Analog Mixer					
Signal-to-Noise Ratio Input to Output—Ports B, C, E, or F to Port D Output		90		dB	dB
Step Size: All Mixer Inputs			1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
Analog Line Level Outputs					
Full-Scale Output Voltage		1.0			Vrms
Ports A, D, E, F, and Mono Out		2.83			V p-p
	Output Impedance(1)		190		Ω
	External Load Impedance(1)	10			kΩ
	Output Capacitance(1)		15		pF
	External Load Capacitance(1)			1000	pF
Analog HP Drive Outputs					
Full-Scale Output Voltage		1.0			Vrms
Ports A and D		2.83			V p-p
	Output Impedance(1)			0.5	Ω
	External Load Impedance(1)	32			Ω
	Output Capacitance(1)		15		pF
	External Load Capacitance(1)			1000	pF
Analog Inputs					
Input Voltages—Ports B, C, E, or F	Mic Boost = 0 dB		1 2.83		Vrms V p-p
Input Voltages—Microphone Boost Amplifier, Ports B, C, or E	Mic Boost = 10 dB		0.316 0.894		Vrms V p-p
	Mic Boost = 20 dB		0.1 0.283		Vrms V p-p
	Mic Boost = 30 dB		0.032 0.089		Vrms V p-p
Input Impedance					
PCBeep			23		kΩ
Ports B, C, E (Microphone Boost = 0 dB)			150		kΩ
Port F			45		kΩ
Input Capacitance(1)			5	7.5	pF

Table 6. General Specifications *(3 of 4)*

Parameter		Min	Typ	Max	Unit
MICROPHONE BIAS					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = 5 V or 3.3 V	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = 5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = 3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When Enabled as BIAS)	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA
GPIO 0					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
GPIO 1 and GPIO 2					
Input Signal High (V_{IH})		$AV_{DD} \times 0.60$		AV_{DD}	V
Input Signal Low (V_{IL})		0		$AV_{DD} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$AV_{DD} \times 0.72$		AV_{DD}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$AV_{DD} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA

Table 6. General Specifications *(4 of 4)*

Parameter		Min	Typ	Max	Unit
S/PDIF-Out					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
Power Supply					
Analog (AV_{DD}) 3.3 V ± 5% Power Supply Range Power Dissipation Supply Current		3.13	3.30 75.9 23	3.46	V mW mA
Digital (DV_{DD}) 3.3 V ± 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 141.9 43	3.63	V mW mA
Digital (DV_{CORE}) 1.7 V Through 1.9 V ± 10% Power Supply Range Power Dissipation Supply Current		1.615	1.70 61 36	1.995	V mW mA
Digital I/O (DV_{IO}) 3.3 V ± 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 3.3 1	3.63	V mW mA
Digital I/O (DV_{IO}) 1.5 V ± 5.5% Power Supply Range Power Dissipation Supply Current		1.418	1.50 0.08 0.05	1.583	V mW mA
Power Supply Rejection (Reference to f_S 100 mV p-p Signal @ 1 kHz)[1]			80		dB

FOOTNOTE:
[1] Guaranteed but not tested.

1.2.1 HD Audio Link Specifications

HD Audio signals comply with the High Definition Audio specifications. Please refer to these specifications at www.intel.com/standards/hdaudio.

Table 7. Power-Down States

Parameter	ID_{VDD} Typ (1.7 V)	ID_{VDD} Typ (3.3 V)	IA_{VDD} Typ	Unit
Function Node in D0, All Nodes Active	36	43	23	mA
Function Node in D3	15.75	17	1	mA
Function Node in D3[1]	7.5	7.5	1	mA
Codec in $\overline{\text{RESET}}$	3	3	3	mA
Individual Block Power Savings				
DAC Pair Powered Down Saves (Each)	4.5	6	5	mA
ADC Pair Powered Down Saves (Each)	4.5	6	3	mA
Mixer Power Control (and Associated Amps) Saves	0	0	2	mA
MIC_BIAS Powered Down Saves[2]	0	0	0.1	mA

FOOTNOTES:

(1) Maximum power saving mode; Register 0x31FD, Bit 4.

(2) Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the high-Z state. The 0 V and high-Z states remain unaffected by the MIC_BIAS power state.

1.2.2 Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Power Supplies	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital (DV_{CORE})	–0.30 V to +2.10 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} +0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} +0.3 V
Ambient Temperature (Operating)	0 °C to +70 °C
Storage Temperature	–65 °C to +150 °C

Electrostatic Discharge Device (ESD)

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

1.2.3 Environmental Conditions

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} – (PD \times \theta_{CA})$
T_{CASE} = case temperature in °C
PD = power dissipation in W
θ_{CA} = thermal resistance (case-to-ambient)
θ_{JA} = thermal resistance (junction-to-ambient)
θ_{JC} = thermal resistance (junction-to-case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
QFN	47	15	32	°C/W

1.3 Pin Configuration and Functional Descriptions

Figure 1. AD1884A Pinout

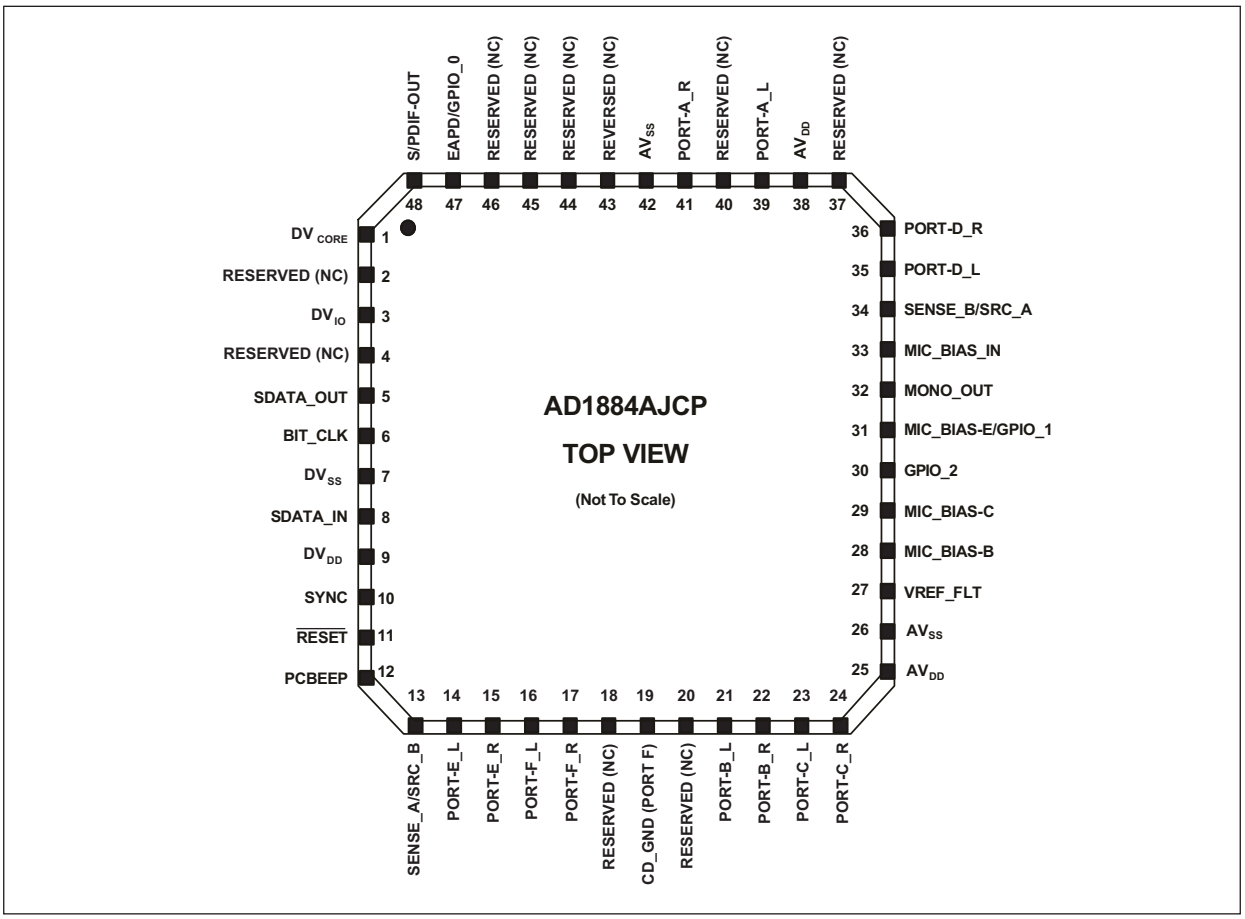


Table 9. Pin Descriptions *(1 of 2)*

Mnemonic	Pin No.	I/O	Description
Digital Interface			
SDATA_OUT	5	I	Link Serial Data Output. AD1884A input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1884A output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. AD1884A master hardware reset.
DIGITAL I/O and EAPD			
GPIO_2	30	I/O	General-Purpose Input/Output Pin. Digital signal used to control or sense external circuitry.
MIC_BIAS-E/GPIO_1	31	I/O	Microphone Bias for Port E/General-Purpose Input/Output. Capable of high-Z, 1.65 V, and 2.86 V. Pin 31 shares functionality between MIC_BIAS-E (default) and GPIO_1. These functions are mutually exclusive and the MIC_BIAS function takes priority over the GPIO function.
EAPD/GPIO_0	47	I/O	EAPD/General-Purpose Input/Output Pin. Pin 47 shares functionality between GPIO_0 and EAPD. These functions are mutually exclusive and the EAPD function takes priority over the GPIO function. By default, the pin is in a high-Z state. External resistors should be used to ensure the proper circuit state when this pin is in high-Z.
S/PDIF_OUT	48	O	Supports S/PDIF Output.
JACK SENSE			
SENSE_A/SRC_B	13	I/O	Jack Sense A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	I/O	Jack Sense E-F Input/Sense A Drive.
Analog I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO	Auxiliary Input/Output Right Channel.
PORT-F_L	16	LI, LO	Auxiliary Input/Output Left Channel.
PORT-F_R	17	LI, LO	Auxiliary Input/Output Right Channel.
CD_GND (PORT-F)	19	I	CD Audio Analog Ground Reference. Must be connected to AGND via a 0.1 μF capacitor if not in use as CD_GND. MUST always be ac-coupled.
PORT-B_L	21	LI, MIC	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC	Rear Panel Stereo MIC/Line-In.

Table 9. Pin Descriptions *(2 of 2)*

Mnemonic	Pin No.	I/O	Description
Analog I/O (continued)			
PORT-C_R	24	LI, MIC	Rear Panel Stereo MIC/Line-In.
MONO_OUT	32	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-D_L	35	HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	HP, LO	Front Panel Headphone/Line-Out.
PORT-A_R	41	HP, LO	Front Panel Headphone/Line-Out.
Filter/MIC_BIAS			
V_{REF} _FLT MIC_BIAS-B MIC_BIAS-C MIC_BIAS_IN 5.0 V or 3.3 V	27 28 29 33	O O O I	Voltage Reference Filter. Switchable Microphone Bias. For use with Port B (Pins 21, 22). Switchable Microphone Bias. For use with Port C (Pins 23, 24). Both MIC bias pins are capable of: High-Z, 0 V, 1.65 V, 3.7 V, and 3.9 V (with 5.0 V on Pin 33) High-Z, 0 V, 1.65 V, 2.86 V, and 3.0 V (with 3.3 V on Pin 33). Source Power for Microphone Bias Boost Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way, the AD1884A is capable of providing 3.9 V as a mic bias to all of the mic bias pins (except on Pin 31). If 5 V is not available, connect this pin to 3.3 V (AV_{DD}) via a low-pass filter.
Power and Ground			
DV_{CORE} 1.7 V to 1.9 V or FILTER	1	I/O	CAUTION: Do not apply 3.3 V to this pin! Filter connection for internal core voltage regulator. If Pin 9 is connected to 3.3 V DV_{DD}, this pin must be connected to filter caps: 10 µF, 1.0 µF, and 0.1µF connected in parallel between Pin 1 and DV_{SS} (Pin 7). Direct, filtered 1.7 V to 1.9 V DV_{DD} can be applied to Pin 1 to lower the digital power requirements. Pin 9 MUST be connected to Pin 1 in this case.
DV_{IO} 1.5 V or 3.3 V	3	I	Link Digital I/O Voltage Reference. 3.3 V ± 10% or 1.5 V ± 5.5%
DV_{SS}	7	I	Digital Supply Return (Ground).
DV_{DD} 1.7 V to 1.9 V or 3.3 V	9	I	Digital Supply Voltage 3.3 V ± 10%. This is regulated down to DV_{CORE} on Pin 1 to supply the internal digital core internal to the AD1884A. Direct, filtered 1.7 V to 1.9 V DV_{DD} can be applied to Pin 1 to lower the digital power requirements. Pin 9 MUST be connected to Pin 1 in this case.
AV_{DD} 3.3 V	25, 38	I	CAUTION: Do not apply 5 V to these pins! Analog Supply Voltage 3.3 V ± 5%. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1884A.

GENERAL NOTES:

1. The symbols used in this table are defined as follows:
   I = input
   O = output
   LI = line level input
   LO = line level output
   HP = output capable of driving headphone load
   MIC = input supports microphones with MIC bias and boost amplifier.

1.4 HD Audio Widgets

Table 10. HD Audio Widgets[1] *(1 of 2)*

Node ID	Name	Type ID	Type	Description
0x00	ROOT	x	Root	Device identification
0x01	FUNCTION	x	Function	Designates this device as an audio codec
0x02	S/PDIF DAC	0	Audio Output	S/PDIF digital stream output interface
0x03	DAC_0	0	Audio Output	Stereo headphone channel digital/audio converter
0x04	DAC_1	0	Audio Output	Stereo front channel digital/audio converter
0x07	Port A Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port A
0x08	ADC_0	1	Audio Input	Stereo record Channel 0 audio/digital converters
0x09	ADC_1	1	Audio Input	Stereo record Channel 1 audio/digital converters
0x0A	Port D Mixer	2	Audio Mixer	Mixes the DAC_1 and analog mixer output to drive Port D
0x0B	Port F Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port F
0x0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_0
0x0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_1
0x0E	Mono Out Selector	3	Audio Selector	Selects the mono out DAC_(0, 1)
0x0F	Port F Out Selector	3	Audio Selector	Selects the Port F DAC_(0, 1)
0x10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
0x11	Port A (Headphone)	4	Pin Complex	Headphone jack pins
0x12	Port D (Line Out)	4	Pin Complex	Line out jack pins
0x13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
0x14	Port B (Mic In)	4	Pin Complex	Microphone in jack pins
0x15	Port C (Line In)	4	Pin Complex	Line in jack pins
0x16	Port F (Aux In/Out)	4	Pin Complex	Auxiliary I/O pins
0x19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
0x1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
0x1B	S/PDIF_Out	4	Pin Complex	S/PDIF output pin
0x1C	Port E (Dock I/O)	4	Pin Complex	Analog dock I/O pins
0x1D	V_{REF} Power Down	F	Vendor Defined	Powers down the V_{REF} circuitry
0x1E	Mono Out Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive mono out

Table 10. HD Audio Widgets[1] (2 of 2)

Node ID	Name	Type ID	Type	Description
0x1F	Stereo Mix-Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
0x20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
0x21	Mixer Output Atten	3	Audio Selector	Attenuates the analog mixer output to drive the port mixers
0x22	Port A Out Selector	3	Audio Selector	Selects the Port A DAC_(0, 1)
0x23	Port E Out Selector	3	Audio Selector	Selects the Port E DAC_(0, 1)
0x24	Port E Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port E
0x25	Port E Mic Boost	3	Audio Selector	0 dB, 10 dB, 20 dB, or 30 dB gain boost for Port E
0x26	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS pins

FOOTNOTES:
(1) All node IDs (NIDs) are sequential in the codec. Any NIDs missing from this table are vendor defined.

1.5 HD Audio Parameters

The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 11. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	Revision ID 01[1]	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
0x00	ROOT	0x11D4 184A	0x0010 0100	0x0001 0001			
0x01	FUNCTION			0x0002 0029	0x0000 0001	0x0001 0C0C	0x4000 0003

FOOTNOTES:
(1) Subject to change with silicon stepping.

Table 12. SubSystem ID

Node ID	Name	Type	Value	31:16 SSID	15:8 SKU	7:0 Asm ID
0x01	FUNCTION	Function	0xBFD4 0000	0xBFD4	0x00	0x00

1.6 Default Configuration Bytes

Table 13. Default Configuration Bytes

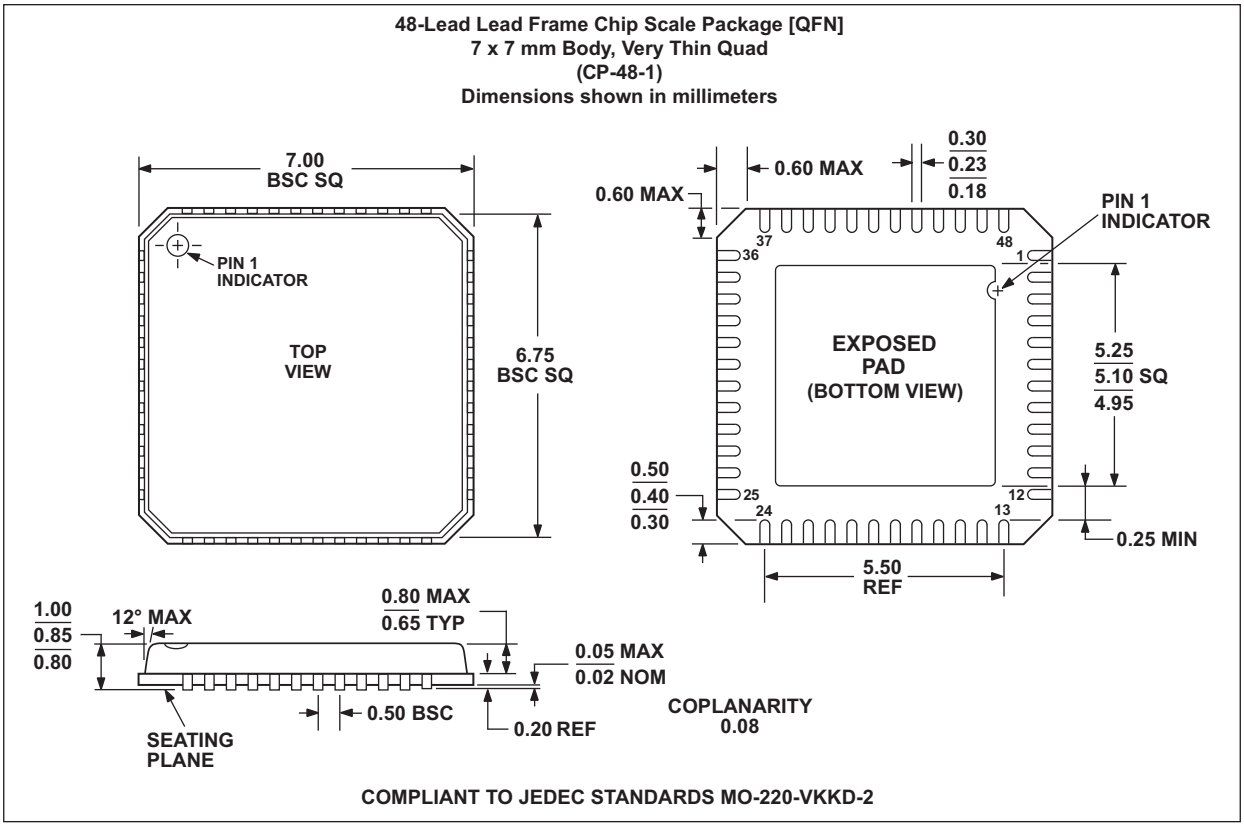
Node ID	Name	Value	31:30	29:28	27:24	23:20
			Connectivity	Location		Def. Device
				Chassis	Position	
0x11	Port A (Headphone)	0x0321 40F0	Jack	External	Left	HP Out
0x12	Port D (Line Out)	0x2121 4010	Jack	Separate	Rear	HP Out
0x13	Mono Out	0x9017 01F0	Fixed	Internal	N/A	Speaker
0x14	Port B (Mic In)	0x03A1 90F0	Jack	External	Left	Mic In
0x15	Port C (Line In)	0xB7A7 0121	Fixed	Other	Special 1	Mic In
0x16	Port F (Aux In/Out)	0x9933 012E	Fixed	Internal	Special 3	CD
0x1A	Analog PCBeep	0x90F3 01F0	Fixed	Internal	N/A	other
0x1B	S/PDIF Out	0x0145 10F0	Jack	External	Rear	SPDIF Out
0x1C	Port E (Dock I/O)	0x21A1 9020	Jack	Separate	Rear	Mic In

Node ID	Name	Value	19:16	15:12	8	7:4	3:0
			Conn Type	Color	JD OVRD	Def. Assn.	Sequence
0x11	Port A (Headphone)	0x0321 40F0	1/8” Jack	Green	0	0xF	0x0
0x12	Port D (Line Out)	0x2121 4010	1/8” Jack	Green	0	0x1	0x0
0x13	Mono Out	0x9017 01F0	Other Analog	Unknown	1	0xF	0x0
0x14	Port B (Mic In)	0x03A1 90F0	1/8” Jack	Pink	0	0xF	0x0
0x15	Port C (Line In)	0xB7A7 0121	Other Analog	Unknown	1	0x2	0x1
0x16	Port F (Aux In/Out)	0x9933 012E	ATAPI	Unknown	1	0x2	0xE
0x1A	Analog PCBeep	0x90F3 01F0	ATAPI	Unknown	1	0xF	0x0
0x1B	S/PDIF Out	0x0145 10F0	Optical	Black	0	0xF	0x0
0x1C	Port E (Dock I/O)	0x21A1 9020	1/8” Jack	Pink	0	0x2	0x0

1.7 Package Dimensions

Figure 2 provides the package dimensions, shown in millimeters

Figure 2. Package Dimensions



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