Video Input Processor (VIP) SAA7111

1 FEATURES

- Four analog inputs, internal analog source selectors, (e.g.: 4 x CVBS or 2 x YC or (1 x YC and 2xCVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS/Y channel
- Switchable white Peak Control
- Two built in analog anti-aliasing filters
- Two 8 bit Video CMOS AD Converters
- On-Chip Clock Generator
- Line-Locked System Clock Frequencies
- Digital PLL for H-Sync processing and Clock Generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical Sync Detection
- Automatic detection of 50/60Hz field frequency, and automatic switching between standards PAL and NTSC
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43
- User programmable luminance peaking or aperture correction'
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Realtime Status Information output (RTCO)
- Brightness Contrast Saturation (BCS)-control on chip
- The YUV (CCIR-601)-bus supports a data rate of:
  864 x fh = 13.5 MHz for 625 line sources
  858 x fh = 13.5 MHz for 525 line sources
- Data output streams for 16/12 or 8 bit width with the formats of
  411 YUV (12 Bit)
  422 YUV (16 Bit)
  422 YUV[CCIR-656](8 Bit)
  565 RGB (16 Bit) with dither
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Power On Control
- Two via I²C-bus switchable outputs for the digitized CVBS or Y/C input signals AD1[7-0] and AD2[7-0]
- Chip enable function (reset for the clock generator)
- Compatible with memory-based features (line-locked clock)
- Boundary Scan Test circuit complies to the IEEE Std. 1149.1 -1990

  ID-Code = 0 7111 02 B
- I²C-bus controlled (full read-back ability by an external controller)

2 APPLICATIONS

- Desktop Video
- Multimedia
- Digital Television
- Image Processing
- Video Phone

3 GENERAL DESCRIPTION

The VIDEO INPUT PROCESSOR is a combination of a two channel analog preprocessing circuit including Source-Selection, Anti-Aliasing Filter and A/D-converter, an Automatic Clamp and Gain Control, a Clock Generation Circuit (CGC), a Digital Multi Standard Decoder (PAL BGHI, PAL M, PAL N, NTSC M, NTSC N), a Brightness-Contrast-Saturation-Control circuit and a Colour Space Matrix (see Fig.1).

The CMOS circuit SAA7111, analog frontend and digital video decoder, is a highly integrated circuit for Desktop Video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL and NTSC signals into CCIR-601 compatible colour component values. The SAA7111 accepts as analog inputs CVBS or S-Video (Y-C) from TV or VCR sources. The circuit is I²C-bus-controlled.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	digital supply voltage range	4.5	5.5	V
V_{DDA}	analog supply voltage range	4.75	5.25	V
T_{amb}	ambient temperature range	0	70	°C

5 ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7111	68	PLCC	Plastic	SOT188DA27

6 BLOCK DIAGRAM

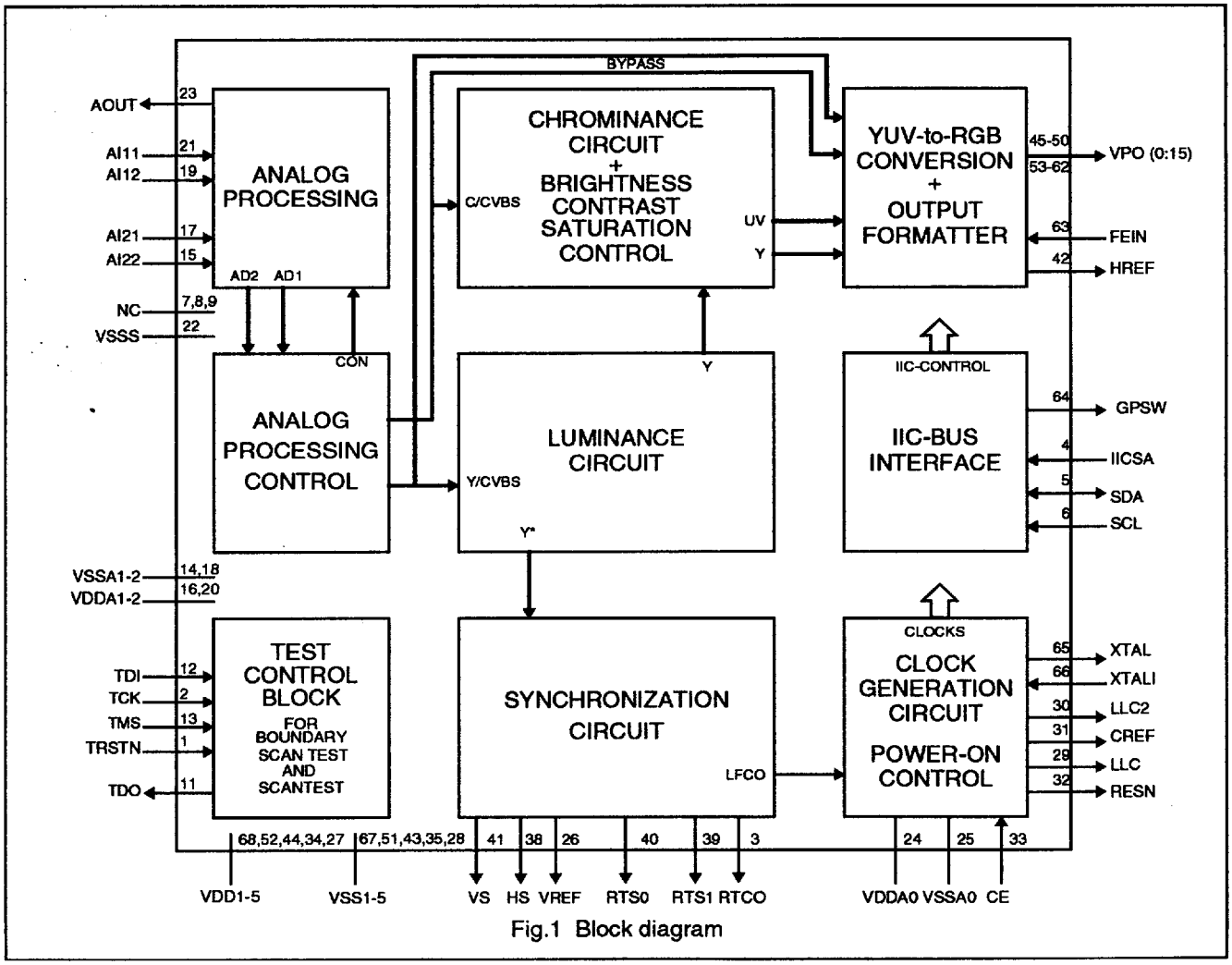


Fig.1 Block diagram

7 PINNING

PIN	SYMBOL	I/O/P	DESCRIPTION
1	TRSTN	I	Test ReSeT Not for Boundary Scan Test. [1*] [2*] [3*]
2	TCK	I	Test Clock for Boundary Scan Test [3*]
3	RTCO	O	Real Time Control Output. Contains information about actual system clock frequency, subcarrier frequency and phase and PAL-sequence
4	IICSA	I	I²C Slave Address select; 0 = > 48h for write, 49h for read, 1 = > 4Ah for write, 4Bh for read
5	SDA	I/O	I²C- bus SERIAL DATA input/output
6	SCL	I	I²C- bus SERIAL CLOCK input
7	NC (REFH)	P	not connected (REFerence High input (+2.25 V), only for analog testing)
8	NC (REFC1)	P	not connected (REFerence Current, only for analog testing)
9	NC (REFC2)	P	not connected (REFerence Current, only for analog testing)
10	NC	P	not connected
11	TDO	O	Test Data Output for Boundary Scan Test [3*]
12	TDI	I	Test Data Input for Boundary Scan Test [3*]
13	TMS	I	Test Mode Select for Boundary Scan Test or Scan Test [3*]
14	V_{SSA2}	P	ground for analog input 2
15	AI22	I	analog input 22
16	V_{DDA2}	P	positive supply voltage (+5V) for analog input 2
17	AI21	I	analog input 21
18	V_{SSA1}	P	ground for analog input 1
19	AI12	I	analog input 12
20	V_{DDA1}	P	positive supply voltage (+5V) for analog input 1
21	AI11	I	analog input 11
22	V_{SSS}	P	SUBSTRATE ground connection
23	AOUT	O	Analog test OUTput; for testing the analog input channels
24	V_{DDA0}	P	positive supply voltage (+5V) for internal CGC (Clock Generation Circuit)
25	V_{SSA0}	P	ground for internal CGC
26	VREF	O	Vertical REFerence output signal (I ²C-bit COMPO = 0) or inverse composite blank signal (I ²C-bit COMPO = 1) (enabled via I²C-bit OEHV)
27	V_{DD5}	P	positive supply voltage (+5V)
28	V_{SS5}	P	ground
29	LLC	O	Line-Locked system Clock output (27 MHz)
30	LLC2	O	Line-Locked Clock 1/2 output (13.5 MHz)
31	CREF	O	Clock Reference output. This is a clock qualifier signal distributed by the internal clock generator circuit (CGC) for a data rate of LLC2. Using CREF all interfaces on the VPO bus are able to generate a bus timing with identical phase. If CCIR 656 format is selected (OFTS0 =1 and OFTS1 = 1) an inverse composite blank signal (pixel qualifier) is provided on this pin.

Table 1 Pinning

PIN	SYMBOL	I/O/P	DESCRIPTION
32	RESN	O	Reset active LOW output; sets the device into a defined state. All data outputs are in high impedance state. The I²C-bus is reset (waiting for start condition).
33	CE	I	Chip Enable; connection to ground forces a reset
34	V_{DD4}	P	positive supply voltage (+5V)
35	V_{SS4}	P	ground
36	NC		not connected
37	NC		not connected
38	HS	O	Horizontal Sync output signal (programmable). The positions of the positive and negative slopes are programmable in 8 LLC increments over a complete line (=64us) via I²C-bus bytes HSB and HSS. Fine position adjustment in 2 LLC increments can be done via I²C bits HDEL1 and HDEL0.
39	RTS1	O	Two functions output: controlled by I²C-bit RTSE1: RTSE1 = 0: Pal Line Identifier (low = "PAL"-line); indicates the inverted and non inverted R-Y-component for PAL signals RTSE1 = 1: H-PLL Locked indicator; a high state indicates that the internal horizontal PLL has locked.
40	RTS0	O	Two functions output: controlled by I²C-bit RTSE0: RTSE0 = 0: Odd/Even field identification (high = odd field). RTSE0 = 1: Vertical Locked indicator; a high state indicates that the internal VNL has locked.
41	VS	O	Vertical Sync signal (enabled via I²C-bit OEHV); this signal indicates the vertical sync with respect to the YUV output. The high period of this signal is approx. six lines if the vertical noise limiter (VNL) function is active. The positive slope contains the phase information for a deflection controller.
42	HREF	O	Horizontal REFerence output signal (enabled via I²C-bit OEHV); this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The high period of HREF is 720 Y samples long. HREF can be used to synchronize data multiplexer/ demultiplexers. HREF is also present during the vertical blanking interval.
43	V_{SS3}	P	ground
44	V_{DD3}	P	positive supply voltage (+5V)
45-50	VPO(15:10)	O	Digital VPO-BUS (Video Port Out) signal; higher bits of the 16-bit YUV-BUS or the 16-bit RGB-BUS output signal. The output data rate, the format and multiplexing scheme of the VPO bus are controlled via I²C-bits OFTS0 and OFTS1. With I²C-bit VIPB = 1 the six MSB's of the digitized input signal (AD1[7-2]) are connected to these outputs.
51	V_{SS2}	P	ground
52	V_{DD2}	P	positive supply voltage (+5V)
53-62	VPO (9-0)	O	Digital VPO-BUS output signal; lower bits of the 16-bit YUV-BUS or the 16-bit RGB-BUS output signal. The output data rate, the format and multiplexing schema of the VPO bus are controlled via I²C-bits OFTS0 and OFTS1. With I²C-bit VIPB = 1 the digitized input signals (AD1[1-0] andAD2[7-0]) are connected to these outputs.

Table 1 Pinning

PIN	SYMBOL	I/O/P	DESCRIPTION
63	FEIN	I	Fast Enable INput signal (active low); this signal is used to control fast switching on the digital YUV bus. A high at this input forces the IC to set its Y and UV outputs to the high impedance state.
64	GPSW	O	General Purpose SWitch (output); the state of this signal is set via I^2C-bus control and the levels are TTL-compatible.
65	XTAL	O	Second terminal of crystal oscillator; not connected if TTL clock signal is used.
66	XTALI	I	Input terminal for 24.576 MHz crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal.
67	V_{SS1}	P	ground
68	V_{DD1}	P	positive supply voltage (+5V)

Table 1 Pinning

Note1* For board design without Boundary Scan implementation (pin compatibility with the SAA7110) connect the TRSTN pin to ground

Note2* This pin provides easy initialization of BST circuitry. TRSTN can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once

Note3* According to the IEEE1149.1 standard the pads TCK, TDI, TMS and TRSTN are input pads with a internal pull-up transistor and TDO a tri-state output pad.

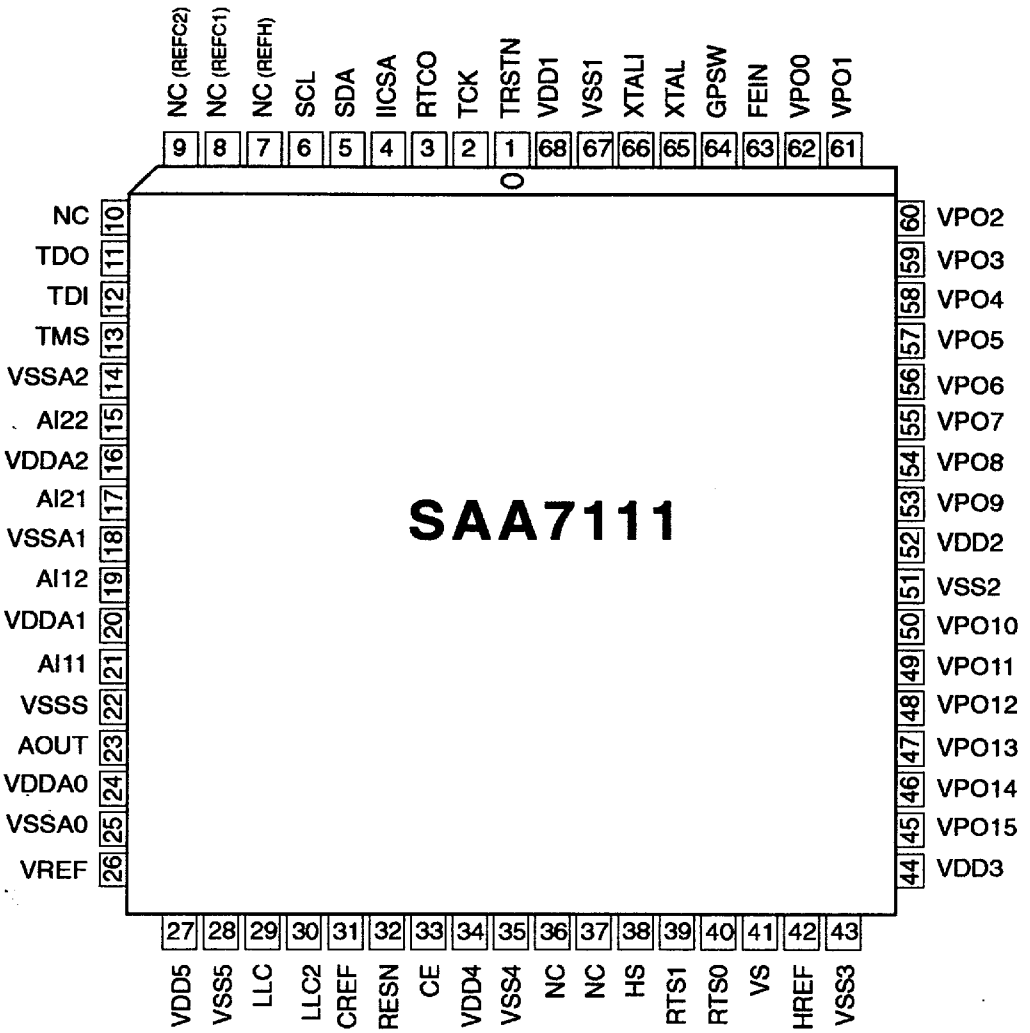


Fig.2 Pinning

8 FUNCTIONAL DESCRIPTION

8.1 ANALOG INPUT PROCESSING

The VIP offers four analog signal inputs, two analog main channels with clamp circuit, analog amplifier, anti alias filter and video CMOS ADC (see Fig.5).

8.2 ANALOG CONTROL CIRCUITS

The anti alias filters are adapted to the line locked clock frequency with help from a filter control.
During the vertical blanking time gain and clamping control are frozen.

8.2.1 CLAMPING

The clamp control circuit controls the proper clamping of the analog input signals. The coupling capacitor is also used to storage and filter the clamping voltage. An internal digital clamp comparator generates the information about clamp-up or clamp-down. The clamping levels for the two A/D channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

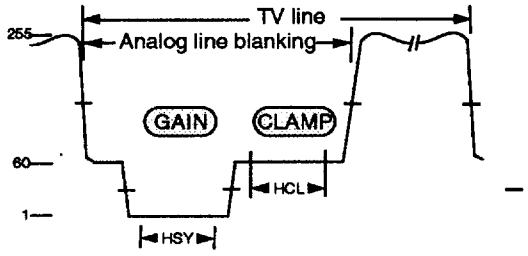


Fig.3 Analog Line
with Clamp (HCL) and Gain Range (HSY)

8.2.2 GAIN CONTROL

Signal (white) peak control limits the gain at signal overshoots. The flow charts figure 9 and figure 10 show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

The gain control circuit gets via I²C the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built in Automatic Gain Control AGC as part of the Analog Input Control (AICO). The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. AGC active time is the sync bottom of the video signal.

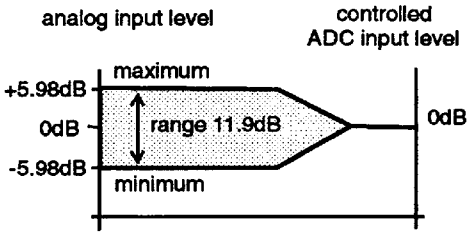


Fig.4 Automatic Gain Range

8.3 CHROMINANCE PROCESSING

The 8-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 (0 and 90 degrees phase relationship to the demodulator axis) are applied. The frequency is dependent on the present colour standard. The output signals of the multipliers are lowpass-filtered (four programmable characteristics) to achieve the desired bandwidth for the colour difference signals.

These signals are fed to the block BCS, which includes five functions:

AGC (automatic gain control for chrominance)

chroma amplitude matching (different gain factors for R-Y and B-Y to achieve CCIR 601 levels),

chroma saturation control

luminance contrast and brightness

limiting YUV to the values 1 (min) and 254 (max) to fulfil CCIR 601 requirements

The burst processing block performs the feedback loop of the chroma PLL and contains

Burstgate accumulator

Colour-identification and -killer

comparison nominal/actual burst amplitude

loopfilter chroma gain control

loopfilter chroma PLL

PAL-sequence-generation

Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chroma combfilter block eliminates crosstalk between the chrominance channels according to PAL-standard-requirements. For NTSC-colour standards the chroma combfilter can be used to eliminate crosstalk from

luminance to chrominance ("cross-colour") for vertical structures. The combfilter can be switched off if desired.

The resulting signals are fed to the output-interface, which contains the VPO output formatter, Y delay compensation (programmable) and the output control logic (see Fig.6).

8.4 RGB MATRIX

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. The realized matrix equations consider the digital quantization:

R = Y + 1.371 V

G = Y - 0.336 U- 0.698 V

B = Y + 1.732 U

After dithering (noise shaping) the RGB data are fed to the output-interface within the VPO -BUS output formatter.

8.5 LUMINANCE PROCESSING

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-Video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via I²C bus) in two bandpass filters with selectable transfer characteristic. A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ('unpeaked') signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominancetrap modes. The improved luminance signal is fed to the BCS-control located in the chrominance processing block (see Fig.7).

8.6 VPO-BUS, DIGITAL OUTPUTS

The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box, or a field memory, a digital colour space converter (SAA 7192 DCSC), a Video enhancement and D/A processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

The output data formats are controlled via the I²C bits OFTS0 and OFTS1. Timing for the datastream formats 411YUV(12Bit), 422YUV(16Bit) and 565RGB(16Bit) with LLC2 data rate is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference). The higher output signals VPO(15:8) in the YUV format perform the digital luminance signal. The lower output signals VPO(7:0) in the YUV format are the bits of the multiplexed colour difference signals (B-Y) and (R-Y). The arrangement of the RGB datastream bits on the VPO-BUS are for B => VPO(4:0) for G => VPO(10:5) and for R => VPO(15:11).

The datastream format 422YUV (the 8 higher output signals VPO(15:8)) in LLC data rate fulfils the CCIR-656 standard with its own timing reference code on the start and the end of each video data block.

A pixel in the format tables is the time required to transfer a full set of samples. In case of 4:2:2 format two luminance samples are transmitted in comparison to one (B-Y) and one (R-Y) sample within a pixel. The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input FEIN to LOW. The signal is used to control fast switching on the digital VPO-bus. High on this pin forces the YUV outputs to a high-impedance state (see Fig.12).

The digitized analog PAL or NTSC signals AD1[7-0] and AD2[7-0] are connected directly to the VPO-bus via I²C-bit VIPB = 1.

AD1[7-0] --> VPO[15-8] and AD2[7-0] -->VPO[7-0]

The selection of the analog input channels are controlled via I²C subaddress 02 MODE select.

8.7 SYNCHRONIZATION

The prefiltered luminance signal is fed to the synchronization stage. It's bandwidth is reduced to 1 MHz in a low- pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e. g. HCL and HSY) are generated according to analog frontend requirements. The output signals HS, VS, and PLIN are locked to the timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO (see Fig.7).

8.8 CLOCK GENERATION CIRCUIT

The internal CGC generates all clock signals required for the video input processor. The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency (6.75 MHz = 432 x fH). Internally the LFCO signal is multiplied by factors 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to get the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor (see Fig.18).

8.9 POWER-ON RESET and CE-INPUT

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 3.5 V) will start the reset sequence: All outputs are forced to 3-state. The indicator output RESN is LOW for about 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system. It is possible to force a reset by pulling the CE (chip enable) to ground. After rising edge of CE and sufficient power supply voltage the outputs LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA return from 3-state to active, while HREF, VREF, HS and VS remain in 3-state and have to be activated via I^2C-programming (see Tab. 7).

8.10 RTCO OUTPUT

This real time control and status output signal contains serial information about actual system clock (increment of the HPLL), subcarrier frequency (increment and phase [via reset] of the FSC-PLL) and PAL-sequence bit. The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve "clean" encoding (see Fig.13).

9 BLOCK DIAGRAM

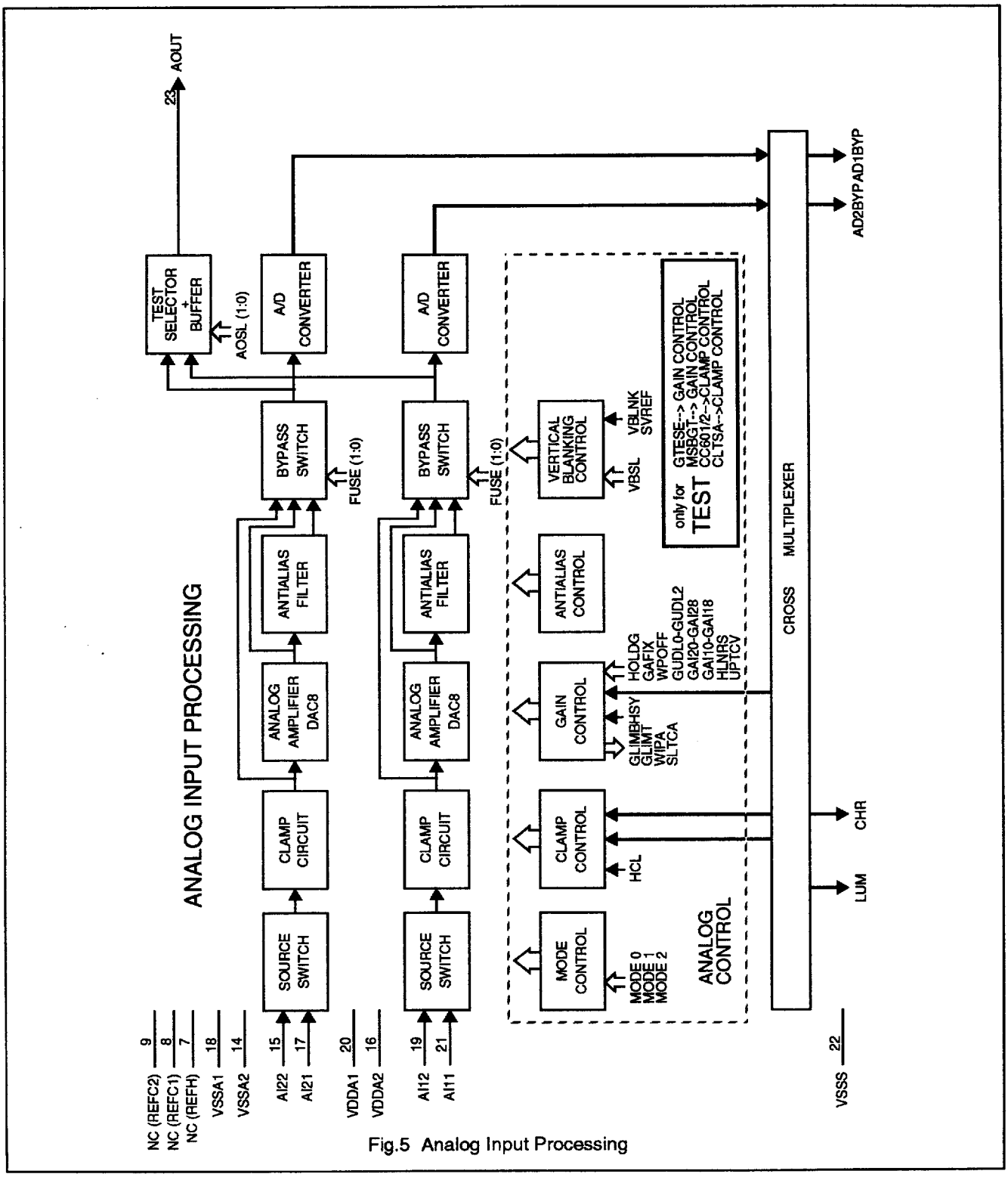


Fig.5 Analog Input Processing

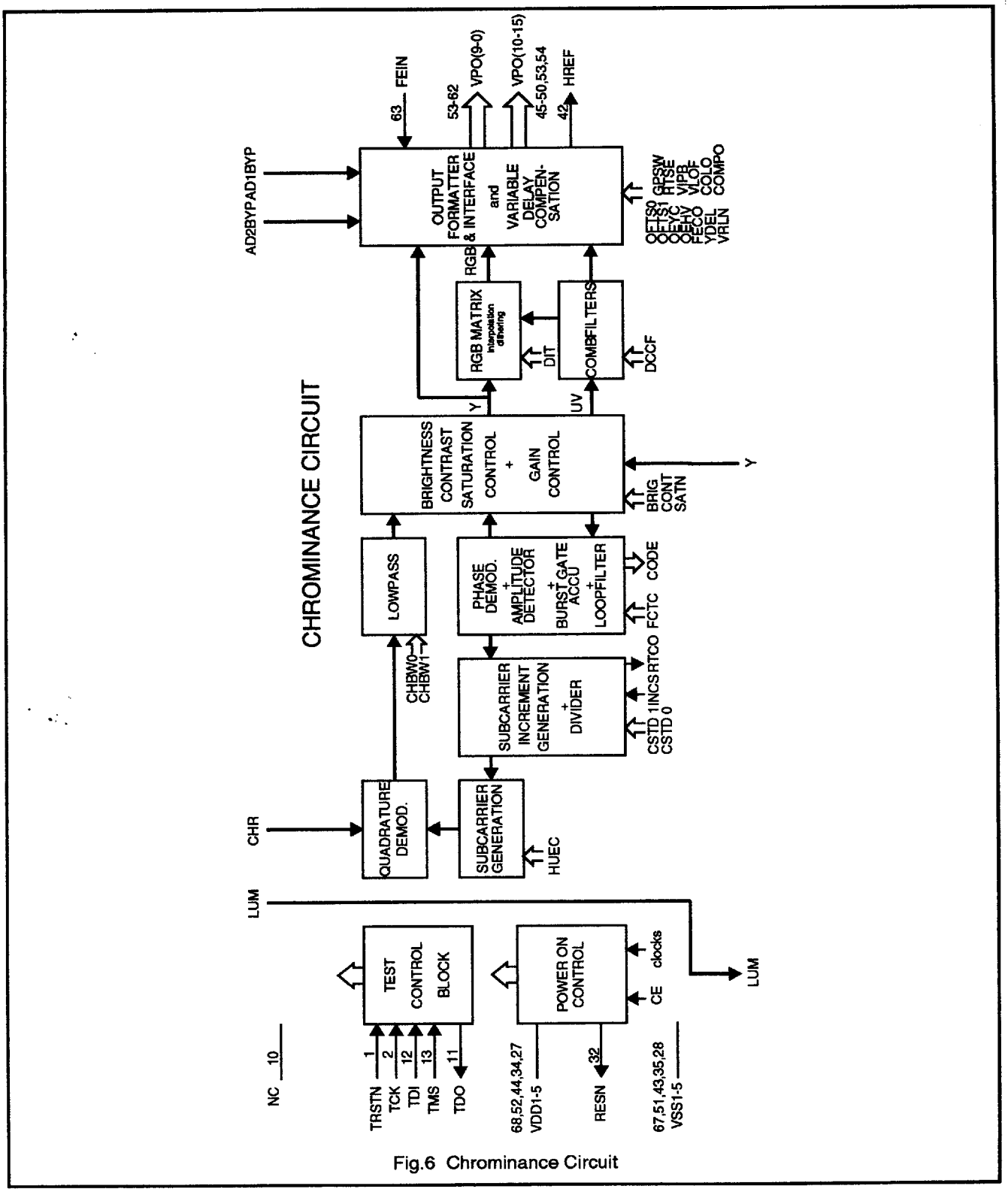


Fig.6 Chrominance Circuit

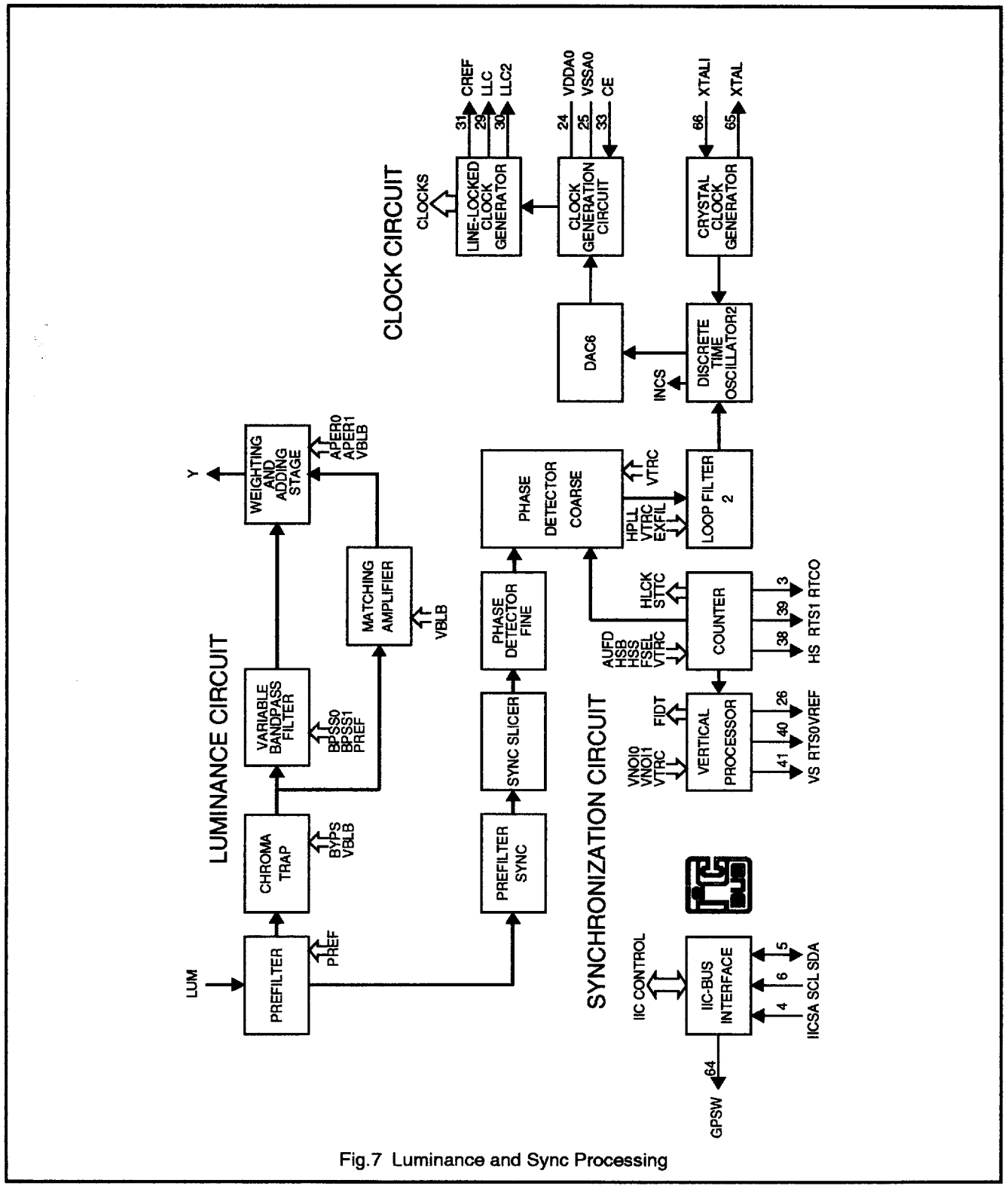


Fig.7 Luminance and Sync Processing

10 GAIN CHARTS

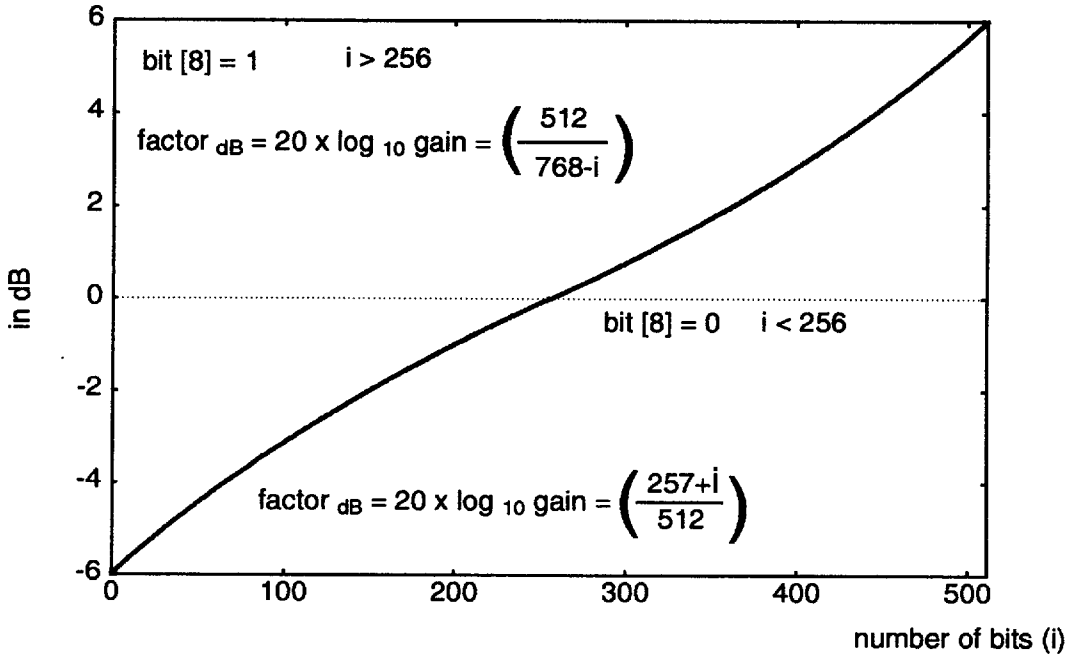


Fig.8 Gain Curve

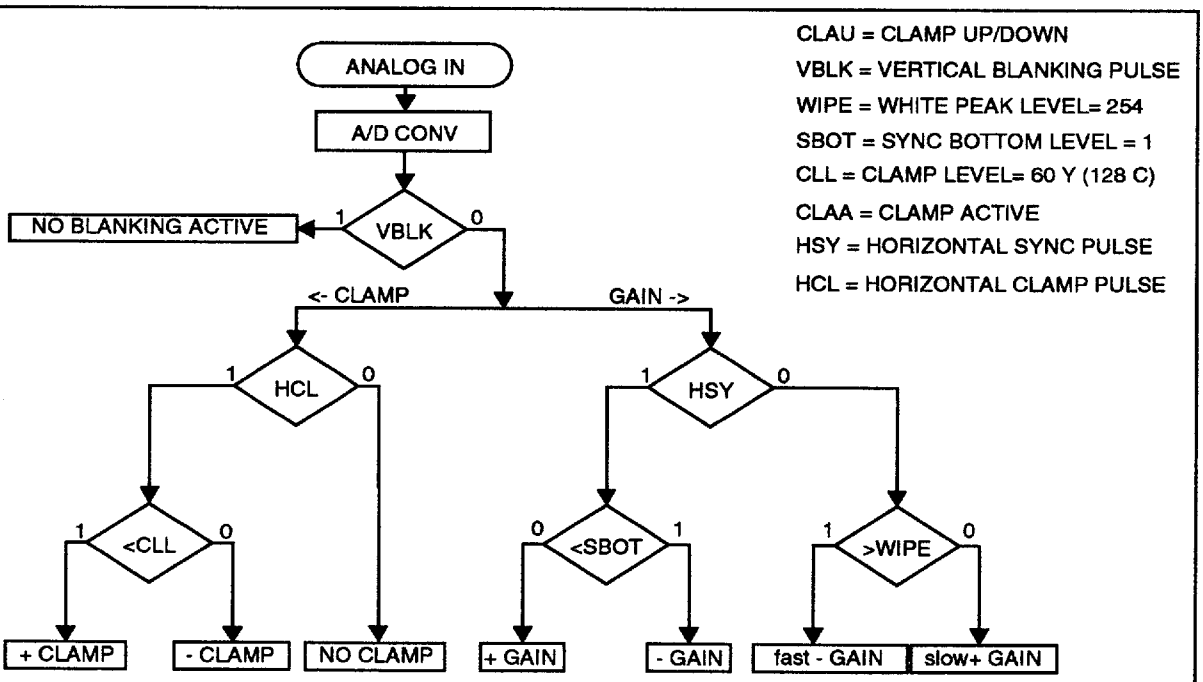


Fig.9 Clamp and Gain Flow

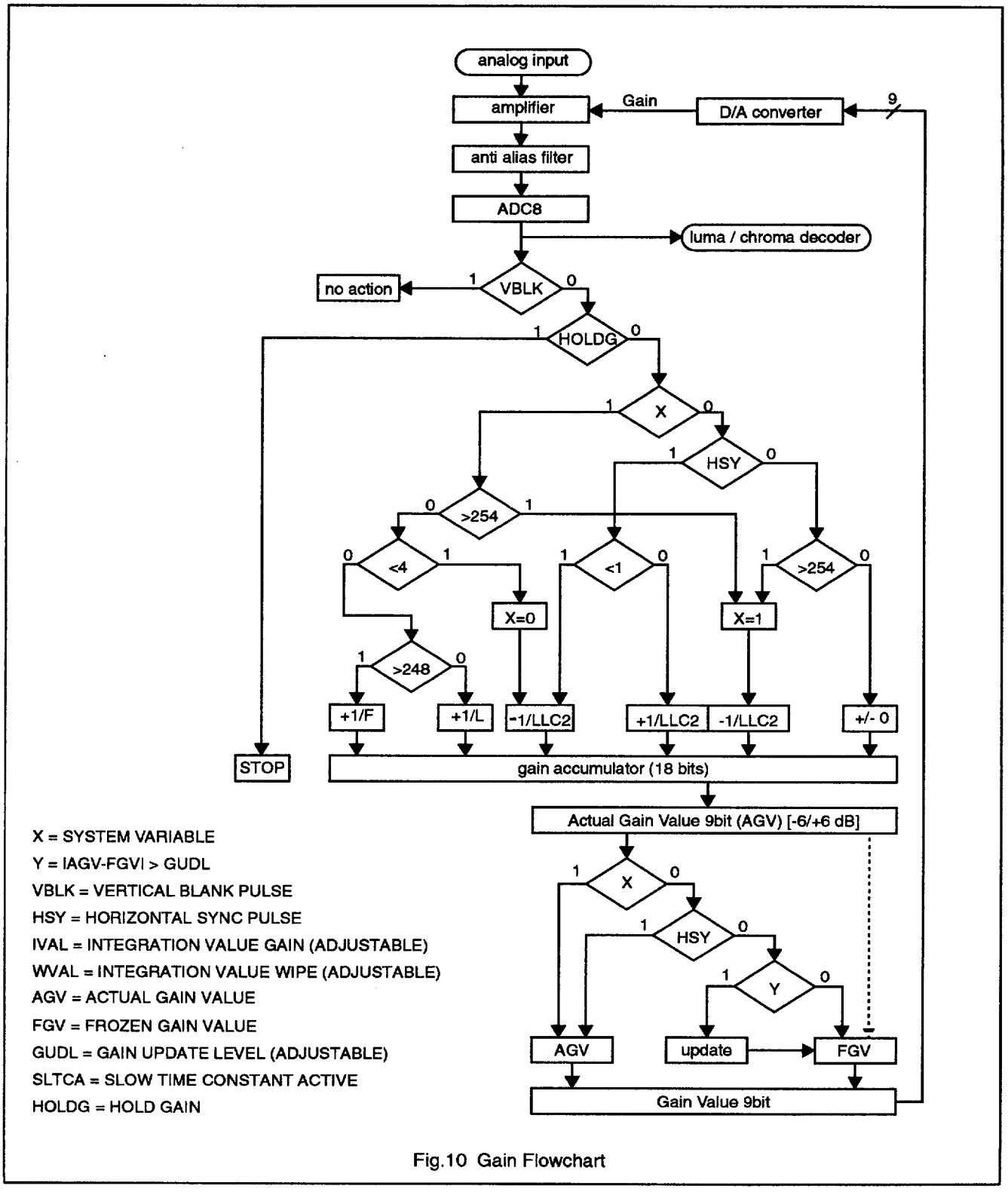


Fig.10 Gain Flowchart

11 CHARACTERISTICS

11.1 LIMITING VALUES

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{stg}	Storage temperature	-65	+150	°C
t_{amb}	Temperature under bias	-10	+80	°C
T_{amb}	Operating ambient temperature range	0	+70	°C
V_{DD}	Supply voltage digital	-0.5	+6.5	V
V_{DDA}	Supply voltage analog	-0.5	+6.5	V
V_I	Input voltage digital	-0.5	+6.5	V
V_I	Input voltage analog	-0.5	+6.5	V
$V_{diffGND}$	Difference voltage V_{SSAall} - V_{SSall}	-	100	mV
V_{ESD}	Electrostatic * handling for all pins	-	±2000	V
P_{tot}	total power dissipation	-	2.5	W
* Equivalent to discharging a 100pF capacitor through an 1.5kW series resistor (Human Body Model)				

Table 2 Limiting Values

11.2 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	LIMITS TYP	MAX	UNIT
Supply						
V_{DD1-5}	digital supply voltage range		4.5	5	5.5	V
I_{DD1-5}	digital total supply current		-	160	-	mA
$V_{DDA0,2-4}$	analog supply voltage range		4.75	5	5.25	V
$I_{DDA0,2-4}$	analog total supply current		-	85	120	mA
Analog part						
I_{clamp}	clamp current	V_F=1.25V_{DC}	-	2	-	µA
$V_{i(pp)}$	input voltage (AC coupling necessary) note 4	C_{coup}=10nF	0.55	1	1.90	V_{pp}
$\|Z_i\|$	input impedance	I_{clamp} off	200	-	-	kW
C_i	input capacitance		-	-	10	pF
a	channel crosstalk	f < 5MHz	-	-	-50-	dB
ADCs						
B	analog bandwidth	-3dB	-	15	-	MHz
Φ_{diff}	differential phase (Amplifier and AAF=bypass)		-	2	-	deg
G_{diff}	differential gain (Amplifier and AAF=bypass)		-	2	-	%

Table 3 Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
f_{LLC}	clock rate ADC		11	-	16	MHz
DLE	DC differential linearity error		-	1/2	-	LSB
ILE	DC integral linearity error		-	1	-	LSB
Digital inputs						
$V_{IL.I2C}$	input voltage LOW	SDA and SCL	-0.5	-	1.5	V
$V_{IH.I2C}$	input voltage HIGH	SDA and SCL	0.7 V_{DD}	-	V_{DD}+0.5	V
V_{IL}	input voltage LOW	other inputs	-0.5	-	0.8	V
V_{IH}	input voltage HIGH	other inputs	2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	1	µA
C_I	input capacitance	other inputs	-	-	8	pF
$C_{I.IO}$	input capacitance	I/O at high impedance	-	-	8	pF
Digital outputs						
$V_{OL.I2C}$	output voltage LOW	SDA at 3mA sink current	-	-	0.4	V
V_{OL}	output voltage LOW	note 1	0	-	0.6	V
V_{OH}	output voltage HIGH	note 1	2.4	-	V_{DD}	V
$V_{OLclocks}$	output voltage LOW	clocks	-0.5	-	0.6	V
$V_{OHclocks}$	output voltage HIGH	clocks	2.6	-	V_{DD}+0.5	V
FEIN input timing						
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold-time		3	-	-	ns
Data and control output timing						
C_L	output load capacitance		15	-	50	pF
t_{OH}	output hold time	15 pF	5	-	-	ns
t_{PD}	propagation delay	40 pF	-	-	20	ns
t_{PZ}	propagation delay to 3-state		-	-	20	ns

Table 3 Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	LIMITS TYP	MAX	UNIT
Clock output timing (LLC, LLC2)						
$C_{L\ LLC}$	output load capacitance		15	-	40	pF
t_{LLC}	cycle time LLC		35	-	39	ns
t_{LLC2}	cycle time LLC2		70	-	78	ns
δ	duty factors: t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	load capacitance = 40 pF	40	-	60	%
t_r	rise time LLC, LLC2	0.6V to 2.6V	-	-	5	ns
t_f	fall time LLC, LLC2	2.6V to 0.6V	-	-	5	ns
t_{dLLC2}	delay time LLC out to LLC2 out	at 1.5V, LLC/LLC2=40pF	-4	-	8	ns
Data qualifier output timing (CREF)						
$t_{OH.CREF}$	output hold time	15 pF	4	-	-	ns
$t_{PD.CREF}$	propagation delay from positive edge of LLC	40 pF	-	-	20	ns
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	-	15625	-	Hz
		60 Hz field	-	15734	-	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		-	-	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL-BGHI	-	4433619	-	Hz
		NTSC-M	-	3579545	-	Hz
		PAL-M	-	3575612	-	Hz
		PAL-N		3582056	-	Hz
$\Delta f_H/f_{Hn}$	lock in range		±400	-	-	Hz
Crystal oscillator						
f_n	nominal frequency	3rd harmonic	-	24.576	-	Mhz
Df/f_n	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistor R_S		-	40	80	W
	motional capacitance C_1		-	1.5 ±20%	-	fF

Table 3 Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	LIMITS TYP	MAX	UNIT
	parallel capacitance C_0		-	3.5 ±20%	-	pF
	Philips catalogue number:	4322 143 05291				

Notes to the characteristics:

1. The levels must be measured with load circuits: 1.2kΩ at 3V (TTL load), C_L=50pF.
Effects of rise and fall times are included in the calculation of t_{OH}, t_{PD} and t_{PZ}. Timings and levels refer to drawings and conditions shown in Fig.11 on next page.

Table 3 Characteristics

12 PROCESSING DELAY

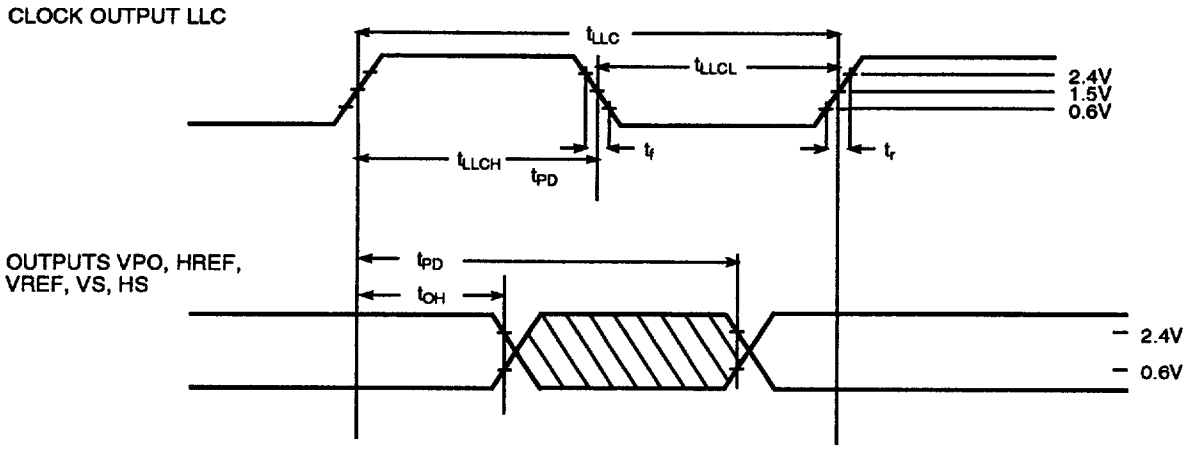
FUNCTION	ANALOG DELAY (TYPICAL) AI22 -> ADCIN(AOUT) (ns)		DIGITAL DELAY ADCIN(AOUT) -> YPOOUT (1/LLC) [YDEL=0, CAD2/3=1]
	AFCCS=0	AFCCS=1	
without AMP, AAF	20		tbd.
with AMP, without AAF	tbd.		
with AMP + AAF (50Hz)	tbd.	tbd.	
with AMP + AAF (60Hz)	tbd.	tbd.	

Table 4 Processing Delay

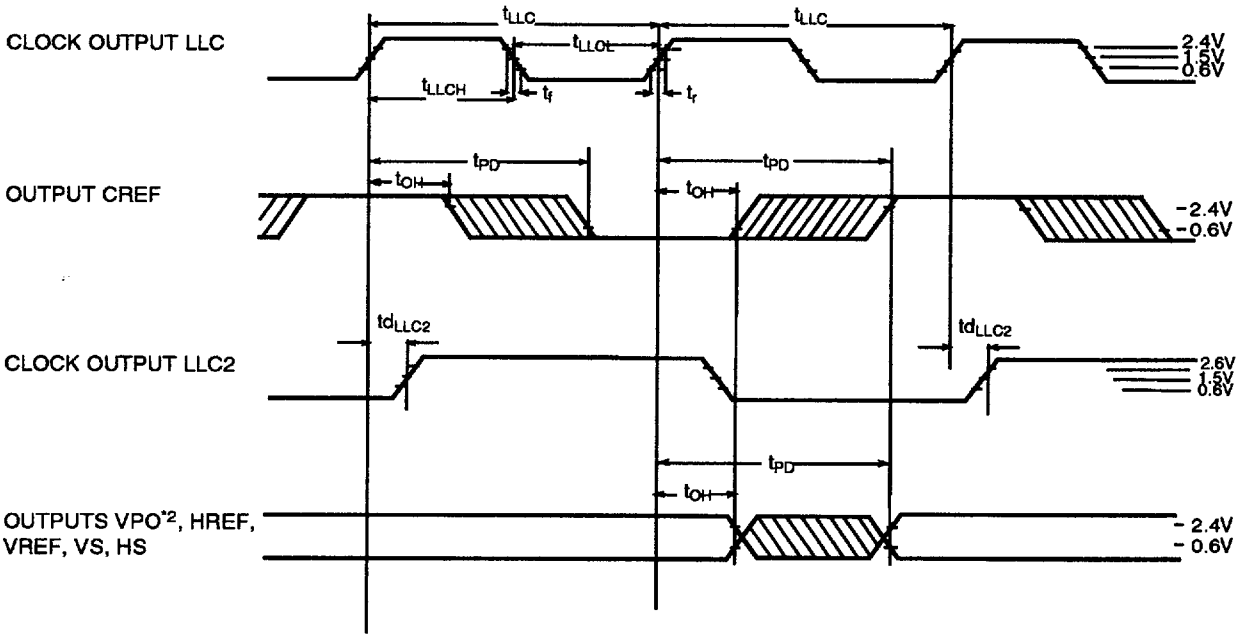
13 TIMING DIAGRAMS

13.1 CLOCK DATA TIMING

8 bit CCIR 656 format of the VPO-bus *1



12 /16 bit format of the VPO-bus *1

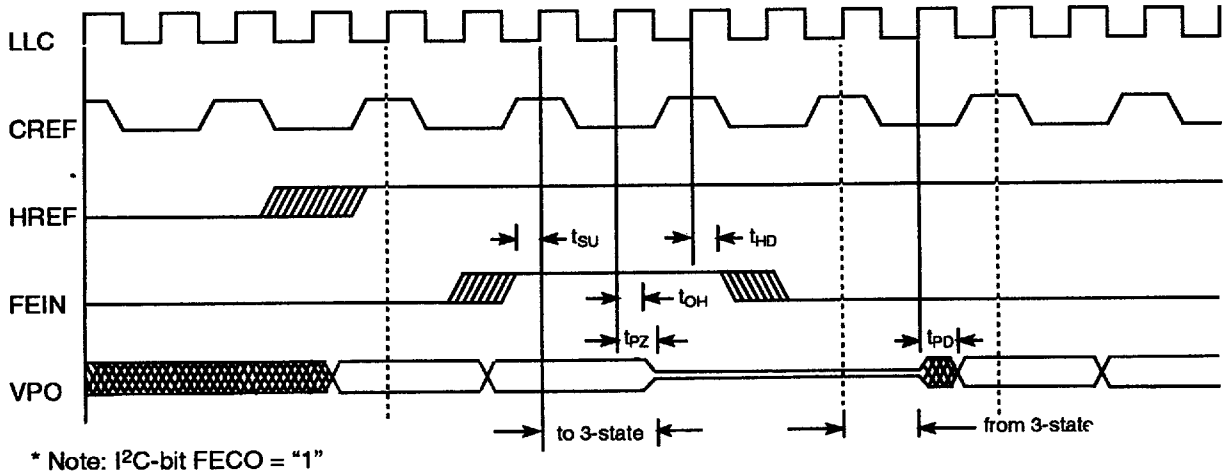


(1) explanation of the output formats see Tab. 8.
(2) for the FEIN timing of the VPO-Bus see Fig.12

Fig.11 CLOCK/DATA Timing

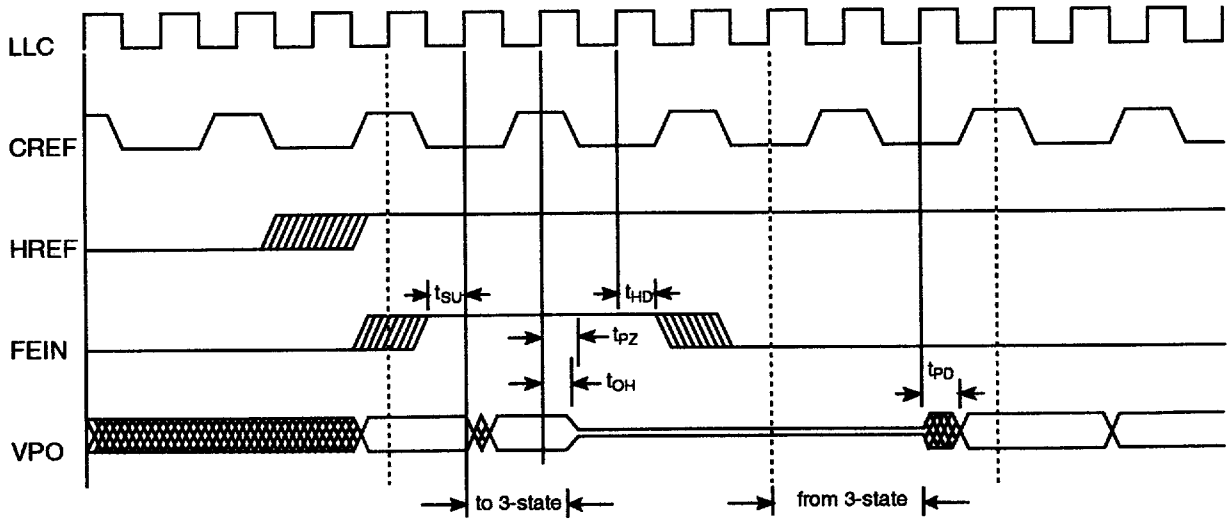
13.2 DIGITAL OUTPUT CONTROL

Fein sampling at CREF = high *



* Note: I²C-bit FECO = "1"

Fein sampling at CREF = low (timing compatible to SAA7110)*



* Note: I²C-bit FECO = "0"

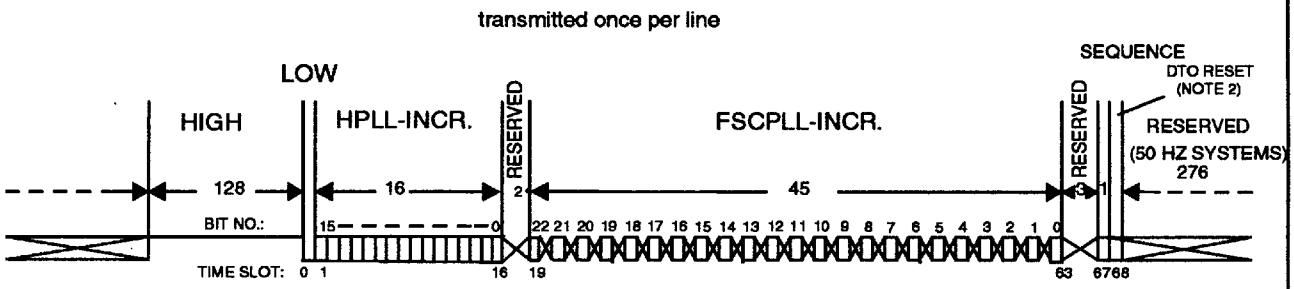
Fig.12 FEIN Timing

OEYC	FEIN	VPO (15:0) (1)	VPO(15:8) (2)	VPO(7:0) (2)
0	0	Z	Z	Z
1	0	active	active	Z
0	1	Z	Z	Z
1	1	Z	active	Z

Table 5 Digital Output Control

1. OFTS[1:0] = 1 0 or 0 1or 00
2. OFTS[1:0] = 1 1

13.3 REALTIME CONTROL OUTPUT



Note 1: RTCO-sequence is generated in LLC/4.
Note 2: Set to zero for one transmission, if a phase reset of the fsc-DTO is applied via I²C-bit CDTO.

Fig.13 Realtime Control Output

13.4 HREF TIMING

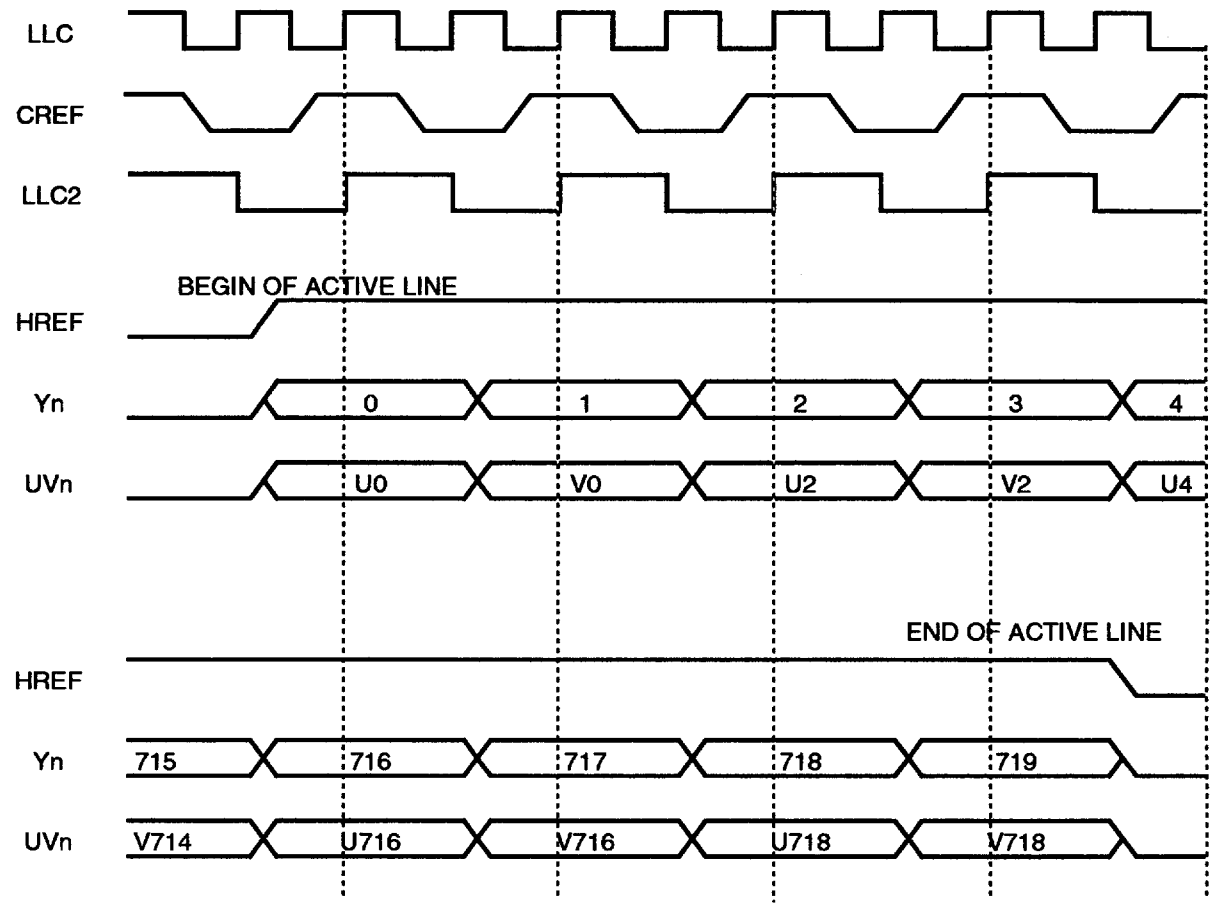
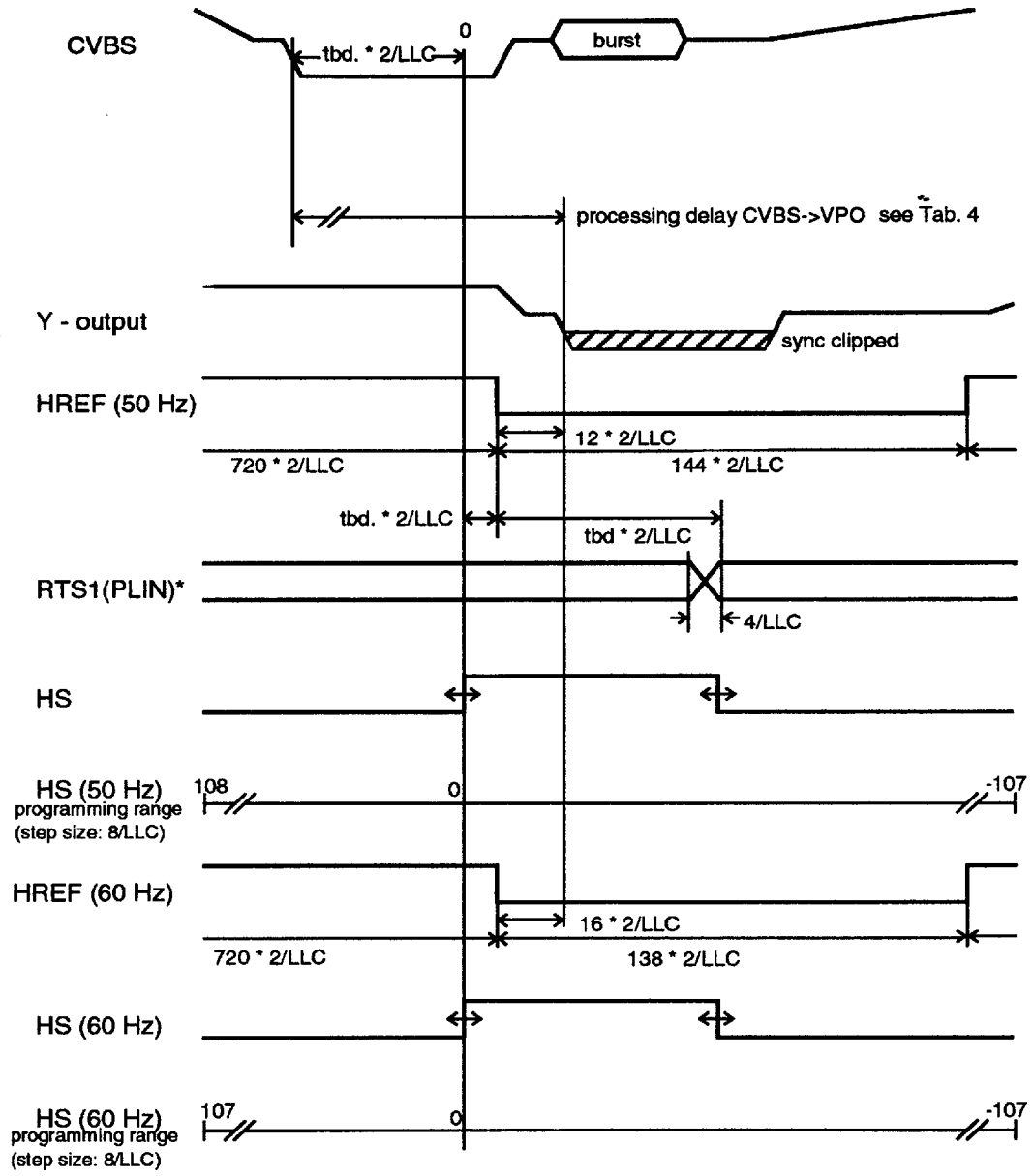


Fig.14 HREF Timing

13.5 HORIZONTAL TIMING



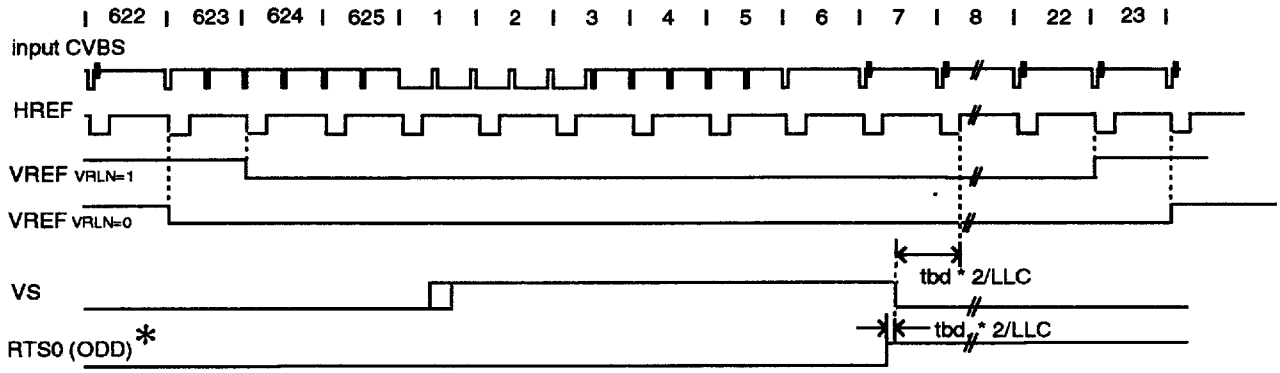
* Note: PLIN is switched to output RTS1 via I²C-bit RTSE1 = "0"

Fig.15 Horizontal Timing

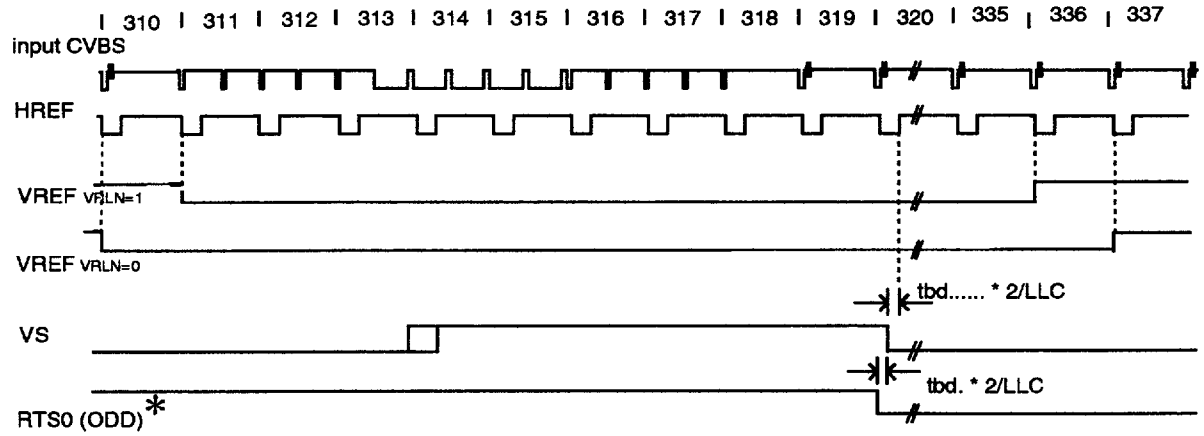
13.6 VERTICAL TIMING 50Hz

condition: Nominal input signal, 50 Hz, VNL in normal mode (VNOI = 00b)

a: 1st field



b: 2nd field



* Note: ODD is switched to output RTS0 via I²C-bit RTSE0 = "0"

The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bit VBLB is set to '1'

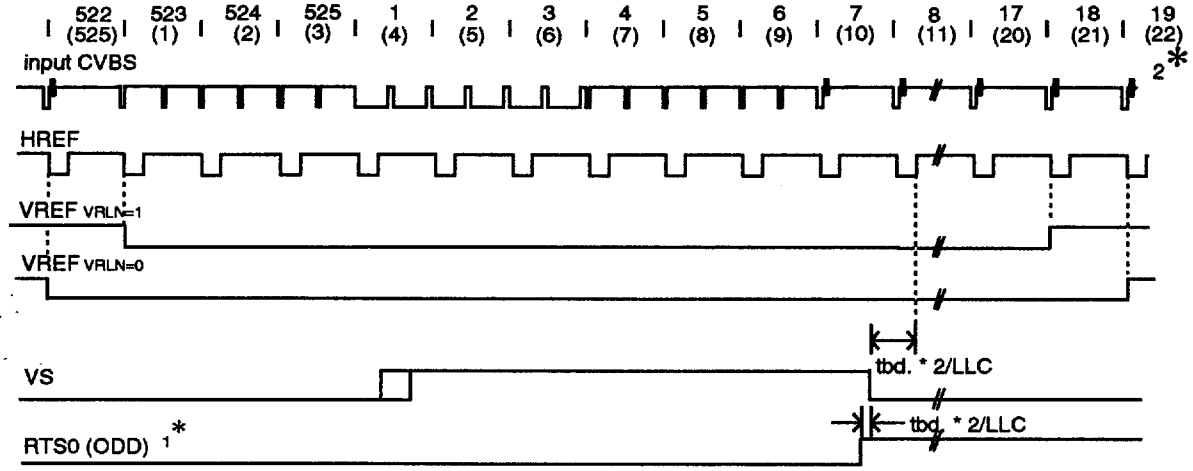
The chrominance delay line (chroma-combfilter for NTSC, phase-error-correcting for PAL) is disabled during VREF = 0)

Fig.16 Vertical Timing 50Hz

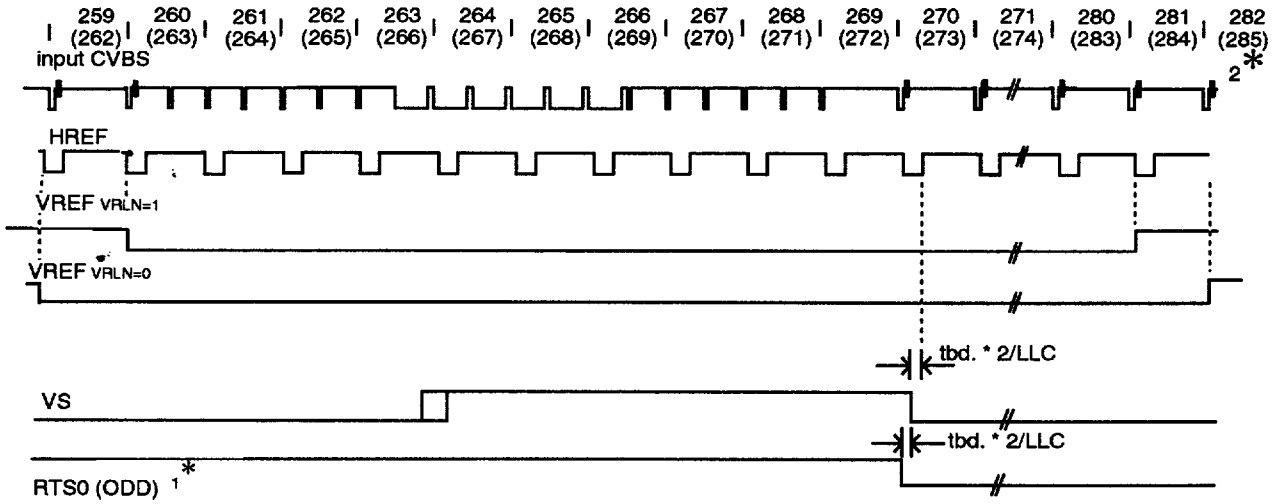
13.7 VERTICAL TIMING 60Hz

condition: Nominal input signal, 60 Hz, VNL in normal mode (VNOI = 00b)

a: 1st field



b: 2nd field



1* Note: ODD is switched to output RTS0 via I²C-bit RTSE0 = "0"

2* Note: Line numbers in brackets refer to CCIR line counting

The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bit VBLB is set to '1'

The chrominance delay line (chroma-combfilter for NTSC, phase-error-correcting for PAL)
is disabled during VREF = 0)

Fig.17 Vertical Timing 60Hz

14 CLOCK SYSTEM

14.1 CLOCK GENERATION CIRCUIT

The internal CGC generates the system clocks LLC, LLC2 and the clock reference signal CREF. The internal generated LFCO (triangular waveform) is multiplied by two or four via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have 50% duty factor.

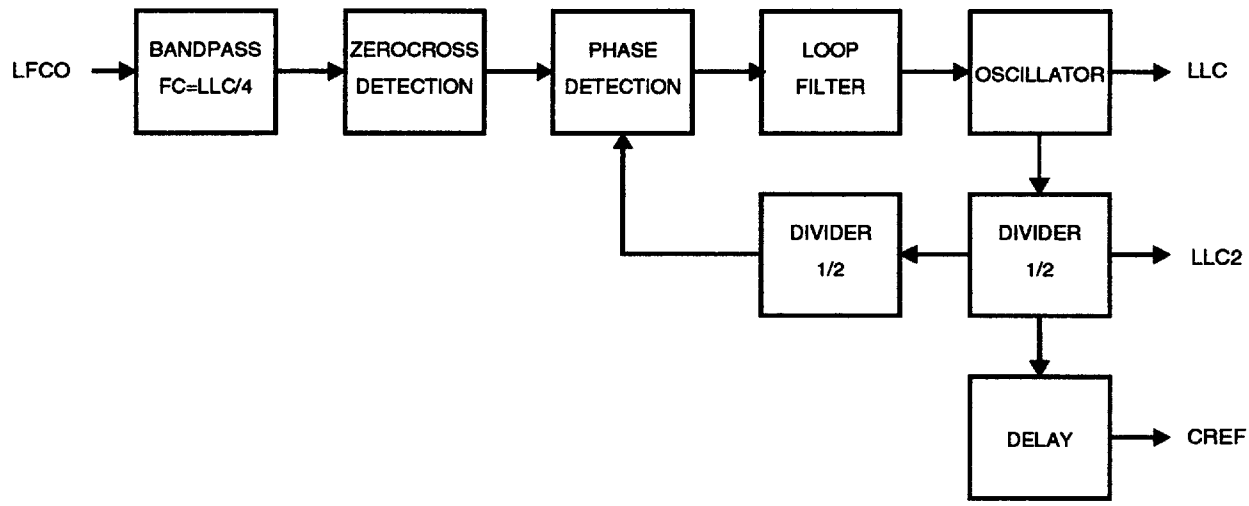


Fig.18 CLOCK Generation Circuit

14.2 CLOCK FREQUENCIES

CLOCK	FREQUENCY (MHZ)
XTAL	24.576
LLC	27
LLC2	13.5
LLC4	6.75
LLC8	3.375

Table 6 CLOCK Frequencies

14.3 POWER-ON CONTROL

Power-on reset is activated at power-on, chip enable, PLL Clock generation failure and if the supply voltage decreases below 3.5 V. The RESN signal can be applied to reset other circuits of the digital TV system.

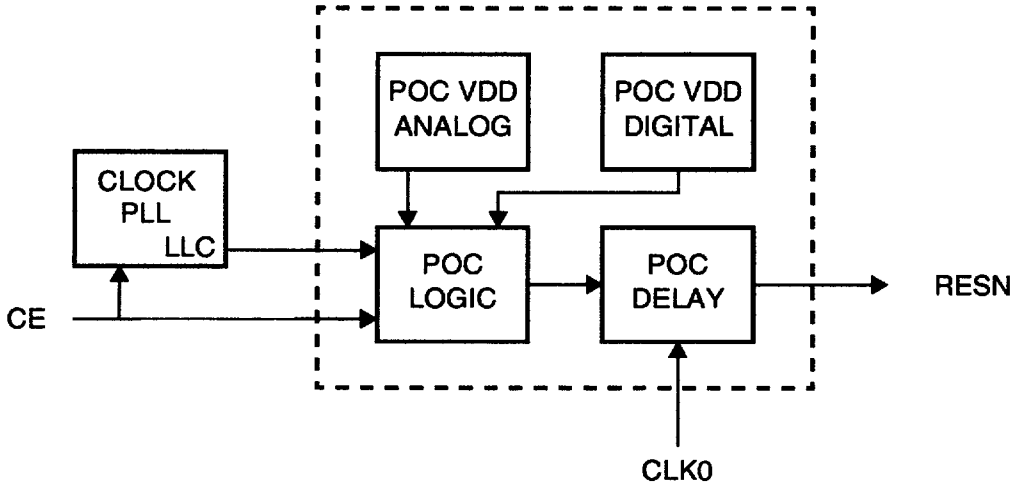


Fig.19 POWER-ON Control

INTERNAL POWER ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
DIRECTLY AFTER POWER ON ASYNCHRONOUS RESET	YPO(15:0), RTCO, RTS0, RTS1, GPSW, HREF, VREF, HS, VS, LLC, LLC2, CREF --> high impedance state	direct switching to high impedance for 20 - 200ms
SYNCHRONOUS RESET SEQUENCE	LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW, SDA become active VPO(15:0), HREF, VREF, HS, VS, --> held in high impedance state	internal reset sequence
STATUS after POWER ON CONTROL SEQUENCE	VPO(15:0), HREF, VREF, HS, VS, --> held in high impedance state	After power on (reset sequence) a complete IIC transmission is required!

Table 7 POWER-ON Control Sequence

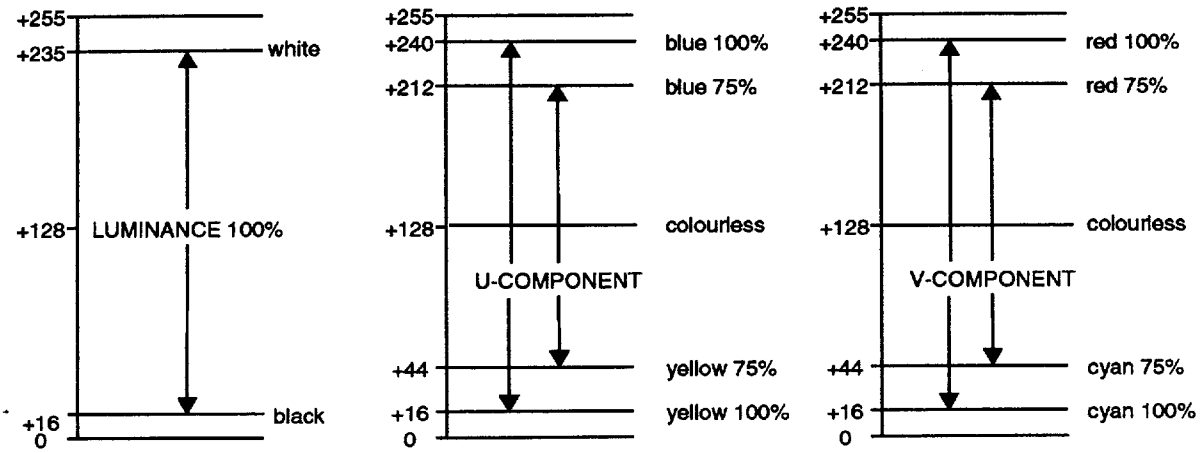
15 OUTPUT FORMATS

BUS SIGNAL	4 1 1				4 2 2 (1)		CCIR 656 (2)				RGB
	12 BIT				16 BIT		8 BIT				16 BIT
VPO15	Y_{07}	Y_{17}	Y_{27}	Y_{37}	Y_{07}	Y_{17}	U_{07}	Y_{07}	V_{07}	Y_{17}	R4
VPO14	Y_{06}	Y_{16}	Y_{26}	Y_{36}	Y_{06}	Y_{16}	U_{06}	Y_{06}	V_{06}	Y_{16}	R3
VPO13	Y_{05}	Y_{15}	Y_{25}	Y_{35}	Y_{05}	Y_{15}	U_{05}	Y_{05}	V_{05}	Y_{15}	R2
VPO12	Y_{04}	Y_{14}	Y_{24}	Y_{34}	Y04	Y_{14}	U_{04}	Y_{04}	V_{04}	Y_{14}	R1
VPO11	Y_{03}	Y_{13}	Y_{23}	Y_{33}	Y_{03}	Y_{13}	U_{03}	Y_{03}	V_{03}	Y_{13}	R0
VPO10	Y_{02}	Y_{12}	Y_{22}	Y_{32}	Y_{02}	Y_{12}	U_{02}	Y_{02}	V_{02}	Y_{12}	G5
VPO9	Y_{01}	Y_{11}	Y_{21}	Y_{31}	Y_{01}	Y_{11}	U_{01}	Y_{01}	V_{01}	Y_{11}	G4
VPO8	Y_{00}	Y_{10}	Y_{20}	Y_{30}	Y_{00}	Y_{10}	U_{00}	Y_{00}	V_{00}	Y_{10}	G3
VPO7	U_{07}	U_{05}	U_{03}	U_{01}	U_{07}	V_{07}	X	X	X	X	G2
VPO6	U_{06}	U_{04}	U_{02}	U_{00}	U_{06}	V_{06}	X	X	X	X	G1
VPO5	V_{07}	V_{05}	V_{03}	V_{01}	U_{05}	V_{05}	X	X	X	X	G0
VPO4	V_{06}	V_{04}	V_{02}	V_{00}	U_{04}	V_{04}	X	X	X	X	B4
VPO3	X	X	X	X	U_{03}	V_{03}	X	X	X	X	B3
VPO2	X	X	X	X	U_{02}	V_{02}	X	X	X	X	B2
VPO1	X	X	X	X	U_{01}	V_{01}	X	X	X	X	B1
VPO0	X	X	X	X	U_{00}	V_{00}	X	X	X	X	B0
Pixel Order Y	0	1	2	3	0	1	0		1		
Pixel Order UV	0				0		0				
Data rates	LLC2				LLC2		LLC				LLC2
I^2C - control signals	OFTS0 = 0				OFTS0 = 1		OFTS0 = 1				OFTS0 = 0
	OFTS1 = 1				OFTS1 = 0		OFTS1 = 1				OFTS1 = 0

Table 8 Output Formats

1. Values according to CCIR 601
2. Before and after the video data, video timing reference codes are inserted according to CCIR 656.

16 VPO OUTPUT SIGNAL RANGE

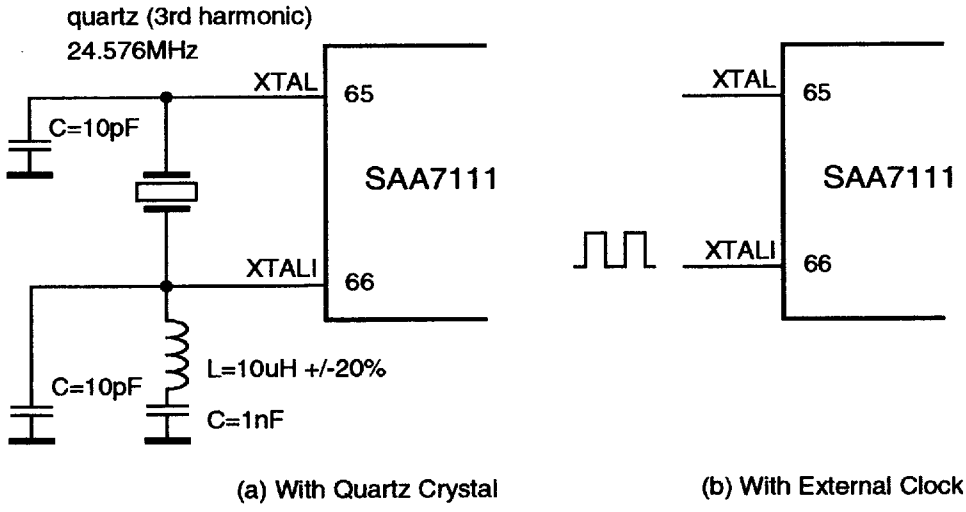


(a) Y Output Range (b) U Output Range (B-Y) (c) V Output Range (R-Y)

CCIR Rec. 601 digital levels

Fig.20 VPO Output Signal Range

17 OSCILLATOR APPLICATION



(a) With Quartz Crystal (b) With External Clock

Fig.21 Oscillator Application

18 VIP APPLICATION DIAGRAM

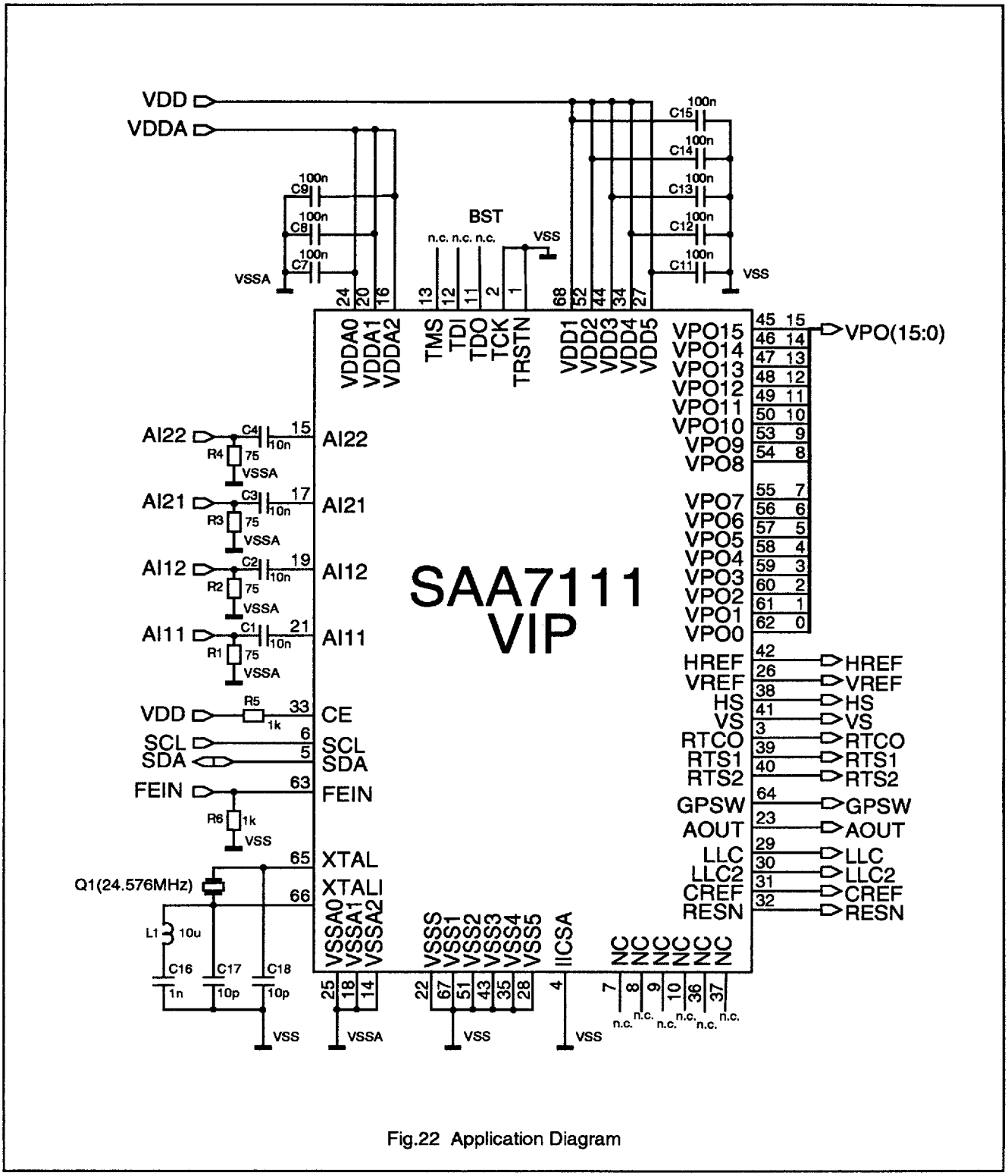


Fig.22 Application Diagram

19 IIC DESCRIPTION

19.1 IIC-BUS FORMAT

S	SLAVEADDRESS	A	SUBADDRESS	A	DATA (N BYTES)*	A	P

S	start condition		
SLAVEADDRESS	0100 100Xb (IICSA=LOW) or 0100 101Xb (IICSA=HIGH)		
A	acknowledge, generated by the slave		
SUBADDRESS	subaddress byte, see reference table		
DATA	data byte, see reference table		
P	stop condition		
X	read/write control bit X=0, order to write (the circuit is slave receiver) X=1, order to read (the circuit is slave transmitter)		
SLAVEADDRESS	read	write	IICSA
	49h 4bh	48h 4ah	0 1
SUBADDRESSES	00 h Chip version 01 h reserved for Chip version 02 h - 05 h Frontend part 06 h - 12 h Decoder part 13 h - 1E h reserved 1F h Status Byte		
* If more than one byte DATA is transmitted, then auto-increment of the subadress is performed.			

Table 9 IIC-Bus Format

19.2 IIC-BUS RECEIVER-TRANSMITTER OVERVIEW TABLE

SLAVEADDRESS		READ 49H 4BH		WRITE 48H 4AH		IICSA 0 1			
REGISTER FUNCTION	**SUB ADDR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Chip version	00	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
reserved for Chip version	01	*	*	*	*	*	*	*	*
Analog Input Control 1	02	FUSE1	FUSE0	GUDL2	GUDL1	GUDL0	MODE2	MODE1	MODE0
Analog Input Control 2	03	TEST	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	GAI28	GAI18
AICo 3	04	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
TEST=1		AIND2	AIND1	REFS2	REFS1	AINS2	AINS1	YSEL	CSEL
AICo 4	05	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
TEST=1		*	CLTSA	CLAA	CLAU	CL602	CL601	GTESE	MSBGT
Horizontal sync start	06	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync Control	08	AUFD	FSEL	EXFIL	*	VTRC	HPLL	VNOI1	VNOI0
Luminance Control	09	BYPS	PREF	BPSS1	BPSS0	VBLB	UPTCV	APER1	APER0
Luminance brightness	0A	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance Contrast	0B	*	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	0C	*	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Chroma Hue control	0D	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chroma Control	0E	CDTO	CM99	CSTD1	CSTD0	DCCF	FCTC	CHBW1	CHBW0
reserved	0F	*	*	*	*	*	*	*	*
Format/Delay Control	10	OFTS1	OFTS0	HDEL1	HDEL0	VRLN	YDEL2	YDEL1	YDEL0
Output Control	11	GPSW	*	FECO	COMPO	OEYC	OEHV	VIPB	COLO
Output Control	12	RTSE1	RTSE0	*	CBR	*	DIT	AOSL1	AOSL0
reserved	13-1E	*	*	*	*	*	*	*	*
* All unused control bits must be programmed with "0"									

Table 10 IIC-Overview

SLAVEADDRESS		READ		WRITE		IICSA			
		49H 4BH		48H 4AH		0 1			
REGISTER FUNCTION	SUB ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Status Byte	1F	STTC	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE
STTC Status Bit for locked horizontal frequency Status LOW: TV-time constant, HIGH: VCR-time-constant									
HLCK Status Bit for locked horizontal frequency.Status LOW: locked, HIGH: unlocked									
FIDT Identification Bit for detected field frequency. Status LOW: 50 Hz, HIGH: 60 Hz									
GLIMT Gain value for active luminance channel is limited (max [top]), active HIGH									
GLIMB Gain value for active luminance channel is limited (min [bottom]), active HIGH									
WIPA White peak loop is activated, active HIGH									
SLTCA Slow Time Constant Active in WIPA -mode									
CODE Status HIGH: Colour signal according to selected standard has been detected									

Table 10 IIC-Overview

19.3 IIC DETAIL

IIC-RECEIVER (SLAVE-ADDRESS 48H / 49H)								
SUBADDRESS 00 CHIP VERSION								
Chip version in readmode	CONTROL BITS							
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	0	0	0	0	0	0	0	0
	chip version number				reserved for chip name			
SUBADDRESS 01 RESERVED FOR CHIP VERSION								
SUBADDRESS 02 ANALOG CONTROL 1 (AICO1)								
MODE select								D2-D0
FUNCTION	MODE2	MODE1	MODE0					
MODE 0: CVBS (automatic gain)	0	0	0					
MODE 1: CVBS (automatic gain)	0	0	1					
MODE 2: CVBS (automatic gain)	0	1	0					
MODE 3: CVBS (automatic gain)	0	1	1					
MODE 4: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	0					
MODE 5: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	1					
MODE 6: Y (automatic gain) + C (gain channel 2 adapted to Y-gain)	1	1	0					
MODE 7: Y (automatic gain) + C (gain channel 2 adapted to Y-gain)	1	1	1					

Table 11 IIC-Detail 1

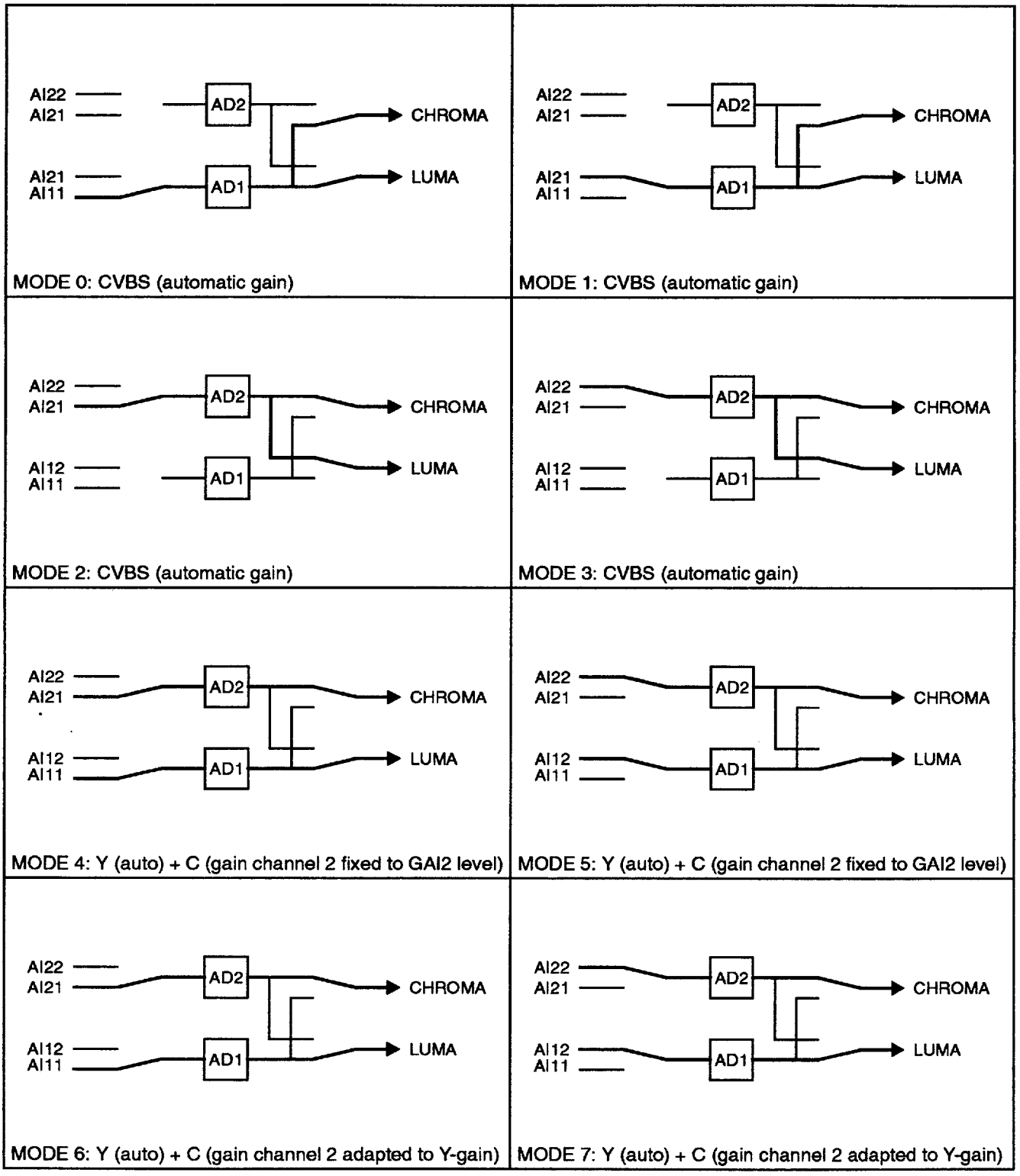


Table 12 IIC-Detail 2

DECIMAL	UPDATE HYSTERESIS for 9 bit gain	CONTROL BITS GUDL(2:0)		
		GUDL2	GUDL1	GUDL0
0...	OFF	0	0	0
... 7...	+/- 7 LSB	1	1	1
Analog function select FUSE				D7-D6
FUNCTION		CONTROL BITS FUSE(1:0)		
		FUSE1	FUSE0	
AMPLIFIER + ANTI ALIAS FILTER bypassed		0	0	
		0	1	
AMPLIFIER active		1	0	
AMPLIFIER + ANTI ALIAS FILTER active		1	1	
SUBADDRESS 03 ANALOG CONTROL 2 (AICO2)				
Static gain control channel 1 GAI18 (see SA 04)				D0
Sign bit of gain control dumping of the gain amplifier		0		
Sign bit of gain control boost of the gain amplifier		1		
Static gain control channel 2 GAI28 (see SA 05)				D1
Sign bit of gain control dumping of the gain amplifier		0		
Sign bit of gain control boost of the gain amplifier		1		
Gain control fix (GAFIX)				D2
automatic gain controlled by MODE(1:0)		0		
gain control is user programmable via GAI1 + GAI2		1		
Automatic gain control integration HOLDG				D3
AGC active		0		
AGC integration hold (freeze)		1		
White peak off (WPOFF)				D4
White peak off		1		
White peak control active		0		
Vertical blanking select (VBSL)				D5
Long vertical blanking		0		
Short vertical blanking		1		
HL Not Reference Select (HLNRS)				D6
Normal clamping by HLnot		0		
Reference Select by HLnot		1		
Switch in analog TEST environment				D7
TEST active		1		
normal application		0		

Table 13 IIC-Detail 3

SUBADDRESS 04 GAIN CONTROL ANALOG (AICO3)										
Static gain control channel 1 GAI1										D7-D0
DECIMAL value	GAIN	sign bit	CONTROL BITS							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0...	- 5.98 dB	0	0	0	0	0	0	0	0	0
....255	0 dB	0	1	1	1	1	1	1	1	1
256...	0 dB	1	0	0	0	0	0	0	0	0
... 511	5.98 dB	1	1	1	1	1	1	1	1	1
TEST ENVIRONMENT SUBADDRESS 04										
Chrominance select CSEL										D0
AD converter 2 -> CHR						0				
AD converter 1 -> CHR						1				
Luminance select YSEL										D1
AD converter 1 -> CVBS						0				
AD converter 2 -> CVBS						1				
Analog input select 1 AINS1										D2
Analog input AI12 selected						0				
Analog input AI11 selected						1				
Analog input select 2 AINS2										D3
Analog input AI22 selected						0				
Analog input AI21 selected						1				
Reference select channel 1 REFS1										D4
Automatic clamping active						0				
Reference level selected						1				
Reference select channel 2 REFS2										D5
Automatic clamping active						0				
Reference level selected						1				
Analog input disable 1 AIND1										D6
Analog inputs 1 enabled						0				
Analog inputs 1 disabled						1				
Analog input disable 2AIND2										D7
Analog inputs 2 enabled						0				
Analog inputs 2 disabled						1				

Table 13 IIC-Detail 3

SUBADDRESS 05 GAIN CONTROL ANALOG (AICO4)										
Static gain control channel 2 GAI2										D7-D0
DECIMAL value	GAIN	sign bit	CONTROL BITS							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0...	- 5.98 dB	0	0	0	0	0	0	0	0	0
....255	0 dB	0	1	1	1	1	1	1	1	1
256...	0 dB	1	0	0	0	0	0	0	0	0
... 511	5.98 dB	1	1	1	1	1	1	1	1	1
TEST ENVIRONMENT SUBADDRESS 05										
MSB for Gain Test (MSBGT)										D0
Internal source of the MSB for gain						0				
External source of the MSB for gain						1				
Gain TESt Enable (GTESE)										D1
Internal Gainloop active						0				
External Gainvalues selected						1				
Clamplevel 60 for channel 1 (CL601)										D2
Clamp level 128						0				
Clamp level 60						1				
Clamplevel 60 for channel 2 (CL602)										D3
Clamp level 128						0				
Clamp level 60						1				
Clamp level for channel 1 (CLAU)										D4
Clamp up						1				
Clamp down						0				
Clamping active for channel 1 (CLAA)										D5
on						1				
off						0				
CLamp TeSt Active 1 (CLTSA)										D6
External source for gain values selected						1				
Normal gainloop active						0				
SUBADDRESS 06 HORIZONTAL SYNC BEGIN										D7-D0
DELAY TIME (STEP SIZE =8/LLC)			HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
+ 255			0	1	1	1	1	1	1	1
- 256			1	0	0	0	0	0	0	0
SUBADDRESS 07 HORIZONTAL SYNC STOP										D7-D0
DELAY TIME (STEP SIZE =8/LLC)			HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
+ 255			0	1	1	1	1	1	1	1
- 256			1	1	1	1	1	1	1	1

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SUBADDRESS 08 SYNC CONTROL		
Vertical noise reduction VNOI		D1-D0
FUNCTION	CONTROL BITS	
	VNOI1	VNOI0
Normal mode	0	0
Searching mode	0	1
Free running mode	1	0
Vertical noise reduction bypassed	1	1
Horizontal PLL clock HPLL		D2
PLL closed	0	
PLL open, horizontal frequency fixed	1	
TV/VCR-mode select VTRC		D3
TV mode	0	
VTR mode	1	
Extended LoopFILter (EXFIL)		D5
Wordwidth of the loopfilter (LF2) amplification = 14 bit	0	
Wordwidth of the loopfilter (LF2) amplification = 16 bit	1	
Field SELection (FSEL)		D6
50 Hz, 625 lines	0	
60 Hz, 525 lines	1	
AUtomatic Field Detection (AUFD)		D7
Field state direct controlled via FSEL	0	
Automatic field detection	1	
SUBADDRESS 09 LUMA CONTROL		
APERture factor (APER)		D1-D0
APERTURE FACTOR	CONTROL BITS	
	APER1	APER0
0	0	0
0.25	0	1
0.5	1	0
1	1	1
Update time interval for analog gain control value (UPTCV)		D2
horizontal update (once per line)	0	
vertical update (once per field	1	
Vertical Blanking Luma Bypass (VBLB)		D3
Active LUMA processing	0	
LUMA bypass	1	

Table 13 IIC-Detail 3

aperture BandPaSS (centre frequency) BPSS		D5-D4
BANDPASS CENTER FREQ.	CONTROL BITS	
centre frequency	BPSS1	BPSS0
4.1 MHz	0	0
3.8 MHz	0	1
2.6 MHz	1	0
2.9 MHz	1	1

PREFilter active (PREF)	D6
Bypassed	0
Active	1

chrominance trap BYPaSs BYPS		D7
CHROMA TRAP	MODE	CONTROL BITS
Active	CVBS	0
Bypassed	S-Video	1

SUBADDRESS 0A LUMINANCE BRIGHTNESS CONTROL (BRIG0 -BRIG7)								D7-D0
OFFSET	CONTROL BITS							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
128 (CCIR-level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

SUBADDRESS 0B LUMINANCE CONTRAST CONTROL (CONT0 -CONT6)								D6-D0
GAIN	CONTROL BITS							
		CONT 6	CONT 5	CONT 4	CONT 3	CONT 2	CONT 1	CONT 0
1.999 (MAXIMUM)		1	1	1	1	1	1	1
1.109 (CCIR-level)		1	0	0	0	1	1	1
1		1	0	0	0	0	0	0
0 (LUMINANCE OFF)		0	0	0	0	0	0	0

SUBADDRESS 0C CHROMINANCE SATURATION CONTROL (SATN0-SATN6)								D6-D0
GAIN	CONTROL BITS							
		SATN 6	SATN 5	SATN 4	SATN 3	SATN 2	SATN 1	SATN 0
1.999 (MAXIMUM)		1	1	1	1	1	1	1
1 (CCIR-level)		1	0	0	0	0	0	0
0 (COLOUR OFF)		0	0	0	0	0	0	0

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SUBADDRESS 0D CHROMINANCE HUE CONTROL (HUEC0-HUEC7)								D7-D0
HUE PHASE (DEG)	CONTROL BITS							
	HUEC 7	HUEC 6	HUEC 5	HUEC 4	HUEC 3	HUEC 2	HUEC 1	HUEC 0
+178.6...	0	1	1	1	1	1	1	1
... 0...	0	0	0	0	0	0	0	0
... -180	1	0	0	0	0	0	0	0

SUBADDRESS 0E CHROMINANCE CONTROL			
Chroma bandwidth (CHBW0-CHBW1)			D1-D0
BANDWIDTH	CONTROL BITS		
	CHBW1	CHBW0	
small (≈ 620 kHz)	0	0	
nominal (≈ 800 kHz)	0	1	
medium (≈ 920 kHz)	1	0	
wide (≈ 1000 kHz)	1	1	
Fast Colour Time Constant (FCTC)			D2
nominal Time constant	0		
fast Time constant	1		
Disable Chroma Combfilter (DCCF)			D3
Chroma combfilter on (during VREF = 1) see figure 17	0		
Chroma combfilter off	1		
Colour Standard (CSTD0 - CSTD1)			D5-D4
colour standard control automatic switching between	CONTROL BITS		
	CSTD1	CSTD0	
PAL BGHI and NTSC M	0	0	
NTSC 4.43 (50Hz) and PAL4.43 (60Hz)	0	1	
PAL N and NTSC 4.43 (60Hz)	1	0	
NTSC N and PAL M	1	1	
CM99 Compatibility to SAA7199			D6
Default value	0		
To be set, if SAA7199 (digital encoder) is used for re-encoding in conjunction with RTCO	1		
Clear DTO (CDTO)			D7
disabled	0		
Every time CDTO is set, the internal subcarrier DTO phase is reset to 0 degree and the RTCO-output generates a "0" at time slot 68 (see RTCO-description). So an identical subcarrier phase can be generated by an external device (e. g. encoder).	1		
SUBADDRESS 0F RESERVED			

Table 13 IIC-Detail 3

SUBADDRESS 10 FORMAT/DELAY CONTROL								
Luminance delay compensation YDEL								D2-D0
LUMINANCE DELAY COMPENSATION (steps in 2/LLC)	CONTROL BITS							
	YDEL2		YDEL1		YDEL0			
0	0		0		0			
3	0		1		1			
-4	1		0		0			
VRLN VRef-position and LeNgth								D3
VRLN	VREF at 60 Hz/525 lines *				VREF at 50 Hz/625 lines *			
	0		1		0		1	
length	240		242		286		288	
line no.	first	last	first	last	first	last	first	last
FIELD 1	19 (22)	258 (261)	18 (21)	259 (262)	24	309	23	310
FIELD 2	282 (285)	521 (524)	281 (284)	522 (525)	337	622	336	623
* Line numbers in Brackets refer to CCIR line counting								
Fine position of HS (HDEL0 - HDEL1)								D5-D4
Fine position of HS with a step size = 2/LLC	CONTROL BITS							
	HDEL1				HDEL0			
0	0				0			
1	0				1			
2	1				0			
3	1				1			
Output Format Selection (OFTS0 - OFTS1)								D7-D6
Formats	CONTROL BITS							
	OFTS1				OFTS0			
RGB 565	0				0			
YUV 422 16 bits	0				1			
YUV 411 12 bits	1				0			
YUV CCIR 656 8bits	1				1			
SUBADDRESS 11 OUTPUT CONTROL								
Colour on (COLO)								D0
Automatic colour killer	0							
Colour forced on	1							
Decoder VIP Bypassed (VIPB)								D1
DMSD-data to YUV output	0							
A/D-data to YUV output	1							

Table 13 IIC-Detail 3

Output Enable Horizontal/Vertical sync (OEHV)		D2
HS, HREF,VREF and VS high impedance/inputs	0	
Output HS, HREF, VREF and VS active	1	
Output Enable YUV-data (OEYC)		D3
VPO-bus high impedance/input	0	
Output VPO-bus active	1	
Inverse composite blank (COMPO)		D4
VREF is vertical reference	0	
VREF is inverse composite blank	1	
FEin COntrol (FECO)		D5
FEIN sampling at CREF = low (SAA7110 compatible, see Fig.12)	0	
FEIN sampling at CREF = high	1	
General Purpose SWitch (GPSW)		D7
switches directly pin 64 GPSW	0	
	1	
SUBADDRESS 12 OUTPUT CONTROL		
AnalOg test SeLect (AOSL)		D1-D0
FUNCTION	AOSL1	AOSL0
AOUT connected to ground	0	0
AOUT connected to input AD1	0	1
AOUT connected to input AD2	1	0
AOUT connected to ground	1	1
DIThering (noise shaping) control (DIT)		D2
Dithering off	0	
Dithering on	1	
Chroma Interpolation filter function (CBR)		D4
cubic interpolation (default)	0	
linear interpolation (lower bandwidth)	1	
Real-Time-outputs-mode SElect (RTSE0)		D6
ODD switched to output pin 40	0	
VL switched to output pin 40	1	
Real-Time-outputs-mode SElect (RTSE1)		D7
PLIN switched to output pin 39	0	
HL switched to output pin 39	1	
SUBADDRESS 13 - 1E RESERVED		

Table 13 IIC-Detail 3