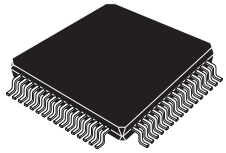
STLC1511

NorthenLite™ G.lite BiCMOS Analog Front-End Circuit

PRODUCT PREVIEW

- Wide transmit (~80dB) and receive (~69dB) dynamic range to limit the external filtering requirements for extended loop reach operation
- Programmable tx gain: 0 ÷ -32dB in 2dB steps
- 14-bit D/A converter in transmit path
- Programmable rx gain: 0 ÷40dB in 0.5dB steps
- 12-bit A/D converter in receive path
- Integrated phase-locked loop with an externall LC or crystal oscillator
- Low power: 300mW @ 5.0V
- 64-pin TQFP package



TQFP64
ORDERING NUMBER: STLC1511

1.0 GENERAL DESCRIPTION

The STLC1511 G.lite Analog Front End (AFE) chip implements the analog transceiver functions required in both a central office modem and a customer premise modem. It connects the digital modem chip with the loop driver and hybrid balance circuits. The STLC1511 has been designed with excellent dynamic range in order to greatly reduce the external filtering requirements at the front end. The AFE chip and its companion digital chip along with a loop driver, implement the complete G.992.2 DMT modem solution.

The STLC1511 transmit path consists of a 14-bit Nyquist rate D/A converter, followed by a programmable gain amplifier (TxPGA). The transmit gain is programmable from 0 to -32dB in 2dB steps.

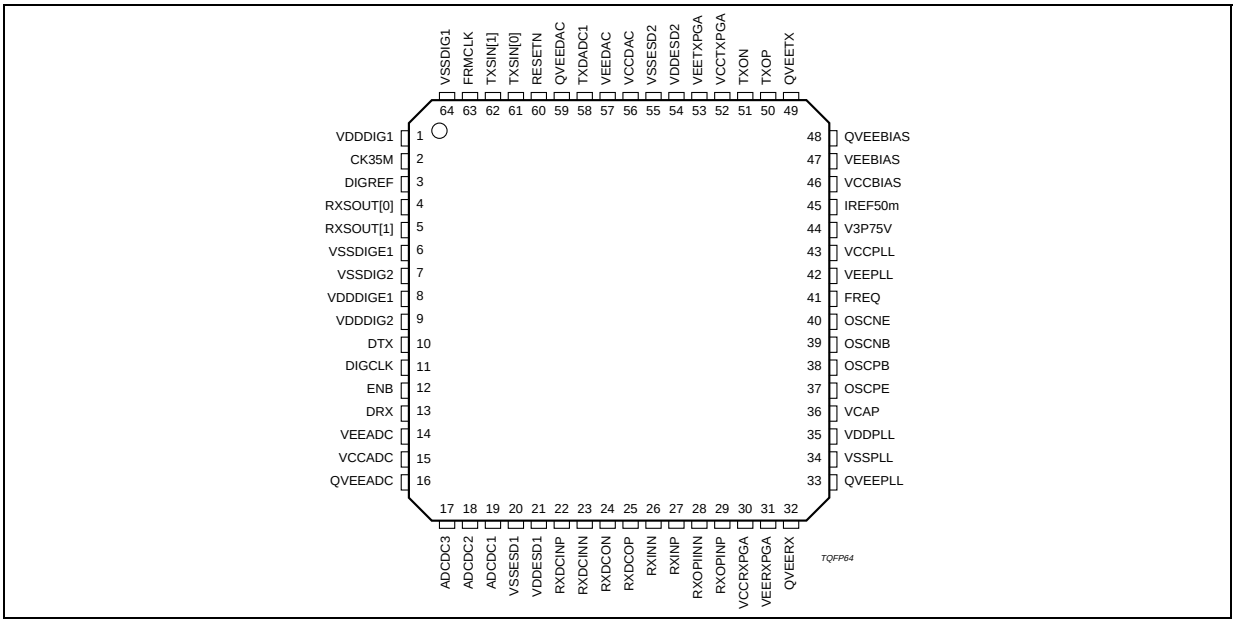
The STLC1511 receive path contains a buffer amplifier followed by a programmable gain amplifier (RxPGA), a low pass anti-aliasing filter, and a 12-bit Nyquist rate A/D converter. The RxPGA is digitally programmable from 0 to 40dB in 0.5dB steps.

2.0 PACKAGING AND PIN INFORMATION

2.1 STLC1511 Pin Allocation

The pinout for the STLC1511 is depicted in Figure 1.

Figure 1. STLC1511 pinout



2.2 Pin Description

Table 1. details the pinout assignment for the STLC1511. The following list gives the different pin types for the STLC1511.

- VDD/VCC - 5V power supply
- VEE/VSS - Ground supply
- DO/DI - Digital Output/ Digital Input
- AO/AI/AIO - Analog Output/ Analog Input/ Analog Input-Output

Table 1. Pin Assignement

Pin #	Pin Name	Pin Type	Pad Type	Description
1	VDDDIG1	VDD	VDDCO	5V supply (digital) for ADC and DAC
2	CK35M	DI	TLCHT	35.328MHz serial interface clock input (also used in Test Mode to test PFD. See Table on page 21)
3	DIGREF	DO	BT4CR	35.328/17.644MHz reference for Digital ASIC PLL
4	RXSOUT[0]	DO	BT4CR	Rx serial data (lsb) output
5	RXSOUT[1]	DO	BT4CR	Rx serial data (msb) output
6	VSSDIGE1	VSS	VSSE	Ground for digital output drivers
7	VSSDIG2	VSS	VSSCO	Ground supply for digital interface, serial interface
8	VDDDIGE1	VDD	VDDE	5 V supply for digital output drivers[1]
9	VDDDIG2	VDD	VDDCO	5 V supply for digital interface, serial interface
10	DTX	DO	BT4CR	Data Output for digital interface
11	DIGCLK	DI	TLCHT	35.328MHz clock input for digital interface
12	ENB	DI	TLCHT	Enable input for digital interface
13	DRX	DI	TLCHT	Data Input for digital interface
14	VEEADC	VEE	VSSCO	Ground for ADC
15	VCCADC	VCC	VDDCO	5 V supply for ADC
16	QVEEADC	VEE	VSSCO	Quiet ground for ADC circuitry
17	ADCDC3	AIO	ANA	ADC reference decoupling (3.75 V) 0.1uF
18	ADCDC2	AIO	ANA	ADC reference decoupling (2.5 V) 0.1uF
19	ADCDC1	AIO	ANA	ADC reference decoupling (1.25 V) 0.1uF
20	VSSESD1	VSS	VSSA	Ground for ESD ring
21	VDDESD1	VDD	VDDA	5 V supply for ESD ring
22	RXDCINP	AI	ANA	RxPGA positive input from DC blocking capacitor
23	RXDCINN	AI	ANA	RxPGA negative input from DC blocking capacitor
24	RXDCON	AO	ANA	RxPGA negative output to DC blocking capacitor
25	RXDCOP	AO	ANA	RxPGA positive output to DC blocking capacitor
26	RXINN	AI	ANA	Rx negative input (AC coupled)
27	RXINP	AI	ANA	Rx positive input (AC coupled)

Table 1. Pin Assignement

Pin #	Pin Name	Pin Type	Pad Type	Description
28	RXOPINN	AI	ANA	Rx opamp negative input (must be DC coupled)
29	RXOPINP	AI	ANA	Rx opamp positive input (must be DC coupled)
30	VCCRXPGA	VCC	VDDCO	5V supply for RxPGA
31	VEERXPGA	VEE	VSSCO	Ground for RxPGA
32	QVEERX	VEE	VSSCO	Quiet ground for Rx circuitry
33	QVEEPLL	VEE	VSSCO	Quiet ground for PLL circuitry
34	VSSPLL	VSS	VSSCO	Ground for Oscillator[2]
35	VDDPLL	VDD	VDDCO	5 V supply for Oscillator[2]
36	VCAP	AO	ANA	Charge pump output to varactor
37	OSCPE	AIO	ANA	Oscillator I/O (emitter)
38	OSCPB	AIO	ANA	Oscillator I/O (base)
39	OSCNB	AIO	ANA	Oscillator I/O (base)
40	OSCNE	AIO	ANA	Oscillator I/O (emitter)
41	FREF	AI	ANA	2.56 MHz PLL input reference/ 35.328 MHz clock input
42	VEEPLL	VEE	VSSCO	Ground for oscillator[2]
43	VCCPLL	VCC	VDDCO	5 V supply for oscillator[2]
44	V3P75V	AIO	ANA	3.75V output from Bandgap to 0.22mF capacitor
45	**IREF50**m	AIO	ANA	External resistor for bias current R=2.5V/ 50mA=50kohm
46	VCCBIAS	VCC	VDDCO	5V supply for biasing
47	VEEBIAS	VEE	VSSCO	Ground for biasing
48	QVEEBIAS	VEE	VSSCO	Quiet ground for bias circuitry
49	QVEETX	VEE	VSSCO	Quiet ground for Tx circuitry
50	TXOP	AO	ANA	Tx positive output
51	TXON	AO	ANA	Tx negative output
52	VCCTXPGA	VCC	VDDCO	5V supply for TxPGA
53	VEETXPGA	VEE	VSSCO	Ground for TxPGA
54	VDDESD2	VDD	VDDA	5V supply for ESD ring
55	VSSESD2	VSS	VSSA	Ground for ESD ring
56	VCCDAC	VCC	VDDCO	5V supply for DAC
57	VEEDAC	VEE	VSSCO	Ground for DAC
58	TXDADC1	AIO	ANA	DAC reference (2.5V) 0.1uF

Table 1. Pin Assignement

Pin #	Pin Name	Pin Type	Pad Type	Description
59	QVEEDAC	VEE	VSSCO	Quiet ground for DAC circuitry
60	RESETN	DI	TLCHT	ResetN for the AFE
61	TXSIN[0]	DI	TLCHT	Tx serial data (lsb) input
62	TXSIN[1]	DI	TLCHT	Tx serial data (msb) input
63	FRMCLK	DO	BT4CR	Tx 4.416MHz frame clock reference output
64	VSSDIG1	VSS	VSSCO	Ground (digital) for ADC and DAC

<1>HCMOS5 guidelines are for 1 pair of power/ground for 4 output drivers (4mA)

<2>Pins 35 and 43 are both connected to the analog VCC supplying the on chip oscillator. Similarly, Pins 34 and 42 are connected to analog VSS for the oscillator. Supply line inductance is reduced using two pads for VCC (and VSS) in this manner. At the board level, Pins 35 and 43 should be connected to analog VCC, and pins 34 and 42 should be connected to analog VSS.

3.0 FUNCTIONAL DESCRIPTION

3.1 General Functional Description

The STLC1511 consists of the following functional blocks:

- Transmit Signal Path
- Receive Signal Path
- Phase Lock Loop and Amplifier for an external oscillator.
- Bias Voltage and Current Generation
- Digital Interface
- Serial Interface

The transmit path contains the 14-bit digital to analog converter (DAC) necessary to generate the transmit signal from a 14-bit digital input word. This transmit signal is then scaled by the on chip programmable gain amplifier (TxPGA) from 0 to -32dB in 2dB steps. The scaled output signal is then driven off chip to the external filters and power amplifier (PA) which drives the DMT signal to the subscriber loop. The transmit path is fully differential but may be used single ended if both outputs from the TxPGA are terminated correctly.

The receive path contains an optional unity gain buffer followed by a two stage programmable gain amplifier (RxPGA), a 1st order low pass anti-aliasing filter, and a 12-bit analog to digital converter (ADC). The RxPGA consists of two stages and the gain is digitally programmable from 0 to 40dB in 0.5dB steps. The receive path is fully differential but may be used single ended provided the other input to the RxPGA is grounded.

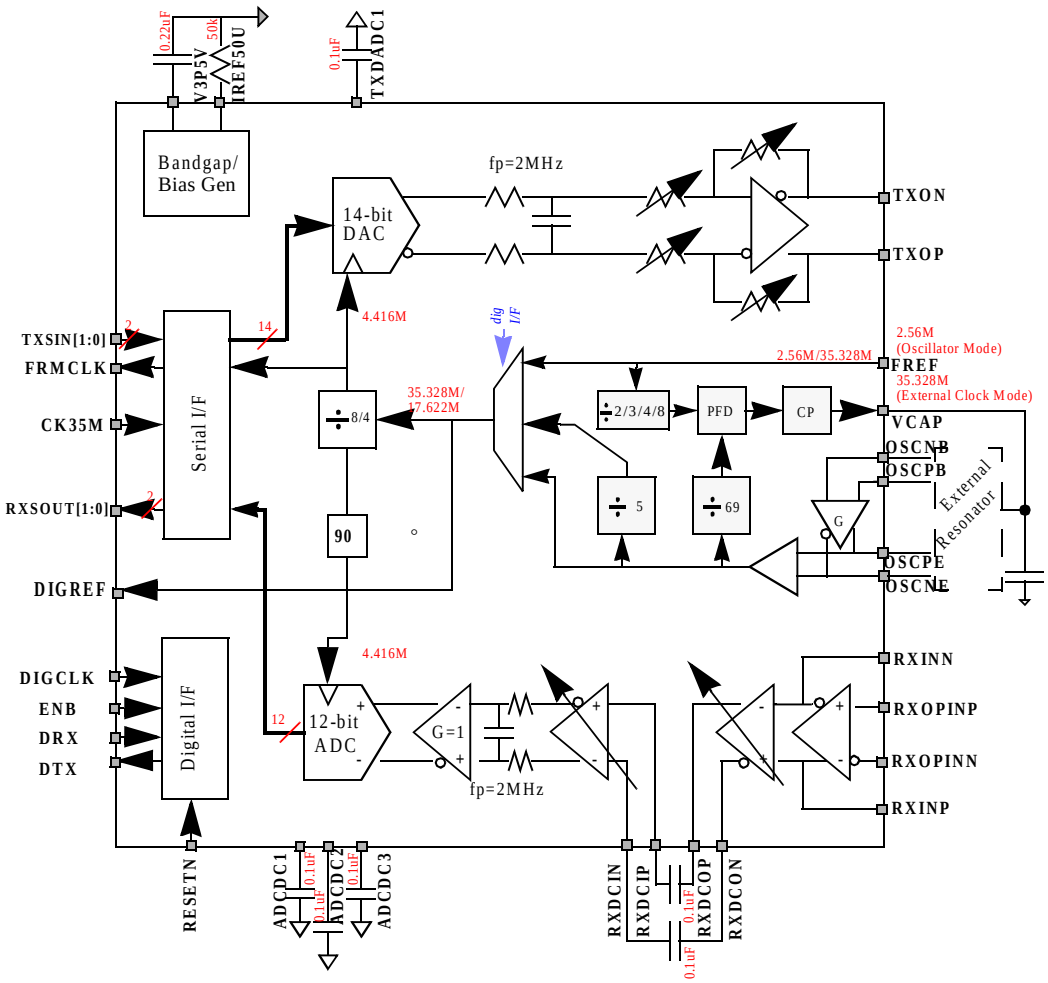
The STLC1511 contains the circuits required to construct a PLL that generates either a 17.644MHz/ 35.328 MHz clock from a 2.56 MHz reference clock when supplied with an external LC or crystal oscillator and tuning circuit. This clock is supplied to the both the transmit and receive converters, and the serial interface used to transfer the Rx/Tx data between the STLC1511 and digital chip. The STLC1511 also has the ability to be driven directly by an external 35.328MHz clock supplied to the FREF pin.

The bias circuitry contains a bandgap voltage reference from which the converter references and analog ground voltage is generated. This block also generates an accurate current using an external resistor from which all of the STLC1511 circuits are biased. In addition, the bias circuitry also generates a 2.5V reference for the external Vco/Vcxo components and can be used for other external circuits if necessary.

There is a 4 pin serial digital interface (**DTX, DRX, DIGCLK, ENB**) that loads a one of four 8-bit control register that controls all the programmable features on the STLC1511. Refer to “Digital Interface And Memory Map” on page 20 for more information on the programmability of the AFE.

To facilitate data transfer between the STLC1511 and the digital ASIC (STLC1510), a 2-bit wide serial interface for the transmit path and a 2-bit wide serial interface for the receive path is incorporated into the AFE. This interface consists of two transmit pins (**TXSIN[0:1]**), two receive pins (**RXSOUT[1:0]**), and the necessary control signals (**FRMCLK, CK35M**) to transmit the required data. For more information See “Serial Interface” on page 18.

Figure 2. The block diagram of the STLC1511



Shaded blocks are only usabe when the PLL is active. Crystal based external resonator for the CPE Mode, LC based resonator for the CO Oscillator Mode. 35.328 MHz external reference in CO External Clock Mode.

3.2 Receive Path Specifications

Note: The first stage of the RxPGA provides a coarse gain of 0/20dB with a differential input or 6/26dB with a single ended input. The second stage implements a programmable gain from 0dB to 20dB in 0.5dB steps.

Table 2. Receive Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5.0Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC±±5%, -40=<$T_{junction}$=<105×C, and worst case process.

Description	min	typ	max	Units	Comments
1st Stage Absolute Gain[1] [2] Diff in to Diff out [3] D = 00 D = 01 Single ended in to Diff out [3] D = 10 D = 11		 0 20 6 26		 dB dB	Where "D" is the binary value in b[7:6] of the control word. Includes Vcc, temperature, process, and frequency variation.
2nd Stage Absolute Gain[1] [2] Diff in to Diff out [4] 0 =< D =< 40 D > 40	 (0.5 · D) - 1.8 18.2	 (0.5 · D) 20	 (0.5 · D) + 0.8 20.8	 dB	Where "D" is the binary value in b[5:0] of the control word. Includes Vcc, temperature, process, and frequency variation.
Relative Gain Accuracy[5] (relative to ideal gain of 0.5dB per LSB change.)	 -0.4		 +0.4	 dB	For more than a 1LSB change in the control word. Assumes a fixed Vcc, temperature, and frequency.
Gain Variation with Temperature[6]	-0.3		+0.3	dB	For a fixed Vcc and frequency f (30kHz =< f =< 540kHz) relative to 27°C.
Gain Variation with Supply Voltage[7]	-0.1		+0.1	dB	For a fixed frequency f. (30kHz =< f =< 540kHz) and fixed temperature relative to Vcc=5.0V.
Gain Variation with Frequency[8] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 -1.0 -1.0		 0 0	 dB	For a fixed Vcc and temperature. relative to 30kHz relative to 155kHz
Gain Step Size For all steps except step 19.5 to 20dB (differential) or step 25.5 to 26dB (single ended) For step 19.5 to 20dB (differential) or step 25.5 to 26dB (single ended)	0.4 0.3	0.5 0.5	0.6 0.7	dB dB	For a 1 LSB change in the control word at a fixed frequency f. (30kHz =< f =< 540kHz)

Table 2. Receive Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5.0Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC±±5%, -40=<$T_{junction}$=<105×C, and worst case process.

Description	min	typ	max	Units	Comments
Input Referred Noise[9 10 11 12] at G=0dB at G=max[13] at G=0dB at G=max[11]		250 15 250 20	252 19 252 27	$\frac{nV}{\sqrt{Hz}}$	spot noise @30Khz measured single ended at RXINP or RXINN spot noise @30kHz measured differentially at RXINP/N
Input Referred Noise[9 10 11] at G=0dB at G=max[11]		250 20	252 27	$\frac{nV}{\sqrt{Hz}}$	spot noise @30kHz measured differentially at RXDCINP/N
Op amp Input Referred Noise[9 10 11]		10	15	$\frac{nV}{\sqrt{Hz}}$	spot noise @30kHz measured differentially at RXOPINP/N
Output Signal to Distortion ratio Two tone (ATE testing)[14] DS Multi tone[15] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz US Multi-tone[16] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 60 63 63 63 63	 66 69 69 69 69		dB	 For all RxPGA gain. Measured at output of ADC
Input Impedance @pins **RXOPINP/N** @ pins **RXINP/N** @ pins **RXDCIP/N**	 250 1 1		 1000 19 10	kW	 Rx Opamp input pins Rx PGA input pins Rx AC coupling pins
DC Offset at output			15	mV	measured at output of ADC
Max Input Signal Level single ended differential			 1.2 2.4	 Vpeak Vpeak	 single-ended input differential input measured at any input (RXINP/N, RXOPINP/N, or RXDCINP/N)
Settling Time[17]			300	nsec	Time for PGA to settle to 3t accuracy after a change in the control word indicated by **ENB** going high.

Table 2. Receive Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5.0Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC±±5%, -40=<$T_{junction}$=<105×C, and worst case process.

Description	min	typ	max	Units	Comments
Power Up Time[18] Rx @ DS[19] Rx @ US[20]			 100 530	 mse c	Time to meet output SNR requirement

<1>For the purposes of this specification, a gain of 1 or 0dB is defined as the ratio of the full scale ADC output word to the input voltage at RXINP/RXINN when the input to the Rx path is at 2.4Vp differential measured between RXINP and RXINN.

<2>For G.lite the STLC1511 will support both CO and CPE applications. As such it needs to support rates from 30kHz to 120kHz (CO Receive band) and 155kHz to 540kHz (CPE Receive band).

<3>First stage gain is measured from RXINP/RXINN (differential input) to RXOP/RXON (differential output). Note that the gain from input to output can be adjusted for single ended input or differential input so that the output signal level at the output of the first stage of the PGA is at full scale. For a single ended input, the unused input, either RXINP or RXINN must be ac coupled to ground.

<4>Second stage gain is measured from RXDCINP/RXDCINN (differential input) to the output of the ADC.

<5>Will be tested at Vcc=5.0V, 27^{o}C, and f=275kHz.

<6>Will be tested at Vcc=5.0V and f=275kHz.

<7>Will be tested at 27^{o}C and f=275kHz.

<8>Will be tested at Vcc=5.0V and 27^{o}C.

<9>Due to 1/f component, the spot noise is maximum at 30kHz over the bands of interest (US and DS).

<10>Noise voltage is specified as the noise spectral density (e_n) at the input. Conversion to power spectral density is as follows

$$PSD = 10 \times \log\left(\frac{en^2}{100} \times 1000\right)$$

<11>Input referred noise assumes that there is a 7dB cut in the first band of aliased noise which falls into the DMT frequencies and that higher order aliases are negligible. For example, the single ended input referred noise for the maximum gain setting of 40dB is calculated as follows:

$$en = \sqrt{\left(1 + \frac{1}{10^{7/20}}\right)\left((17nV/\sqrt{Hz})^2 + \left(\frac{17nV/\sqrt{Hz}}{10^{20/20}}\right)^2\right) + \left(\frac{250nV/\sqrt{Hz}}{10^{40/20}}\right)^2}$$

In general, the single ended input referred noise can be calculated as follows:

$$en = \sqrt{\left(1 + \frac{1}{10^{7/10}}\right)\left((17n\dot{V}/Hz)^2 + \left(\frac{17nV/\sqrt{Hz}}{10^{G1/20}}\right)^2\right) + \left(\frac{250nV/\sqrt{Hz}}{10^{(G1+G2)/20}}\right)^2}$$

where G1 and G2 are the gains of the first and second stages of the RxPGA respectively. Note that the assumption of a 7dB cut on the aliased noise is also used in the above formula and that all other higher order noise is sufficiently suppressed.

<12>Note that the Rx path noise at 0dB gain is dominated by the quantization noise of the ADC and as such there is very little process, vcc, or temperature dependency and the variation from typical to maximum noise is only due to the Rx PGA.

<13>At maximum gain PGA and Rx input opamp noise are the dominant contributors.

<14>Two tone distortion is measured with two sinewaves with each sinewave at an amplitude of 1/2 full scale. Tone one is at f1=400kHz and tone two is at f2=500kHz. The two tone distortion requirement is measured from the rms voltage of a single signal tone to the peak rms voltage of the distortion products.

<15>A multi-tone sine wave is used for the DS Multi-tone test. (The multi-tone signal will be 89 sinewaves equally spaced from 36*4.3125kHz to 125*4.3125kHz with a peak-to-rms ratio of 5.3V/V and an rms voltage equal to 1/5.3 of the peak full scale range of the PGA.) Multi-tone test measures the difference between the rms voltage of a single tone at the output to the rms voltage of the peak distortion product at the output in the band of interest.

<16>A multi-tone sine wave is used for the US Multi-tone test. (The multi-tone signal will be 22 sinewaves equally spaced from 7*4.3125kHz to 28*4.3125kHz with a peak-to-rms ratio of 5.3V/V and an rms voltage equal to 1/5.3 of the peak full scale range of the PGA.) Multi-tone test measures the difference between the rms voltage of a single tone at the output to the rms voltage of the peak distortion product at the output in the band of interest.

<17>The 1t settling time is roughly equivalent to the unity gain frequency of the PGA block.

<18>The power up time is the time it takes the power up transient to dissipate such that the output SNR specification is met. This time is dominated by the coupling capacitors at pins **RXINP/N** and **RXDCIP/N**.

<19>Minimum DS frequency is 36*4.3125kHz=155.25kHz and as such the coupling capacitors between **RXINP/N** and **RXDCIP/N** must be such that the high pass pole is ~15kHz (typical). With a 1kW minimum input impedance at **RXDCIP/N** this gives a capacitor value of about 10nF. This gives a 1t settling time of 10ms.To guarantee 12-bit performance a minimum of 10t settling gives 100ms.

<20>Minimum DS frequency is 7*4.3125kHz=30.1875kHz and as such the coupling capacitors between **RXINP/N** and **RXDCIP/N** must be such that the high pass pole is ~3kHz (typical). With a 1kW minimum input impedance at **RXDCIP/N** this gives a capacitor value of about 53nF. This gives a 1t settling time of 53ms.To guarantee 12-bit performance a minimum of 10t settling gives 530ms.

3.3 TRANSMIT PATH SPECIFICATIONS

Table 3. Transmit Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5 Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC ±5%, -40 =< $T_{junction}$ =< 105×C, and worst case process.

Description	min	typ	max	Units	Comments
Absolute Gain[1] [2] 0 =< D =< 16 D > 16	-(2 · D) - 1.8 -33.8	-(2 · D) -32.0	-(2 · D) - 1.0 -31.0	dB	Where “D” is the binary value in b[11:7] of the control word. Includes Vcc, temperature, process, and frequency variation.
Gain Step Size	1.8	2.0	2.2	dB	For a 1 LSB change in the control word at a fixed frequency f (30kHz =< f =< 540kHz)
Relative Gain Accuracy[3] (relative to ideal gain of 2dB per step.)	-0.4		+0.4	dB	For more than a 1LSB change in the control word. Assumes a fixed Vcc, temperature, and frequency.
Gain Variation with Temperature[4]	-0.3		0.3	dB	For a fixed Vcc and frequency f (30kHz =< f =< 540kHz) relative to 27^{o}C.
Gain Variation with Supply Voltage[5]	-0.1		0.1	dB	For a fixed frequency f. (30kHz =< f =< 540kHz) and fixed temperature relative to Vcc=5.0V.
Gain Variation with Frequency[6] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 -0.6 -1.0		 0 0	dB	For a fixed Vcc and temperature. relative to 30kHz relative to 155kHz

Table 3. Transmit Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5 Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC ±5%, -40 =< $T_{junction}$ =< 105×C, and worst case process.

Description	min	typ	max	Units	Comments
Output Signal to Distortion ratio Two tone[7] DS Multi-tone[8] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz US Multi-tone[9] 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 75 78 76 78 78	 81 84 82 84 84		dB	For all TxPGA gains. Measured differentially at TXOP/N
Output Referred Noise Voltage [10] [11] [12] TxPGA Gain = 0dB 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz TxPGA Gain = min 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz		 80 80 30 30	 100 100 40 40	$\frac{nV}{\sqrt{Hz}}$	measured differentially at TXOP/N
Output Signal to Noise and Distortion Ratio (DS) [13] [14] TxPGA Gain = 0dB 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz TxPGA Gain = min 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 74 73 53 53	 80 79 59 59		dB	measured differentially at TXOP/N
Output Signal to Noise and Distortion Ratio (US) [15] [13] TxPGA Gain = 0dB 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz TxPGA Gain = min 30kHz =< f =< 120kHz 155kHz =< f =< 540kHz	 76 76 55 55	 82 82 61 61		dB	measured differentially at TXOP/N
Out of Band Noise			72	$\frac{nV}{\sqrt{Hz}}$	band from 550KHz - 2.2 MHz (f_S/2)
Maximum Output Signal @TXOP/N			2.4	Vp	differential output
Load Resistance @ pin **TXOP/N**	500			W	per output to 2.5V
Load Capacitance @ pin **TXOP/N**			10	pF	per output to 2.5V

Table 3. Transmit Path Specifications

Unless otherwise noted, typical specifications apply for VCC=5 Volts, temperature=27×C, nominal process and current. Maximum and minimum performance is with VCC ±5%, -40 =< $T_{junction}$ =< 105×C, and worst case process.

Description	min	typ	max	Units	Comments
Settling Time[16]			300	nsec	Time for PGA to settle to 3t accuracy after a change in the control word indicated by **ENB** going high.

<1>For the purposes of this specification, a gain of 1V/V (i.e. 0dB) is defined as the ratio of the full scale DAC input word to the output voltage at TXOP/TXON when the output from the Tx path is at 2.4Vp differential measured between TXOP and TXON.

<2>For G.lite the STLC1511 will support both CO and CPE applications. As such it needs to support rates from 30kHz to 120kHz (CPE Transmit band) and 155kHz to 540kHz (CO Transmit band). 275kHz is roughly in the middle of the required frequency range.

<3>Will be tested at Vcc=5.0V, 27^{o}C, and f=275kHz.

<4>Will be tested at Vcc=5.0V and f=275kHz.

<5>Will be tested at 27^{o}C and f=275kHz.

<6>Will be tested at Vcc=5.0V and 27^{o}C.

<7>Two tone distortion is measured with two sinewaves with each sinewave at an amplitude of 1/2 full scale. Tone one is at f1=400kHz and tone two is at f2=500kHz. The two tone distortion requirement is measured from the rms voltage of a single signal tone to the peak rms voltage of the distortion products.

<8>A multi-tone sine wave is used for the DS Multi-tone test. (The multi-tone signal will be 89 sinewaves equally spaced from 36*4.3125kHz to 125*4.3125kHz with a peak-to-rms ratio of 5.3V/V and an rms voltage equal to 1/5.3 of the peak full scale range of the PGA.) Multi-tone measures the difference between the rms voltage of a single tone at the output to the rms voltage of the peak distortion product at the output in the band of interest.

<9>A multi-tone sine wave is used for the US Multi-tone test. (The multi-tone signal will be 21 sinewaves equally spaced from 7*4.3125kHz to 28*4.3125kHz with a peak-to-rms ratio of 5.3V/V and an rms voltage equal to 1/5.3 of the peak full scale range of the PGA.) Multi-tone test measures the difference between the rms voltage of a single tone at the output to the rms voltage of the peak distortion product at the output in the band of interest.

<10>Noise voltage is specified as the noise spectral density (e_n) at the output. Conversion to power spectral density is as follows:

$$PSD = 10 \times \log\left(\frac{en^2}{100} \times 1000\right)$$

<11>The output referred noise voltage for the STLC1511 can be calculated as follows:

$$en = \sqrt{(40n\dot{V}/Hz)^2 + (10^{(G+5.3)/20} \times 50n\dot{V}/Hz)^2}$$

where G is the gain of the TxPGA expressed in dB.

<12>The output referred noise of the Tx path at the 0dB gain setting is mainly due to the output referred noise of the DAC amplified by 5.3dB to the output of the chip. The DAC noise itself is made up of roughly equal contributions between quantization noise and thermal noise. It is only the thermal noise portion which will significantly change between a typical and worst case device.

<13>The SNDR is the ratio of PSD of the signal to the PSD of the noise plus distortion. The input for this test is as described in *h* above scaled by the gain to produce a full scale output signal.

<14>The effective noise plus distortion floor can be calculated from the SNDR based on the PSD of the output signal

.

$$PSD = 10 \times \log\left(\frac{(2.4/(5.3 \times \sqrt{540kHz - 155kHz}))^2}{100} \times 1000\right) = -52.7dBm/Hz$$

So that for G=0, the effective noise plus distortion floor will be at -52.7dBm/Hz - 74dB = -126.7dBm/Hz and for G=max, the floor is at -52.7dBm/Hz -32dB (cutback) - 53dB = -137.7dBm/Hz

<15>The SNDR is the ratio of PSD of the signal to the PSD of the noise plus distortion. The input for this test is as described in *i* above scaled by the gain to produce a full scale output signal.

<16>1t settling time is roughly equivalent to the unity gain frequency of the PGA block.

3.4 Phase Lock Loop

The STLC1511 has been intended for use in either the Central Office application (CO) using an external clock of 35.328MHz, in the Central Office application using an external 2.56Mhz clock and on-ship PLL , or in a Customer Premise Equipment application (CPE).

In the CO application (External Clock Mode), the reference clock used for the converters and internally in the STLC1511 is provided by an external reference. In the CO application (Oscillator Mode), the STLC1511 provides the ability to drive a LC oscillator and generate the require clocks using an on-chip PLL. In the Customer Premise Equipment (CPE) application, the STLC1511 provides the crystal driver for use with a external crystal and feedback network. In the CPE application the tuning signal must be provided by the digital modem ASIC (STLC1510).

While the above descriptions highlight the intended applications, the STLC1511 also has the flexibility to provide a PLL function when used with a different reference frequency and external 35.328MHz crystal. Table 4 highlights the different PLL modes for the STLC1511.

Table 4. PLL Application Modes[1]

Description	FREF freq MHz	DIGREF freq MHz	PLL active?	LC Osc freq MHz	XTAL freq MHz	AFE Control 5 [b5:b0]
CO External Clock Mode[2]	35.328	35.328	No	N/A	N/A	000000
CO Oscillator Mode	2.56	17.664	Yes	88.32	N/A	001001
CPE Mode	N/A	35.328	No	N/A	35.328	000110
PLL Misc. 1	1.536	35.328	Yes	N/A	35.328	011110
PLL Misc. 2	2.048	35.328	Yes	N/A	35.328	101110
PLL Misc. 3	4.096	35.328	Yes	N/A	35.328	111110

<1>Presently only applications described in this table are supported.

<2>The clock jitter specification for an externally supplied DAC or ADC clock (on pins FREF when in CO External Clock mode) is the same as the jitter specification for the PLL.

3.4.1 Central Office (External Clock Mode)

In CO External Clock Mode the 35.328MHz reference clock on pin **FREF** is divided down and used in both the TX and RX converters. In this mode of operation, the PLL and oscillator driver are powered down.

External Clock Mode is selected by setting b5:b0 of register “AFE Control 4” to “000000”. See section 3.7 for more information.

3.4.2 Central Office (Oscillator Mode)

In Oscillator Mode the 2.56MHz reference clock on pin **FREF** is used as the reference clock for the STLC1511 PLL. This clock is used to lock the LC oscillator frequency to 88.32MHz which is further divided down to provide the sampling clocks to both the TX and RX converters and passed to the digital ASIC STLC1510 as its PLL reference on the pin **DIGREF**. *The clock supplied to the digital ASIC STLC1510 via* ***DIGREF*** *is running at a rate of 17.664MHz in this mode.*

details the CO PLL and oscillator performance when connected as shown in Figure 3, "CO Frequency vs. Tuning Voltage".

CO Oscillator mode is selected by setting b5:b0 in register “AFE Control 5” to “001001”. See section "Digital Interface And Memory Map" on page 20 for more information.

Table 5. CO PLL Specifications

Unless otherwise noted, typical specifications apply for VCC=5.0 V, temperature=25×C, nominal process and bias current. Maximum and minimum performance is with VCC ±5%, -40 =< $T_{junction}$ =< 105×C, and worst case process.

Description	min	typ	max	Units	Comments
Reference Clock Frequency		2.56		MHz	on pin FREF
Output Clock Frequency		17.644		MHz	at pin DIGREF
LC Frequency Tuning Range[e]	84	88.32	94	MHz	Assumes 2% capacitors.
Oscillator Signal Level	200		500	mVp	
Power Up Time		200		msec	
VCO Gain Vco gain (LC)	5.0	5.4	6	MHz/V	see CAPTION FIGURE 4 on page 14
Charge Pump Current	180	200	220	mA	
Input Impedance @OSCPB and OSCNB[1]					see TITLE 3 3.4.3 on page 16
Output Impedance @OSCPE and OSCNE[a]					see TITLE 3 3.4.3 on page 16
CO Phase Noise at f_s[2] 5KHz offset 10kHz offset 20kHz offset 30kHz offset 100kHz offset 200kHz offset 300kHz offset 400kHz offset 500kHz offset			 89 91 97 101 120 129 133 137 141	dBc/Hz	Phase noise at **DIGREF** output (i.e. 17.664MHz) in CO Oscillator mode.

<1>Input and output impedance measured with 50kW from OSCPB to Vcc and OSCNB to Vcc

<2>For inband noise, phase noise at multiples of 4.3125kHz will rms add to degrade the inband SNR. Similarly, for out of band signals, phase noise will rms add depending on the offset between the carrier and the band of interest to reduce the SNR. For example, noise contributions on carriers from 34 to 127 will rms add to degrade the SNR on the edge of the US band (carrier 26).

Figure 3. CO Frequency vs. Tuning Voltage

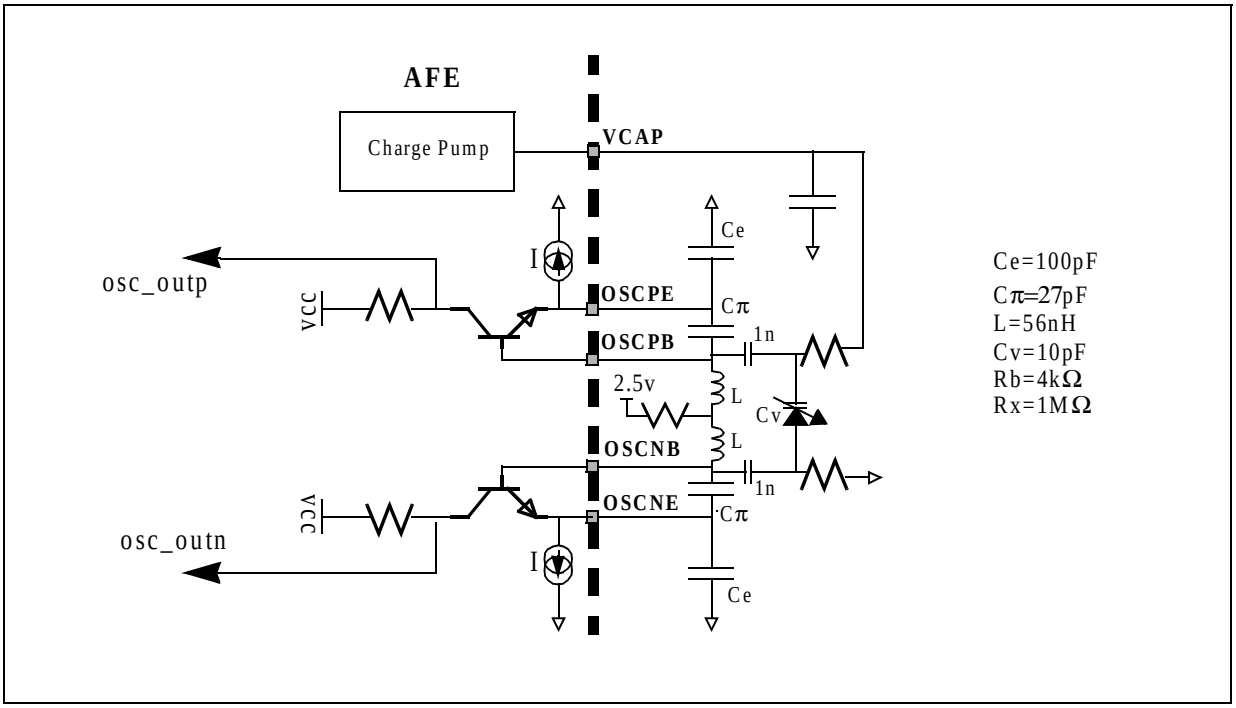


Figure 4. CO Frequency vs. Tuning Voltage

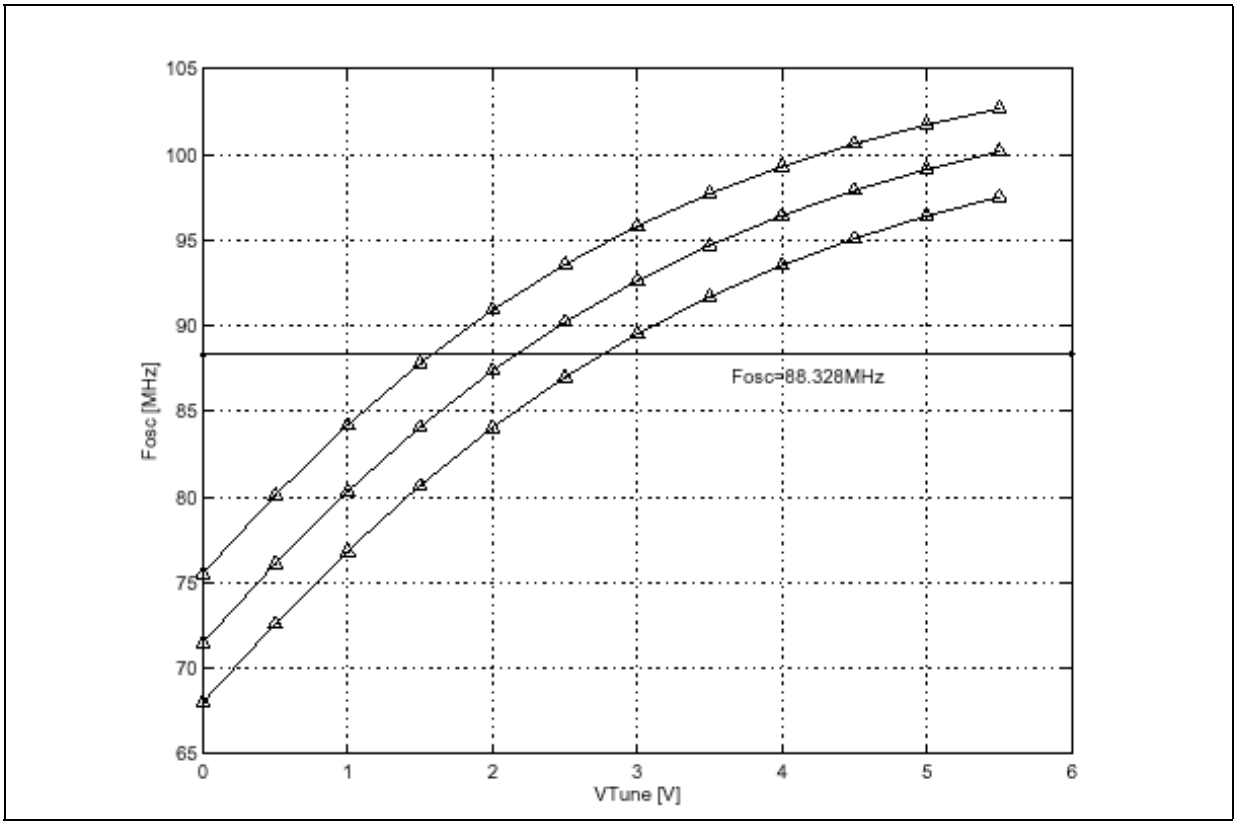


Figure 5. Oscillator Input Impedence

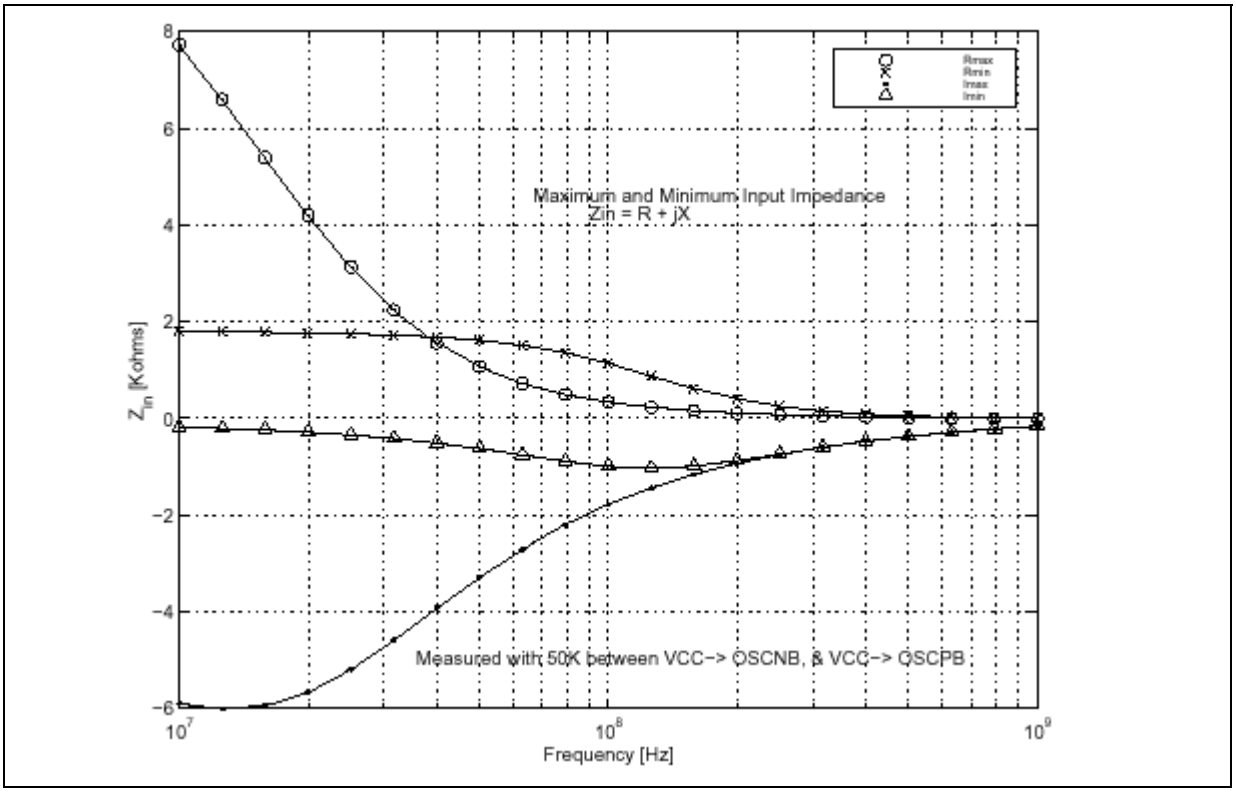
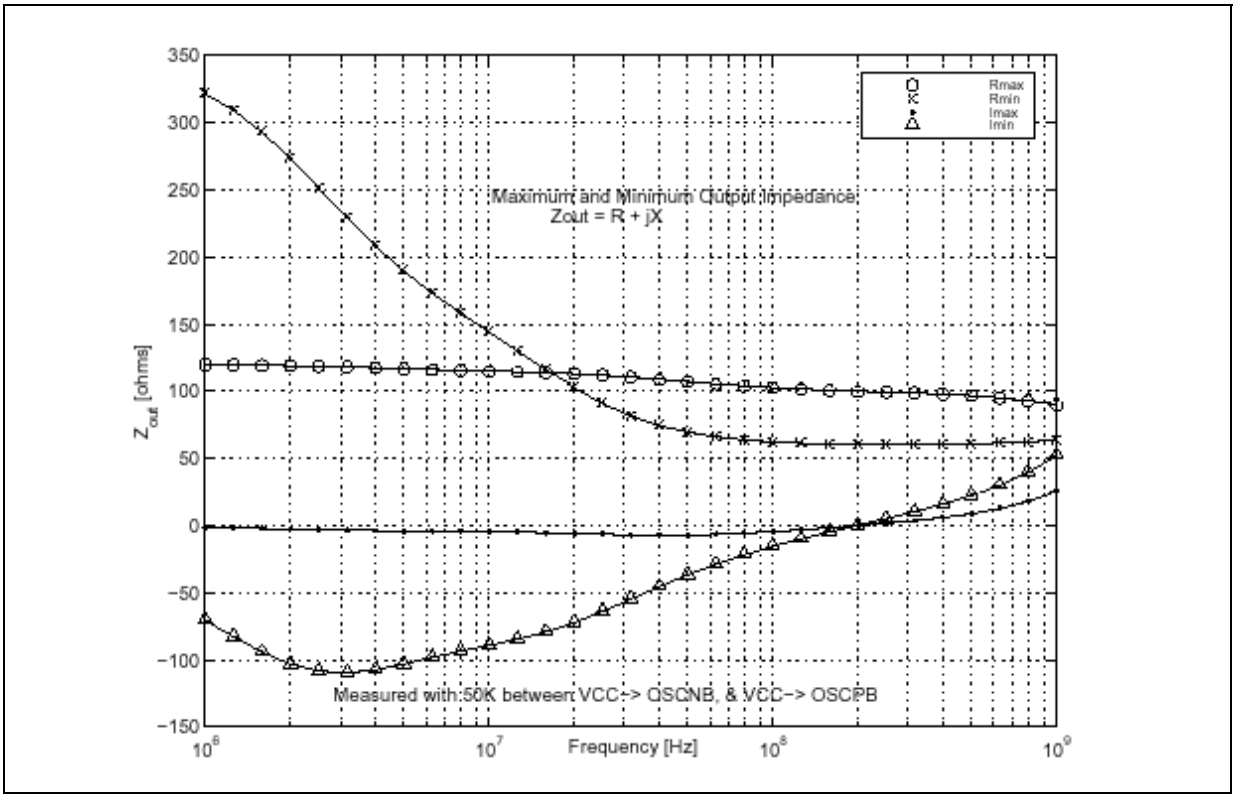


Figure 6. Oscillator Output Impedence



3.4.3 Customer Premise Equipment

In CPE mode, the STLC1511 provides the amplifier required to power the off-chip crystal oscillator. The crystal oscillator runs at a frequency of 35.328 MHz (series resonant) which is further divided down to provide the sampling clocks to both the TX and RX converters and passed to the STLC1510 as its PLL reference on the pin **DIGREF**. Note that in CPE mode, neither the PLL or the pin **FREF** is used (**FREF** should be connected to either Vdd or Vss) and that the tuing for the external oscillator is generated on the STLC1510.

The following table details the CPE oscillator performance when connected as shown in Figure 3. on page 14. CPE mode is selected by setting b5:b0 in register “AFE Control 5” to “001110”. See section "Digital Interface And Memory Map" on page 20 for more information.

Note the reference design provided is based on a Reeves Hoffman fundamental Mode AT cut crystal at 35.328MHz.(Crystal accuracy@+/-50ppm (+/-15ppm calibration tolerance, +/-15ppm 10 year aging, +/-20 ppm temperature variation, Rs@15Ω max, Cm@15fF max, and Co@3.5pF typ (assumes a HC49/43 package).)

Table 6. CPE PLL Specifications

Unless otherwise noted, typical specifications apply for VCC=5.0 V, temperature = 25×C, nominal process and bias current. Maximum and minimum performance is with VCC ± 5%, -40 =< $T_{junction}$ =< 105×C, and worst case process.					
Description	**min**	**typ**	**max**	**Units**	**Comments**
Output Clock Frequency		35.328		MHz	at pin DIGREF
Crystal Accuracy[1] [2]	-50		+50	ppm	crystal accuracy for CPE.
Crystal Frequency Tuning Range[2] [3]	-125		+125	ppm	Occurs at CPE. Assumes CO is free running
Oscillator Signal Level	200		500	mVp	
Power Up Time		5	10	msec	
VCO Gain Vcxo gain (crystal)	1.4	1.6	1.7	KHz/V	see TITLE 2 3.5 on page 18
Input Impedance @OSCPB and OSCNB[4]					see TITLE 3 3.4.3 on page 16
Output Impedance @OSCPE and OSCNE[4]					see TITLE 3 3.4.3 on page 16
CPE Phase Noise at f_s[5] 10Hz offset 20Hz offset 40Hz offset 60Hz offset 80Hz offset 100Hz offset 200Hz offset 400Hz offset 600Hz offset 800Hz offset 1000Hz offset			 -51.9 -57.9 -63.9 -67.5 -69.9 -71.9 -77.9 -83.9 -87.5 -89.9 -91.9	dBc/Hz	Phase noise at DIGREF output (i.e. 35.328MHz) in CPE mode.

<1>For the CPE side a crystal oscillator will be used.

<2>50ppm accuracy is divided as ±15ppm for manufacture, ± 15ppm for 10 year drift, and ± 20ppm for temperature variation.

<3>Worst case for tuning is when CO is not locked and CPE must retime from CO. Nominally the tuning range for the CO is ±50ppm, so that if the CO is free running, the CPE must tune over the CO inaccuracy and the CPE crystal inaccuracy as well.

<4>Input and output impedance measured with 50kW from OSCPB to Vcc and OSCNB to Vcc

<5>For inband noise, phase noise at multiples of 4.3125kHz will rms add to degrade the inband SNR. Similarly, for out of band signals, phase noise will rms add depending on the offset between the carrier and the band of interest to reduce the SNR. For example, noise contributions on carriers from 34 to 127 will rms add to degrade the SNR on the edge of the US band (carrier 26).

Figure 7. Typical CPE Oscillator Configuration

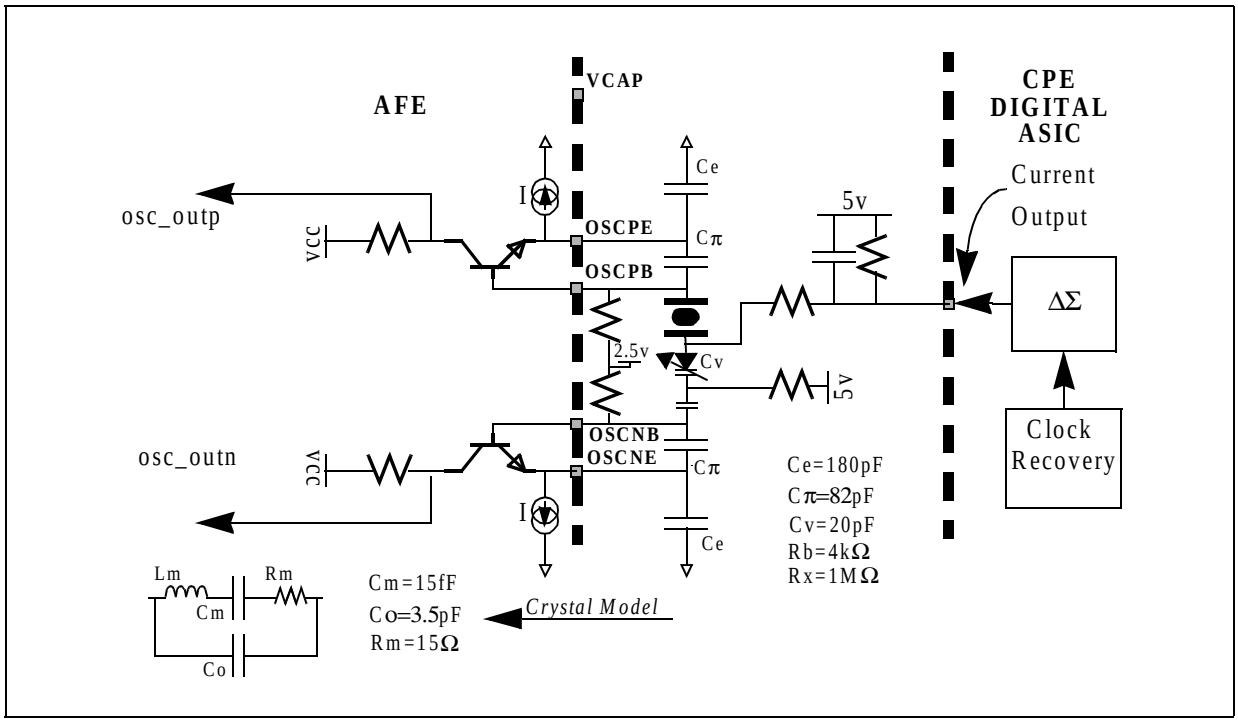
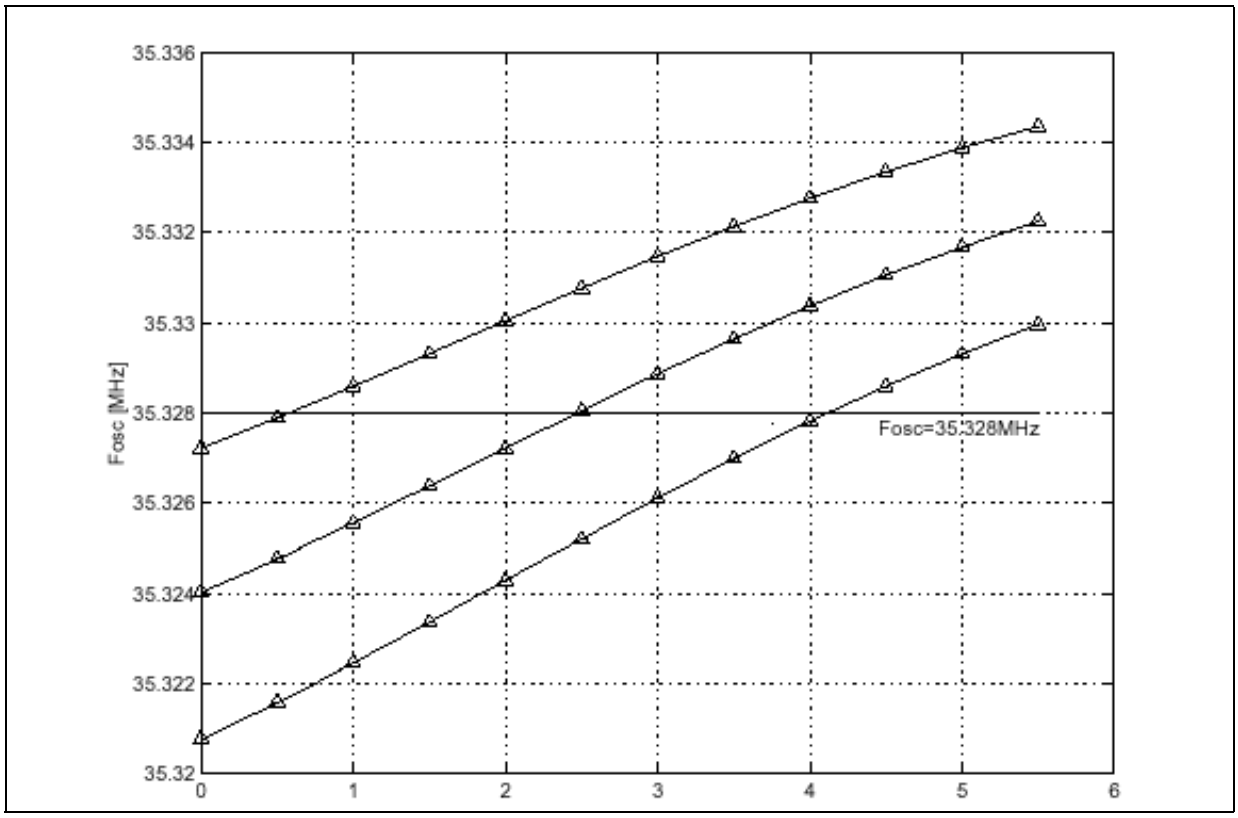


Figure 8. CPE Frequency vs. Tuning Voltage



3.5 Reference Voltages

Table 7. Reference Voltages/Currents

Unless otherwise noted, typical specifications apply for VCC = 5.0 V, temperature=25×C, nominal process and bias current. Maximum and minimum performance is with VCC ± 5%, -40 =<$T_{junction}$ =< 105×C, and worst case process and bias current.					
Description	**min**	**typ**	**max**	**Units**	**Comments**
V3P75V Output voltage	3.6375	3.750	3.8625	Volts	measured at V3P75V
Output Referred Noise Voltage at ANG			10	$\frac{nV}{\sqrt{Hz}}$	measured at V3P75V
TXDADC1 Output voltage	2.425	2.5V	2.575	Volts	measured at TXDADC1
TXDADC1 Output current			50	mA	measured at TXDADC1
External resistor at IREF	49	50	51	kW	assume 2%
External capacitor at V3P75V		0.22		mF	

3.6 Serial Interface

The serial interface on the AFE provides for transmission of transmit and receive data between the STLC1511 and digital modem ASIC. This is accomplished with a two bit wide data stream in each direction plus the appropriate clocks. The data for the transmit path is input to the AFE on the **TXSIN[1:0]** pins and the data for the receive path is output on the **RXSOUT[1:0]** pins.

The serial interface also consists of a 35.328MHz clock (**CK35M**) which is generated in the STLC1510 and is used to retime the Tx data sent to the STLC1511. It is also used in the STLC1511 to retime the Rx data before it is sent to the digital chip.

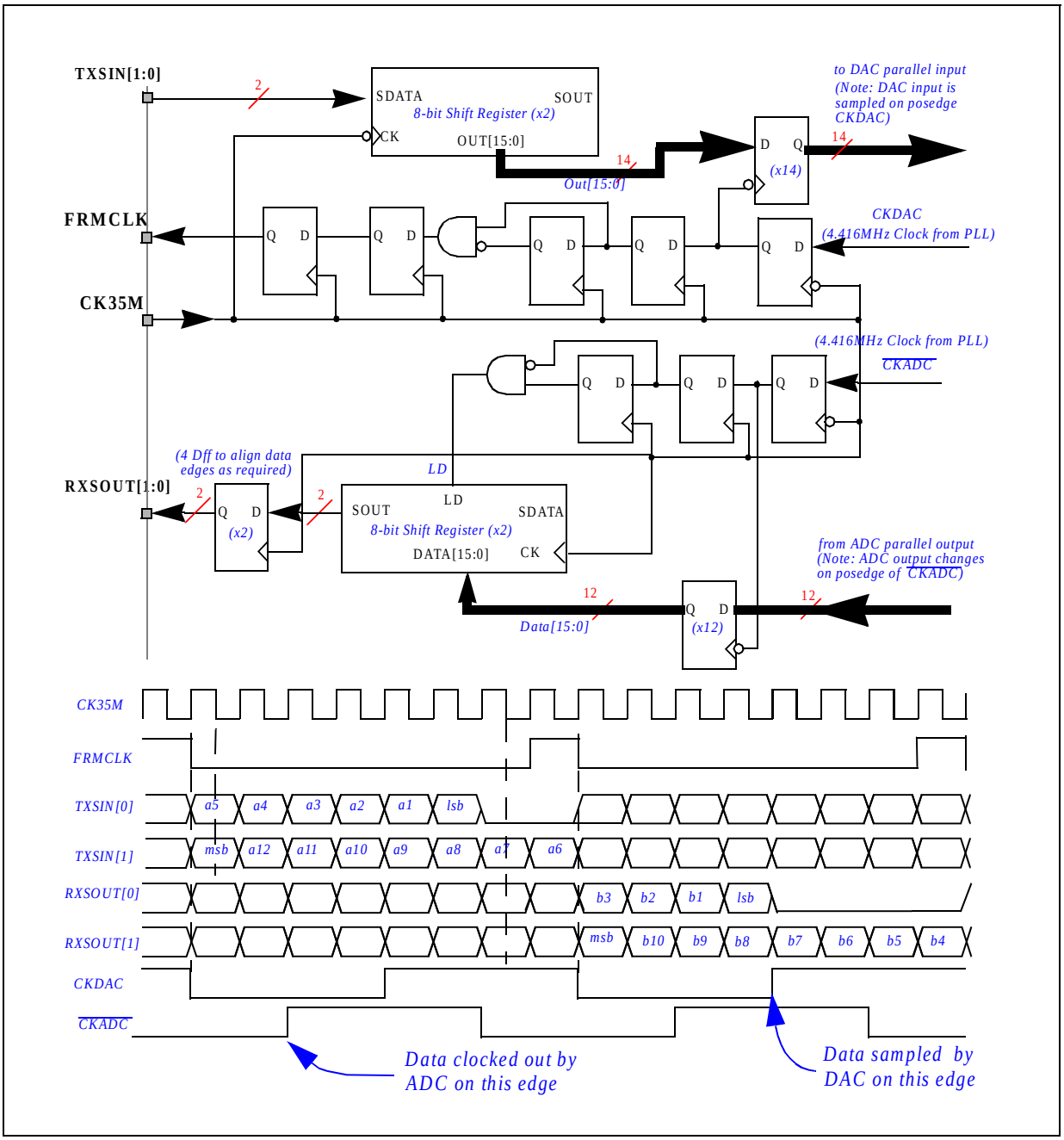
A 4.416MHz pulse is also output from the STLC1511. This pulse on pin **FRMCLK** is used to indicate the start of the output and input data words. The alignment of the data to the **FRMCLK** signal is shown below.

A diagram of this interface is show in Figure 11.

Note the MSB of each of the 8-bit registers is transferred first (MSB = b15/ b7.)

Note that the data word used by the converters is in 2's complement notation.

Figure 9. Serial Interface Block Diagram

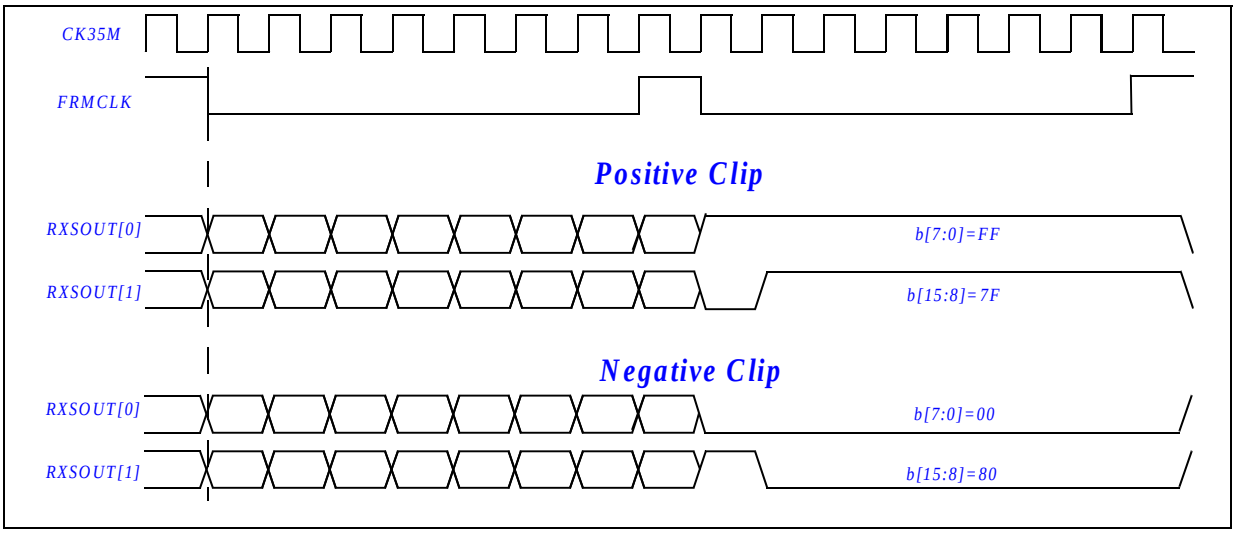


3.6.1 ADC Clip Indicator

Normally, the receive signal level is set such that the input to the STLC1511 plus the RxPGA gain will not saturate the input to the ADC converter (for maximum ADC input levels).

If the input signal is too large however and causes the ADC to clip, the STLC1511 will report to the digital chip that a clip has occurred. This is accomplished by forcing the output data stream supplied to the digital chip to either “7FFF” hex for an out of range positive input or to “8000” hex for an out of range negative input. This is highlighted in Figure 10.

Figure 10. Clip Indicator Output.



Bit 0 in the “AFE Status” register is also set to high when a clip occurs. This bit can be disabled via the control interface, see Table 8 on page 21 for more details. This bit is cleared on read. For more information see "Digital Interface And Memory Map" on page 20.

3.6.2 Tx Loop Back

When bit “b1” of register “011” (AFE Control 4) is asserted the data received on the TXSIN[1:0] pins is converted to parallel and then sent directly to both the DAC and the RX parallel data input replacing the usual data from the ADC.

This allows a “loop back” to the input TX data from TXSIN[1:0] to the RXSOUT[1:0] to help the testability of the serial interface.

3.7 Digital Interface And Memory Map

All parametric specifications in Table 2 on page 6 and Table 3 on page 9 are guaranteed assuming that the Digital Interface is inactive.

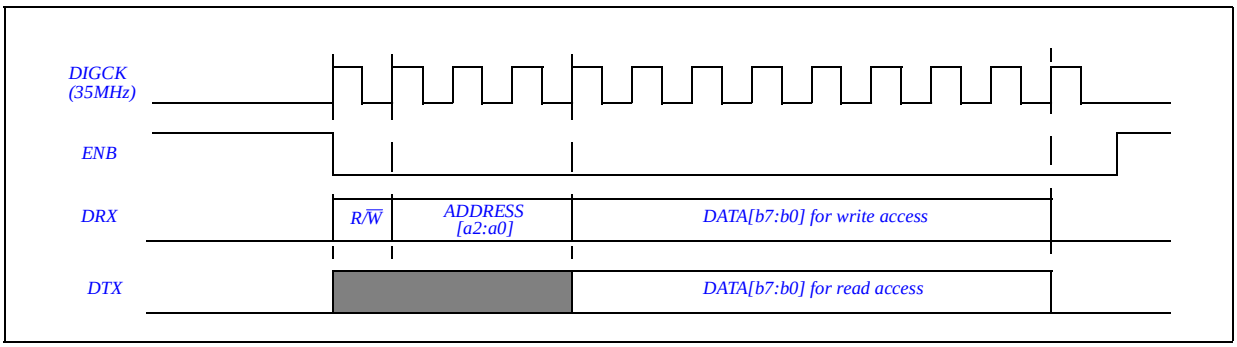
All parametric specifications in Table 2 and Table 3 are guaranteed assuming that the Digital Interface is inactive. The digital interface operates at a rate of 35.328 MHz. The companion DSP chip, STLC1510, sources the 35.328 MHz clock used by the AFE. To minimize the impact of digital noise on the STLC1511, this supplied clock is gated, and is only enabled during data transfers and during reset. **The clock does not need to be present in order to reset the chip.**

The processor interface consists of four pins: 1) the 35.328 MHz gated clock (DIGCLK); 2) a data in port for data transfers (DRX); a data out pin for data transfer (DTX); and 4) a chip select pin (ENB).

There are a total of 12 bits which are serially transmitted between the STLC1510 and AFE during data transfers. The gated clock lasts for a duration of 12 clock cycles. This 12 cycle interaction consists of a R/W bit, a 3 bit address, and a 8 bit data word.

The format for this serial transaction is given below in Figure 11.

Figure 11. Digital Interface Timing Diagram



During a transaction, the first bit sent to the AFE determines the type of transaction, R/W="1" corresponds to a read transaction while R/W="0" corresponds to a write transaction. The next three bits, address[a2:a0], determine which of the 8 AFE registers will be accessed (Table 8). This is followed by the 8-bit data word.

In both Read and Write transactions, bit 0 (***LSB***) of the serially transferred 8-bit word is clocked from the data source first (the data source being the external DSP during Write transactions; the STLC1511 during Read transactions).

The definition of these fields within the 8-bit word is outlined below in Table 8 and in the detailed register maps following.

When the voltage on the **RESETN** pin is low, the bits in the control register will be reset as per defined in the detailed register maps.

For a write operation, the data on the **DRX** pin is latched into the STLC1511 on the negative edge of the **DIGCLK** signal. The data should change state on the positive edge of the clock.

For a read operation, the data on the **DTX** pin is output on the positive edge of the clock on pin **DIGCLK**.

Table 8. AFE Register Map Summary

Addr [a2:a0]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Type
000	STLC1511 Control 1 (Rx PGA Gain)	Rx PGA Gain								RW
001	STLC1511 Control 2 (Tx PGA Gain)	not used			Tx PGA Gain					RW
010	STLC1511 Control 3 (Power Down Reg)	not used				Rx Opamp Power Down	not used	Rx Power Down	Tx Power Down	RW
011	STLC1511 Control 4 (Misc. Control)	not used			DIV Output (Test mode)		PLL PFD input sel	Tx Loop back	Clip Indicator enable	RW
100	AFE Control 5 (PLL Control)	not used	DIG-REF Enable	FREF Mode		PLL Mode	Osc Mode[1]	Clock Source Control		R/W
101	not used	not used								
110	not used	not used								
111	AFE Status	not used							Clip Status	R

<1>Presently there is no difference in the oscillator driver between Oscillator Mode and CPE modes so this bit is unused. However, it may be required in the future and should be programmed correctly in case needed.

Table 9. Detailed Register Map: AFE Control Byte 1

Title:	AFE Control 1 (Rx PGA Gain)			
Label:	Rx Gain		Access Type:	R/W
Address:	000		Bits Used:	8
Description:	Rx PGA Gain Setting			
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
RX Gain	b5-b0	0ŠDŠ40 DŠ40	Gain=D*0.5 dB Gain=20 dB	000000
RX Gain MSB	b7-b6	00 01 10 11	Gain=0 dB Gain=20 dB Gain=6 dB Gain=26 dB	0

Table 10. Detailed Register Map: AFE Control Byte 2

Title:	AFE Control 2 (Tx PGA Gain)			
Label:	Tx Gain		Access Type:	R/W
Address:	001		Bits Used:	5
Description:	Tx PGA Gain Setting			
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
TX Gain	b4-b0	0ŠDŠ16 DŠ16	Gain= -D*2 dB Gain=-32 dB	00000
not used	b7-b5			000

Table 11. Detailed Register Map: AFE Control 3

Title:	AFE Control 3 (Power Down Reg)			
Label:	Power Down		Access Type:	R/W
Address:	010		Bits Used:	3
Description:	Power Down Register			
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
Tx Power Down[1]	b0	0 1	Power up transmit path Power down transmit path	1
Rx Power Down[2]	b1	0 1	Power up receive path Power down receive path	1
not used	b2			0

Table 11. Detailed Register Map: AFE Control 3

Title:	AFE Control 3 (Power Down Reg)		
Label:	Power Down	Access Type:	R/W
Address:	010	Bits Used:	3
Description:	Power Down Register		

Bit Label	Bit(s)	Value	Bit Description	Reset
Rx Opamp Power Down	b3	0 1	Power up RxPGA Power down RxPGA	1
not used	b7-b4			0

<1>During power down the Tx serial interface is also disabled and TXSCLK is tristated.

<2>During power down the Rx serial interface is also disabled and RXSCLK and RXSOUT[1:0] are tristated

Table 12. Detailed Register Map: AFE Control 4

Title:	AFE Control 4 (Misc. Control)		
Label:	Misc Control	Access Type:	R/W
Address:	011	Bits Used:	5
Description:	Mode Control/Misc.		

Bit Label	Bit(s)	Value	Bit Description	Reset
Clip Indicator Enable	b0	0 1	Clip indicator disabled Clip indicator enabled	1
Tx Loop back	b1	0 1	Normal operation Test mode. Tx data sent to serial I/F is muxed to Rx input and trasmitted via the serial I/F	0
PLL Phase/Freq Input Select (Test Mode)	b2	0 1	Source of PLL phase-frequency detector feedback input. Output of feedback dividers. Signal on FREF is sent directly to PFD (ref input) and signal on **pin CK35M** is sent directly to PFD (vco input).	0
DIV Output (Test Mode only)	b3-b4	00 01 10 11	normal operation Output of DIV69 counter is output to DIGREF pin Output of DIV2/3/4/8 counter is output to DIGREF pin Output of DIV5 counter is output to DIGREF pin	0
not used	b7-b5			000

Table 13. Detailed Register Map: AFE Control 5

Title:	AFE Control 5 (PLL Control)		
Label:	PLL Control	Access Type:	R/W
Address:	100	Bits Used:	7
Description:	PLL Control Register		

Bit Label	Bit(s)	Value	Bit Description	Reset
Clock Source Control	b0-b1	00 01 10 11	(CO External Clock Mode.) Output of clock selection MUX is from **FREF** pin. This state also powers down the PLL and oscillator driver. (CO Oscillator Mode.) Output of clock selection MUX is from output of divide by 5. (CPE Mode). Output of clock selection MUX is from output of oscillator driver. (Other CPE Mode). Output of clock selection MUX is from output of oscillator driver.	00
OSC Mode[1]	b2	0 1	(CO Oscillator mode.) AFE is configured to drive external 88.32MHz LC oscillator. (CPE mode.) AFE is configured to drive external 35.328MHz crystal oscillator.	1
PLL Mode	b3	0 1	PLL active (PFD,CP active) PLL Inactive (PFD,CP powered down)	0
FREF Mode[2]	b5-b4	00 01 10 11	FREF frequency is 2.56MHz FREF frequency is 1.536MHz FREF frequency is 2.048MHz FREF frequency is 4.096MHz	00
DIGREF Enable	b6	0 1	**DIGREF** Output pin tristated **DIGREF** Output pin active	1
reserved	b7			0

<1>Presently there is no difference in the oscillator driver between CO Oscillator and CPE modes so this bit is unused. However, it may be required in the future and should be programmed correctly in case needed.

<2>For FREF at 2.56MHz (b5:b4 = “00”), the compare frequency for the PLL is at 1.28MHz. For all other FREF modes the compare frequency is at 512kHz.

Table 14. Detailed Register Map: *not used*

Title:	AFE Control 6 (Misc Control 2)			
Label:	Misc Control 2		Access Type:	R/W
Address:	101		Bits Used:	0
Description:				
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
not used	b7-b0			00000000

Table 15. Detailed Register Map: *not used*

Title:	not used			
Label:			Access Type:	R/W
Address:	110		Bits Used:	0
Description:				
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
not used	b7-b0			00000000

Table 16. Detailed Register Map: AFE Status

Title:	AFE Status			
Label:	AFE Status		Access Type:	R
Address:	111		Bits Used:	2
Description:	AFE Read only Status			
Bit Label	**Bit(s)**	**Value**	**Bit Description**	**Reset**
Clip Status?	b0	0 1	A/D clip not detected A/D clip detected	0
not used	b7-b2			000000

3.8 TIMING

Table 17. describes the timing relationships between important signals.

Table 17. Timing

Symbol	Parameter	Spec Min	Typ [1]	Spec Max	Units
t_{SENB}	ENB falling to DIGCLK rising	1	5		ns
t_{HENB}	ENB rising to DIGCLK falling	1	5		ns
t_{SDRX}	Data in valid to DIGCLK falling	2	5		ns
t_{HDRX}	DIGCLK falling to Data in hold	2	5		ns
t_{DDTX}	DIGCLK rising to Data out valid		5	10	ns
t_{SCK35}	TXSIN[1:0] valid to CK35M falling	2	5		ns
t_{HCK35}	CK35M falling to TXSIN[1:0] hold	2	5		ns
t_{DRX}	CK35M rising to RXSOUT[1:0] valid		5	10	ns
t_{DFC}	CK35M rising to FRMCLK valid		5	10	ns
$t_{DDRCK35}$	DIGREF rising to CK35M rising	10	12	20	ns
$t_{RDIGREF}$	DIGREF rise time (20% to 80%)	1	2	3	ns
$t_{FDIGREF}$	DIGREF fall time (80% to 20%)	1	2	3	ns

<1>Load on all output pads assumed to be < 25pF.This gives a delay through the TLCHT pad of approximately 5ns.

3.9 POWER UP RESET

When the voltage on the **RESETN** pin is low the bits in the control register will be reset as per the detailed register maps in “Digital Interface And Memory Map” on page 20.

In addition, digital output pins, **DTX**, **FRMCLK**, and **RXSOUT[1:0]** are high impedance. The other digital outputs are always as defined in Table 1 on page 2.

4.0 PACKAGE INFORMATION, SUPPLY RATINGS, AND OPERATING ENVIRONMENT

4.1 The thermal impedance

The thermal impedance of the package is about 64 °C/W for the following conditions°

Table 18. Board Assumptions:

PC Board	6 layer, 1oz copper
Ambient Temperature	85^0C
Air Flow	natural convection
Power Dissipation	300mW

Table 19. Board Assumptions:

PC Board	6 layer, 1oz copper
Ambient Temperature	85^0C
Air Flow	natural convection
Power Dissipation	300mW

COMMENT ON RELIABILITY: *The maximum continuous junction temperature for this part while meeting 20 year reliability is 125°C.*

4.2 Environmental Conditions

Table 20. Environment conditions

T_a Long-Term (Continuous)	-40 to +80 ^{0}C
T_a Short-Term[1]	-40 to +85 ^{0}C

<1>Short-term is defined as no greater than 96 consecutive hours and 15 days per year.

4.3 Power Supply Input Limits

Table 21. defines the maximum and minimum power supply requirements to meet specifications as outlined in section 3.2 and 3.3.

Table 21. Power Supply Limits

Parameter	Limits			Unit	Conditions
	min	typ	max[1]		
Positive Supply Voltage	4.75	5	5.25	Volts	

Table 21. Power Supply Limits

Parameter	Limits			Unit	Conditions
	min	typ	max[1]		
Tx Powered Up CO Oscillator mode CO External Clock mode CPE mode Tx Powered Down CO Oscillator mode CO External Clock mode CPE mode		 65 60 65 41 36 41	 71 66 71 45 39 45	mA	Includes 4mA for digital supplies and digital I/O
Tx Powered up CO Oscillator mode CO External Clock mode CPE mode Tx Powered Down CO Oscillator mode CO External Clock mode CPE mode		 325 300 325 200 175 200	 373 347 373 237 205 237	mW	Includes 20mW for digital supplies and digital I/O

<1>Maximum current assumes a 7% increase due to process/temperature/Vcc plus the variation in the external 50k resistor (assumed 2%) connected to IREF50u. For this table the total variation is assumed at 9%.

4.4 Power Supply Noise

Table 22. Power Supply Noise

Noise Band	Maximum 5V Supply Noise Spectral Density	Max 5V Supply Noise (Over noise band)
30kHz < f < 112kHz	1.4µVrms/rtHz @ 112kHz, rising 6dB per octave for decreasing frequency	1.0mVrms
146kHz < f < 547kHz	1.0µVrms/rtHz @ 146kHz, dropping 6dB per octave to 0.25µVrms/rtHz @ 547kHz	0.30mVrms

4.5 Absolute Maximum Ratings

The following table describes the maximum and minimum voltage ratings

Table 23. Maximum and minimum voltage ratings

pin	Maximum	Minimum
all VCC pins	6.5V	-0.5V
all other pins	VCC+0.4	-0.4

4.6 Pin DC Electrical Specification

Table 24. General Interface Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit
Iil	Low level input current	Vi=0V			1	µA
Iih	High level input current	Vi=Vcc			1	µA
Ioz	Tri-state output leakage[1]	Vo=0V or Vcc			1	µA

<1>The leakage currents are generally very small, < 1nA. The value given here, 1mA, is a maximum that can occur after an ESD stress.

BT4CR is a CMOS tristate 4mA output pad buffer with slew rate control.

Table 25. CMOS Output Pad (BT4CR) DC Electrical Characteristics[1], [2]

	Parameter	Conditions	Min	Typ	Max	Unit
Vol	Low level output voltage	Iol=4mA			0.4	V
Voh	High level output voltage	Ioh=4mA	0.9*Vdd5		Vdd5	V

<1>Characterized for VCC=3.0 to 3.6V. This pad must be characterized at VCC=5.0V+-5% and the table updated

<2>Assumes a 200mV voltage drop in both supply lines. This will not be the case in the STLC1511.

Table 26. TTL Input Pad (TLCHT) DC Electrical Characteristics[1], [2]

	Parameter	Conditions	Min	Typ	Max	Unit
Vil	Low level input voltage				0.8	V
Vih	High level input voltage		2.0			V
Vilhyst	Low level Threshold input falling		0.9		1.45	V
Vihyst	High level Threshold input rising		1.4		1.9	V

<1>Characterized for VCC=3.0 to 3.6V. This pad must be characterized at VCC=5.0V+-5% and the table updated

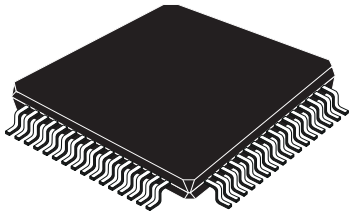
<2>Assumes a 200mV voltage drop in both supply lines. This will not be the case in the STLC1511.

4.7 Package

The STLC1511 will be packaged in a 64pin 10x10x1.4mm Thin Quad Flat Pack (TQFP) package.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP64