Data Sheet | May 5, 2008 | FN9034.3

Microprocessor CORE Voltage Regulator Multi-Phase Buck PWM Controller

The HIP6301V and HIP6302V control microprocessor CORE voltage regulation by driving up to four synchronous-rectified buck channels in parallel. Multiphase buck converter architecture uses interleaved timing to multiply ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and a smaller implementation area. The HIP6301V is a versatile 2- to 4-phase controller and the HIP6302V is a cost-saving dedicated 2-phase controller.

The HIP6301V and HIP6302V are exact pin compatible replacements for their predecessor parts, the HIP6301 and HIP6302. They are the first controllers to incorporate Dynamic VID™ technology to manage the output voltage and current during on-the-fly DAC changes. Using Dynamic VID, the HIP6301V and HIP6302V detect changes in the VID code, and gradually change the reference in 25mV increments until reaching the new value. By gradually changing the reference setting, in-rush current and the accompanying voltage swings remain negligibly small.

Intersil offers a wide range of MOSFET drivers to form highly integrated solutions for high-current, high slew-rate applications. The HIP6301V and HIP6302V regulate output voltage, balance load currents and provide protective functions for two to four synchronous-rectified buck converter channels. These parts feature an integrated high-bandwidth error amplifier for fast, precise regulation and a 5-bit DAC for the digital interface to program the 0.8% accuracy. A window comparator toggles PGOOD if the output voltage moves out of range, and acts to protect the load in case of over voltage.

Current sensing is accomplished by reading the voltage developed across the lower MOSFETs during their conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, load sharing, and overcurrent protection. This saves cost by taking advantage of the power device's parasitic on resistance.

Features

- Multi-Phase Power Conversion
- Precision CORE Voltage Regulation
  - ±0.8% System Accuracy Over-Temperature
- Microprocessor Voltage Identification Input
  - Dynamic-VID Technology
  - 5-bit VID Decoder
- Precision Channel-Current Balance
- Overcurrent Protection
- Lossless Current Sensing
- Programmable "Droop" Voltage
- Fast Transient Response
- Selection of 2-, 3-, or 4-Phase Operation
- High Ripple Frequency (100kHz to 6MHz)
- Pb-Free Available (RoHS Compliant)

Ordering Information

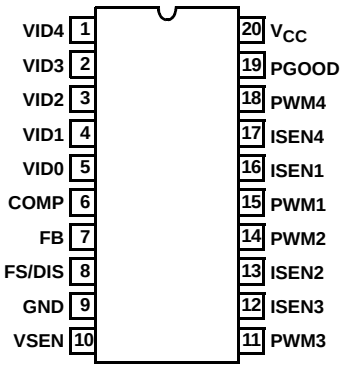
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP6301VCB*	HIP6301VCB	0 to +70	20 Ld SOIC	M20.3
HIP6301VCBZ* (Note)	HIP6301VCBZ	0 to +70	20 Ld SOIC (Pb-free)	M20.3
HIP6301VCBZA* (Note)	HIP6301VCBZ	0 to +70	20 Ld SOIC (Pb-free)	M20.3
HIP6302VCB*	HIP6302VCB	0 to +70	16 Ld SOIC	M16.15
HIP6302VCBZ* (Note)	HIP6302VCBZ	0 to +70	16 Ld SOIC (Pb-free)	M16.15

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

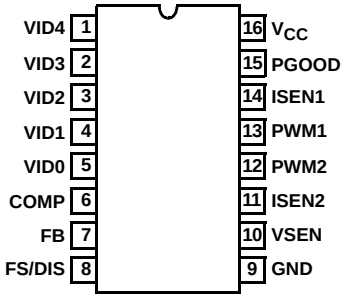
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

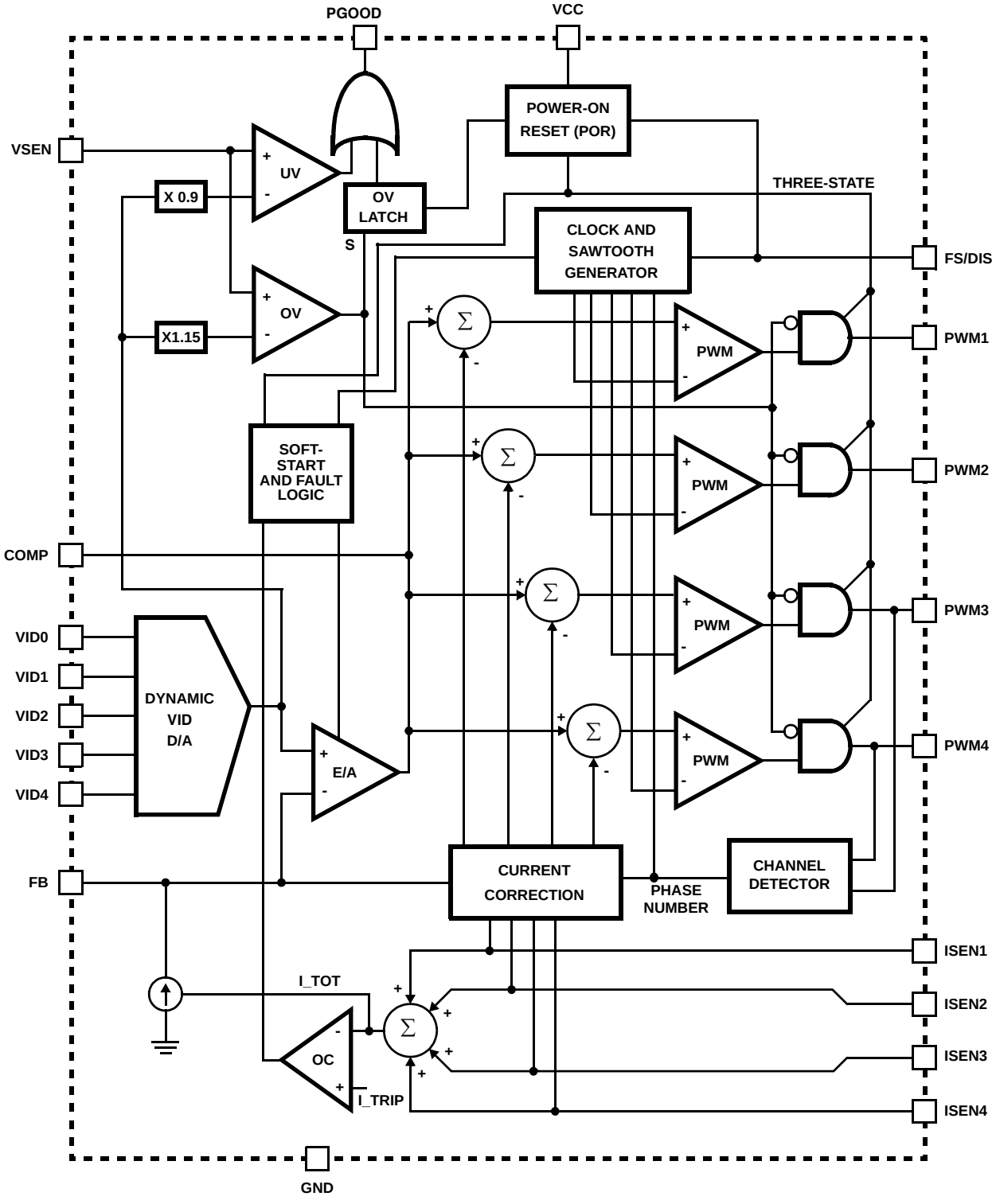
HIP6301V
(20 LD SOIC
TOP VIEW



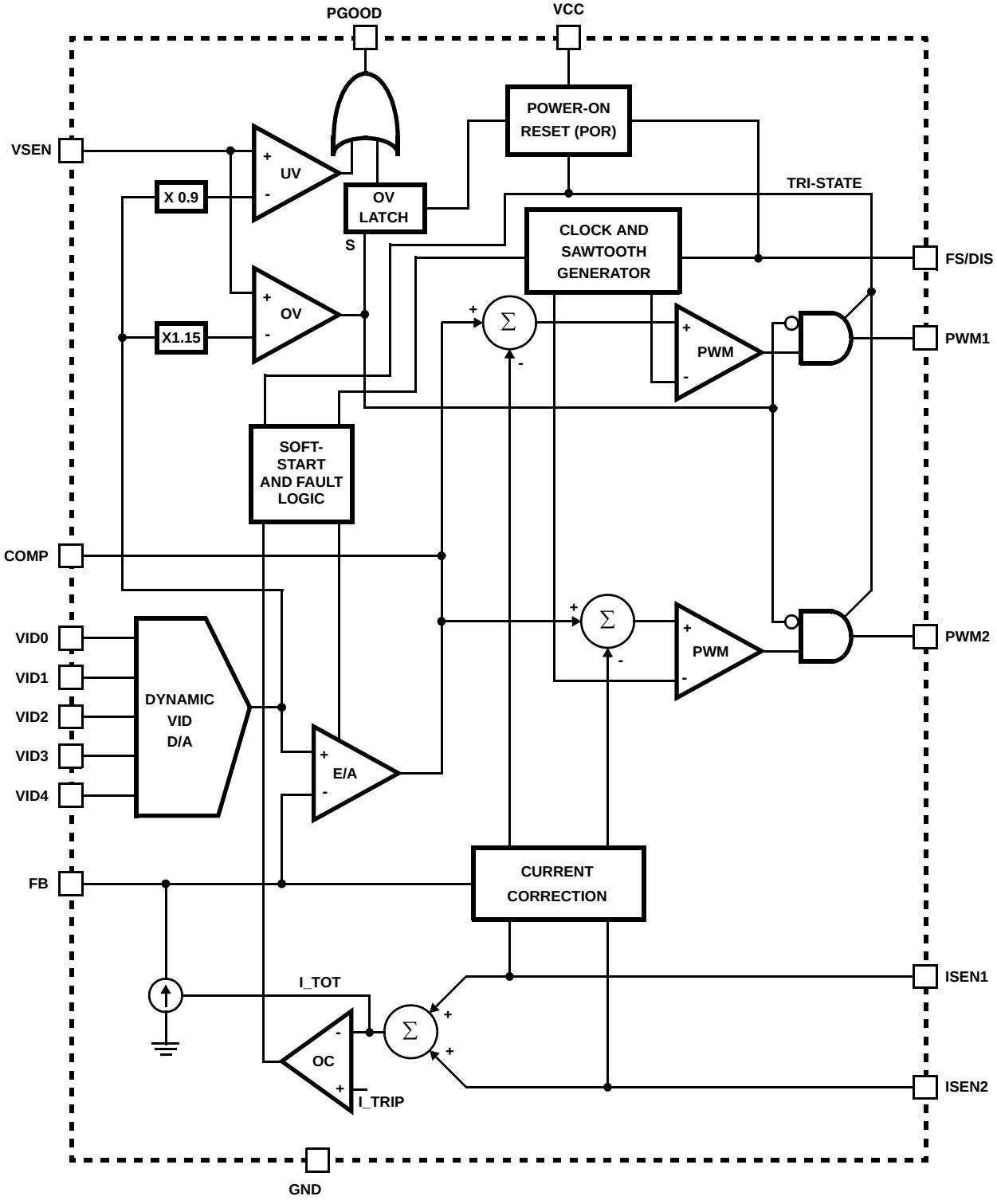
HIP6302V
(16 LD SOIC
TOP VIEW



HIP6301V Block Diagram

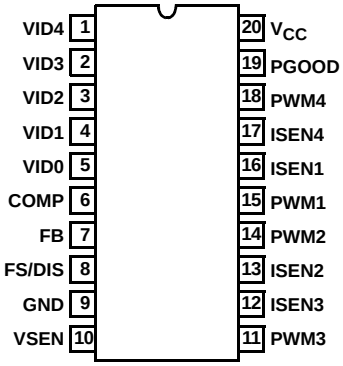


HIP6302V Block Diagram

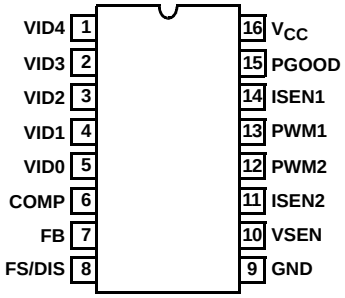


HIP6301V and HIP6302V Functional Pin Descriptions

HIP6301V
(20 LD SOIC
TOP VIEW



HIP6302V
(16 LD SOIC
TOP VIEW



VID4, VID3, VID2, VID1 and VID0 (Pins 1 thru 5 - Both Parts)

Voltage Identification inputs. The HIP6301V and HIP6302V decode the VID bits to establish the reference voltage (see Table 1). Each pin has an internal 20µA pull-up current source to 2.5V making the parts compatible with CMOS and TTL logic from 5V down to 2.5V. When a VID change is detected, the reference voltage slowly ramps up or down to the new value in 25mV steps. VID input levels above 2.9V may produce an reference-voltage offset inaccuracy.

COMP (Pin 6 - Both Parts)

Output of the internal error amplifier. Connect this pin to the external feedback and compensation network.

FB (Pin 7 - Both Parts)

Inverting input of the internal error amplifier.

FS/DIS (Pin 8 - Both Parts)

Channel frequency, F_{SW}, select and disable. A resistor from this pin to ground sets the switching frequency of the converter. Pulling this pin to ground disables the converter and three states the PWM outputs. See Figure 10.

GND (Pin 9 - Both Parts)

Bias and reference ground. All signals are referenced to this pin.

VSEN (Pin 10 - Both Parts)

Power-good monitor input. Connect to the microprocessor CORE voltage.

PWM1 (Pin 15 - HIP6301V, Pin 13 - HIP6302V), PWM2 (Pin 14 - HIP6301V, Pin 12 - HIP6302V), PWM3 (Pin 11 - HIP6301V only) and PWM4 (Pin 18 - HIP6301V only)

PWM outputs for each channel. Connect these pins to the PWM input of the external MOSFET driver. For HIP6301V systems using 3 channels, connect PWM4 high. For two channel systems, connect PWM3 and PWM4 high.

ISEN1 (Pin 16 - HIP6301V, Pin 14 - HIP6302V), ISEN2 (Pin 13 - HIP6301V, Pin 11 - HIP6302V), ISEN3 (Pin 12 - HIP6301V only) and ISEN4 (Pin 17 - HIP6301V only)

Current sense inputs from the individual converter channel's phase nodes. Unused sense lines MUST be left open.

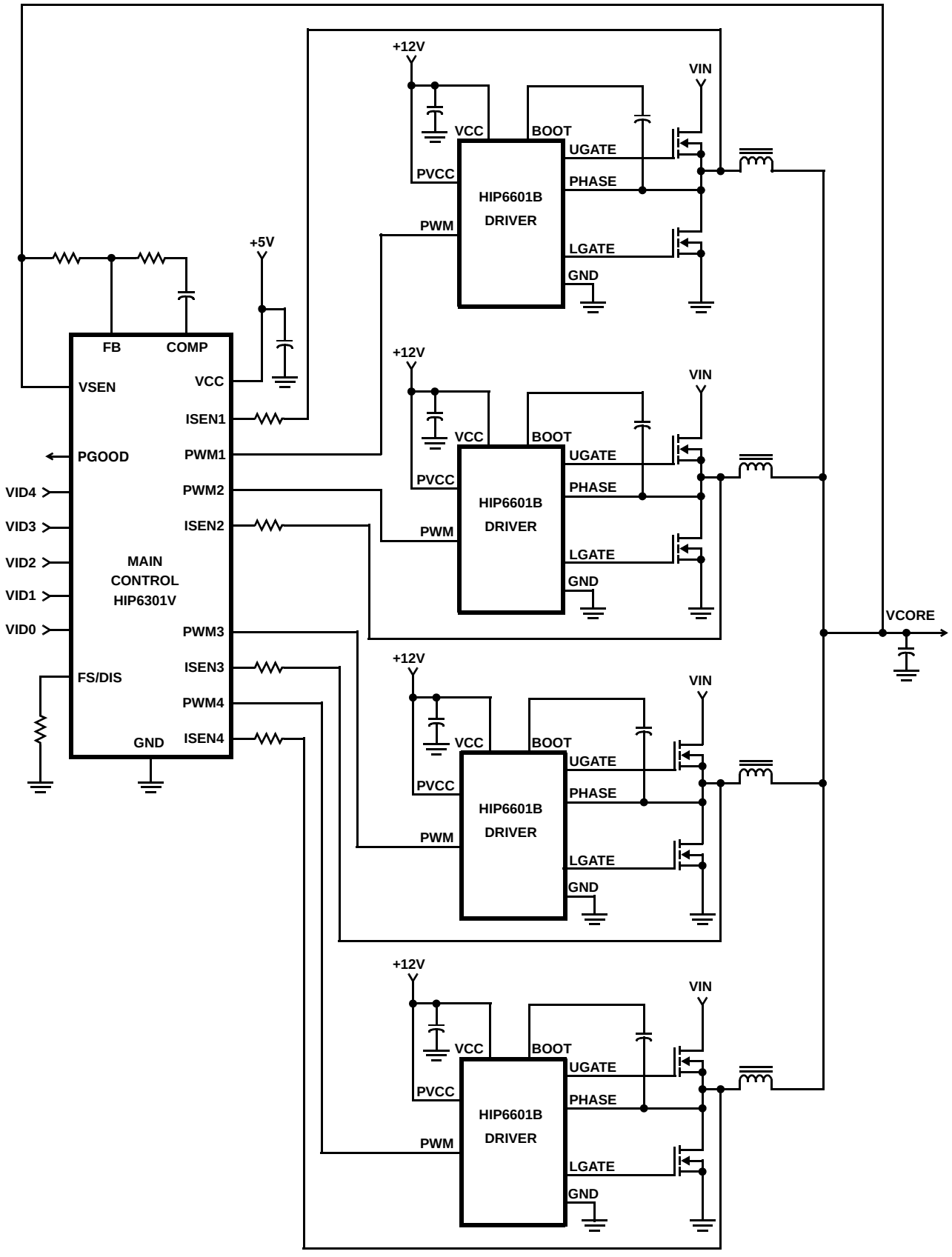
PGOOD (Pin 19 - HIP6301V, Pin 15 - HIP6302V)

Power-good. This pin is an open-drain logic signal that indicates when the microprocessor CORE voltage (VSEN pin) is within specified limits and soft-start has timed out.

V_{CC} (Pin 20 - HIP6301V, Pin 16 - HIP6302V)

Bias supply. Connect this pin to a 5V supply.

Typical Application - HIP6301V Controller with HIP6601B Gate Drivers



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} + 0.3V

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld SOIC Package	70
20 Ld SOIC Package	65

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty..

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. (See Tech Brief TB379 for details.)
2. VID input levels above 2.9V may produce an reference-voltage offset inaccuracy.
3. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_A = +0°C to +70°C, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
INPUT SUPPLY POWER					
Input Supply Current	R_T = 100kΩ	-	-	15	mA
POR (Power-On Reset) Threshold	V_{CC} Rising	4.25	4.38	4.5	V
	V_{CC} Falling	3.75	3.88	4.00	V
REFERENCE AND DAC					
System Accuracy	Percent system deviation from programmed VID Codes	-0.8	-	0.8	%
DAC (VID0 - VID3) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.8	V
DAC (VID0 - VID3) Input High Voltage	DAC Programming Input High Threshold Voltage	2.0	-	-	V
VID Pull-Up	VIDx = 0V or VIDx = 2.5V (Note 2); Not tested - for reference only	10	-	40	µA
CHANNEL GENERATOR					
Frequency, F_{SW}	R_T = 100kΩ, ±1%	224	280	336	kHz
Disable Voltage	$V_{FS/DIS}$ to disable controller; Not tested - for reference, only	-	-	1.0	V
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground	-	72	-	dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10k to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, R_L = 10k to ground	-	5.3	-	V/µs
Maximum Output Voltage	R_L = 10k to ground	3.6	-	-	V
Minimum Output Voltage	R_L = 10k to ground	-	-	0.5	V
I_{SEN}					
Full-Scale Current Level	Not tested - for reference, only	-	50	-	µA
Overcurrent Trip Level	Not tested - for reference, only	-	82.5	-	µA
POWER-GOOD MONITOR					
Undervoltage Threshold	VSEN Rising	-	0.92	-	V_{DAC}
Undervoltage Threshold	VSEN Falling	-	0.90	-	V_{DAC}
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
PROTECTION					
Overvoltage Threshold	VSEN Rising	1.12	1.15	1.20	V_{DAC}
Overvoltage Hysteresis	VSEN Falling; Not tested - for reference, only	-	2	-	%

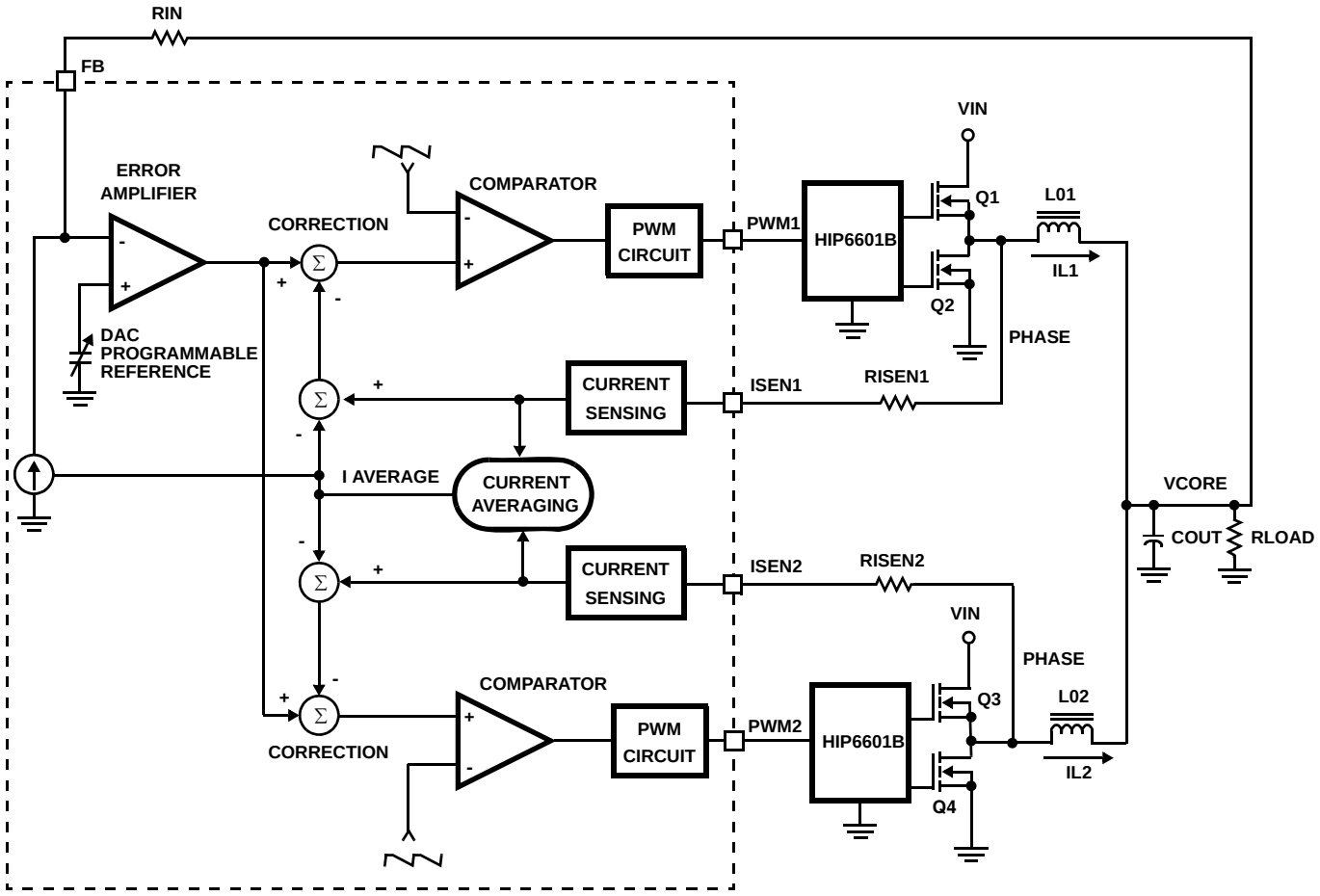


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE HIP6301V VOLTAGE AND CURRENT CONTROL LOOPS FOR 2-PHASE REGULATOR

Operation

Figure 1 shows a simplified diagram of the voltage regulation and current control loops. Both voltage and current feedback are used to precisely regulate voltage and tightly control the output currents, I_{L1} and I_{L2}, of the two power channels. The voltage loop comprises the error amplifier, comparators, gate drivers and output MOSFETs. The error amplifier is essentially connected as a voltage follower that has as an input, the programmable reference DAC and an output that is the CORE voltage.

Voltage Loop

Feedback from the CORE voltage is applied via resistor R_{IN} to the inverting input of the error amplifier. This signal can drive the error amplifier output either high or low, depending upon the CORE voltage. Low CORE voltage makes the amplifier output move towards a higher output voltage level. Amplifier output voltage is applied to the positive inputs of the comparators via the correction summing networks. Out-of-phase sawtooth signals are applied to the two Comparators inverting inputs. Increasing error amplifier voltage results in increased comparator output duty cycle. This increased duty cycle signal is passed through the PWM CIRCUIT with no phase reversal and on to the HIP6601B, again with no phase reversal for gate drive to the upper MOSFETs, Q_1 and Q_3. Increased duty cycle or ON-time for the MOSFET transistors results in increased output voltage to compensate for the low output voltage sensed.

Current Loop

The current control loop works in a similar fashion to the voltage control loop, but with current control information applied individually to each channel's comparator. The information used for this control is the voltage that is developed across $r_{DS(ON)}$ of the lower MOSFETs, Q_2 and Q_4, when they are conducting. A single resistor converts and scales the voltage across the MOSFETs to a current that is applied to the current sensing circuit within the controller. Output from these sensing circuits is applied to the current averaging circuit. Each PWM channel receives the difference signal from the summing circuit that compares the average sensed current to the individual channel current. When a power channel's current is greater than the average current, the signal applied via the summing correction circuit to the comparator, reduces the output pulse width of the comparator to compensate for the detected "above average" current in that channel.

Droop Compensation

In addition to control of each power channel's output current, the average channel current is also used to provide CORE voltage droop compensation. Average full channel current is defined as 50µA. By selecting an input resistor, R_{IN}, the amount of voltage droop required at full load current can be programmed. The average current driven into the FB pin results in a voltage increase across resistor R_{IN} that is in the direction to make the error amplifier "see" a higher voltage at the inverting input, resulting in the Error Amplifier adjusting the output voltage lower. The voltage developed across R_{IN} is equal to the "droop" voltage. "Current Sensing and Balancing" on page 13 for more details.

Applications and Convertor Start-Up

Each PWM power channel's current is regulated. This enables the PWM channels to accurately share the load current for enhanced reliability. The HIP6601, HIP6602 or HIP6603 MOSFET driver interfaces with the HIP6301V. For more information, see the datasheets for the individual Intersil MOSFET drivers.

The HIP6301V is capable of controlling up to 4 PWM power channels. Connecting unused PWM outputs to V_{CC} automatically sets the number of channels. The phase relationship between the channels is 360°/number of active PWM channels. For example, for three channel operation, the PWM outputs are separated by 120°. Figure 2 shows the PWM output signals for a four channel system.

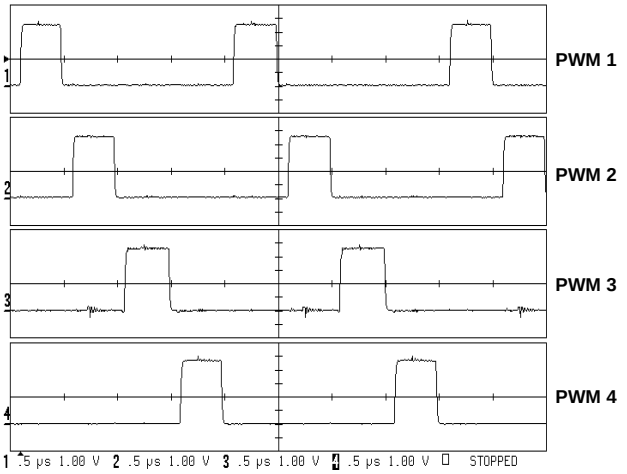


FIGURE 2. FOUR PHASE PWM OUTPUT AT 500kHz

Power supply ripple frequency is determined by the channel frequency, F_{SW}, multiplied by the number of active channels. For example, if the channel frequency is set to 250kHz and there are three phases, the ripple frequency is 750kHz.

The IC monitors and precisely regulates the CORE voltage of a microprocessor. After initial start-up, the controller also provides protection for the load and the power supply. The following section discusses these features.

Initialization

HIP6301V and HIP6302V circuits usually operate from an ATX power supply. Many functions are initiated by the rising supply voltage to the V_{CC} pin of the controller. Oscillator, Sawtooth Generator, Soft-start and other functions are initialized during this interval. These circuits are controlled by POR, Power-On Reset. During this interval, the PWM outputs are driven to a three-state condition that makes these outputs essentially open. This state results in no gate drive to the output MOSFETS.

Once the V_{CC} voltage reaches 4.375V (±125mV), a voltage level to insure proper internal function, the PWM outputs are enabled and the Soft-start sequence is initiated. If for any reason, the V_{CC} voltage drops below 3.875V (±125mV), the POR circuit shuts the converter down and again three states the PWM outputs.

Soft-start

After the POR function is completed with V_{CC} reaching 4.375V, the soft-start sequence is initiated. Soft-start by its slow rise in CORE voltage from zero, avoids an overcurrent condition by slowly charging the discharged output capacitors. This voltage rise is initiated by an internal DAC that slowly raises the reference voltage to the error amplifier input. The voltage rise is controlled by the oscillator frequency and the DAC within the controller, therefore, the output voltage is effectively regulated as it rises to the final programmed CORE voltage value.

For the first 32 PWM switching cycles, the DAC output remains inhibited and the PWM outputs remain three stated. From the 33rd cycle and for another, approximately 150 cycles the PWM output remains low, clamping the lower output MOSFETs to ground, (see Figure 3). The time variability is due to the error amplifier, sawtooth generator and comparators moving into their active regions. After this short interval, the PWM outputs are enabled and increment the PWM pulse width from zero duty cycle to operational pulse width, thus allowing the output voltage to slowly reach the CORE voltage. The CORE voltage will reach its programmed value before the 2048 cycles, but the PGOOD output will not be initiated until the 2048th PWM switching cycle.

The soft-start time or delay time, DT = $2048/F_{SW}$. For an oscillator frequency, F_{SW}, of 200kHz, the first 32 cycles or 160µs, the PWM outputs are held in a three state level as explained above. After this period and a short interval previously described, the PWM outputs are initiated and the voltage rises in 10.08ms, for a total delay time DT of 10.24ms.

Figure 3 shows the start-up sequence as initiated by a fast rising 5V supply, V_{CC}, applied to the controller. Note the short rise to the three state level in PWM 1 output during first 32 PWM cycles.

Figure 4 shows the waveforms when the regulator is operating at 200kHz. Note that the soft-start duration is a

function of the Channel Frequency, as explained previously. Also note the pulses on the COMP terminal. These pulses are the current correction signal feeding into the comparator input (see Figure 1).

Figure 5 shows the regulator operating from an ATX supply. In this figure, note the slight rise in PGOOD as the 5V supply rises.The PGOOD output stage is made up of NMOS and PMOS transistors. On the rising V_{CC}, the PMOS device becomes active slightly before the NMOS transistor pulls “down”, generating the slight rise in the PGOOD voltage.

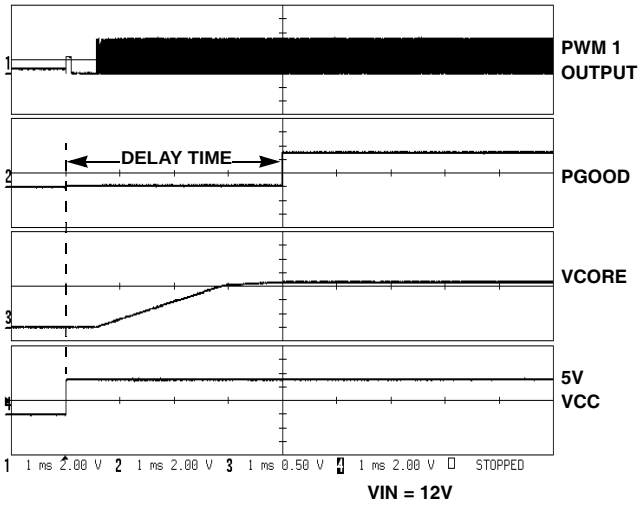


FIGURE 3. START-UP OF 4-PHASE SYSTEM OPERATING AT 500kHz

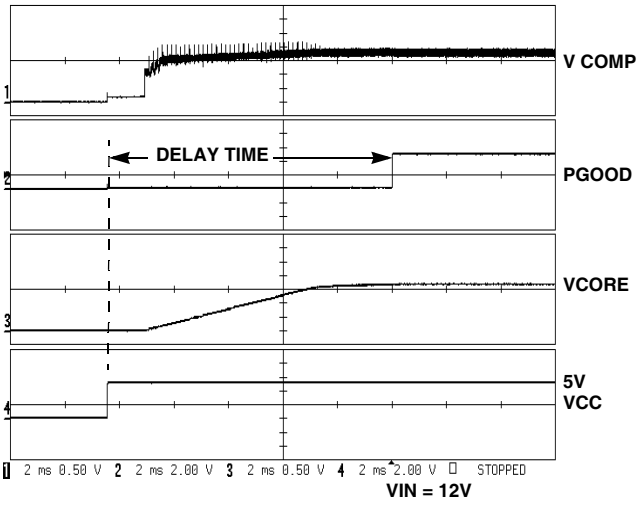
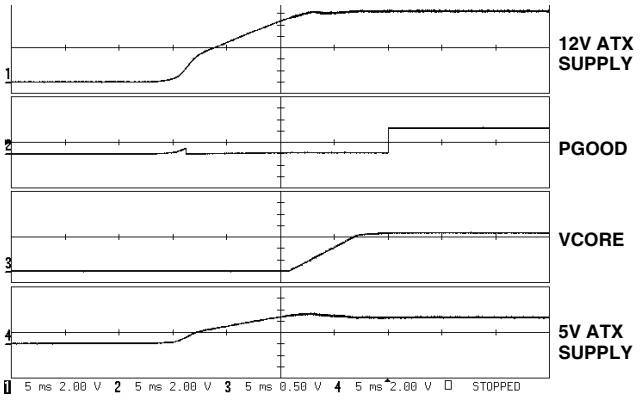


FIGURE 4. START-UP OF 4-PHASE SYSTEM OPERATING AT 200kHz



VIN = 5V, CORE LOAD CURRENT = 31A
FREQUENCY 200kHz
ATX SUPPLY ACTIVATED BY ATX “PS-ON PIN”

FIGURE 5. SUPPLY POWERED BY ATX SUPPLY

Note that Figure 5 shows the 12V gate driver voltage available before the 5V supply to the controller has reached its threshold level. If conditions were reversed and the 5V supply was to rise first, the start-up sequence would be different. In this case the controller may sense an overcurrent condition due to charging the output capacitors. The supply would then restart and go through the normal soft-start cycle.

Dynamic VID

The HIP6301V and HIP6302V require up to two full clock cycles to detect a change in the VID code. VID code changes that are not valid for at least two cycles may or may not be detected. Once detected, the controller waits an additional two-cycle wait period to be certain the change is stable. After the two-cycle wait period, the DAC begins stepping toward the new VID setting in 25mV increments. The DAC makes one 25mV step every two clock cycles. For example, a 500kHz system detecting a change from 1.300V to 1.800V requires between 84ms and 88ms to complete the change.

If a new VID code is detected during a DAC change and the DAC can continue toward the new VID code without changing direction, processing continues without interruption. If a new VID code is detected during a DAC change and the DAC has to change direction in order to proceed toward then new VID code, processing halts. A two-cycle wait period is initiated and processing continues as above. These decisions are made with reference to the transitional DAC value rather than the original target value.

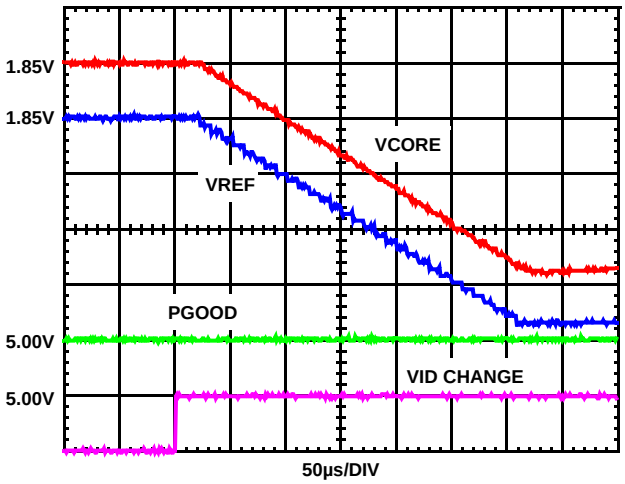


FIGURE 6. VCORE TRACKING THE REFERENCE VOLTAGE AFTER A 1.85V TO 1.10V CHANGE COMMAND

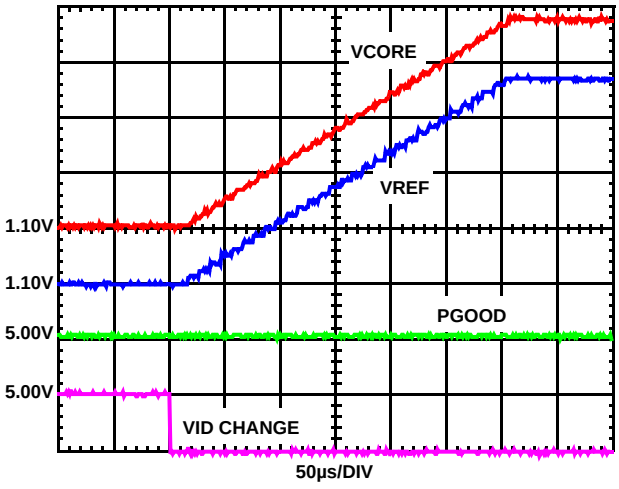


FIGURE 7. VCORE TRACKING THE REFERENCE VOLTAGE AFTER A 1.10V TO 1.85V CHANGE COMMAND

Fault Protection

The HIP6301V and HIP6302V protect the microprocessor and the entire power system from damaging stress levels. Within the controller, both overvoltage and overcurrent circuits are incorporated to protect the load and regulator.

Overvoltage

The VSEN pin is connected to the microprocessor CORE voltage. A CORE overvoltage condition is detected when the VSEN pin goes more than 15% above the programmed VID level.

The overvoltage condition is latched, disabling normal PWM operation, and causing PGOOD to go low. The latch can only be reset by lowering and returning V_{CC} high to initiate a POR and soft-start sequence.

During a latched overvoltage, the PWM outputs will be driven either low or three state, depending upon the VSEN input. PWM outputs are driven low when the VSEN pin detects that the CORE voltage is 15% above the programmed VID level. This condition drives the PWM outputs low, causing in the lower or MOSFETs to conduct and shunt the CORE voltage to ground to protect the load.

If after this event, the CORE voltage falls below the overvoltage limit (plus some hysteresis), the PWM outputs will be three state. The HIP6601 family drivers pass the three state information along, and shuts off both upper and lower MOSFETs. This prevents “dumping” of the output capacitors back through the lower MOSFETs, avoiding a possibly destructive ringing of the capacitors and output inductors. If the conditions that caused the overvoltage still persist, the PWM outputs will be cycled between three state and V_{CORE} clamped to ground, as a hysteretic shunt regulator.

Undervoltage

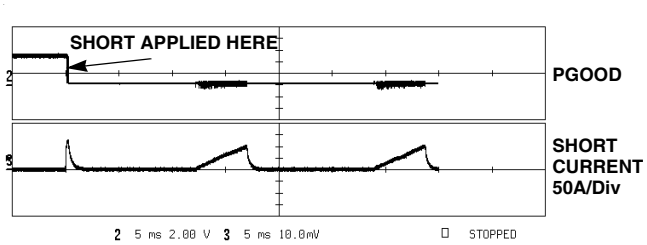
The VSEN pin also detects when the CORE voltage falls more than 10% below the VID programmed level. This causes PGOOD to go low, but has no other effect on operation and is not latched. There is also hysteresis in this detection point.

Overcurrent

In the event of an overcurrent condition, the overcurrent protection circuit reduces the average current delivered to less than 25% of the current limit. When an overcurrent condition is detected, the controller forces all PWM outputs into a three state mode. This condition results in the gate driver removing drive to the output stages. The controller goes into a wait delay timing cycle that is equal to the soft-start ramp time. PGOOD also goes “low” during this time due to VSEN going below its threshold voltage.To lower the average output dissipation, the soft-start initial wait time is increased from 32 to 2048 cycles, then the soft-start ramp is initiated. At a PWM frequency of 200kHz, for instance, an overcurrent detection would cause a dead time of 10.24ms, then a ramp of 10.08ms.

At the end of the delay, PWM outputs are restarted and the soft-start ramp is initiated. If a short is present at that time, the cycle is repeated. This is the hiccup mode.

Figure 8 shows the supply shorted under operation and the hiccup operating mode previously described. Note that due to the high short circuit current, overcurrent is detected before completion of the start-up sequence so the delay is not quite as long as the normal soft-start cycle.



HICCUP MODE. SUPPLY POWERED BY ATX SUPPLY
CORE LOAD CURRENT = 31A, 5V LOAD = 5A
SUPPLY FREQUENCY = 200kHz, VIN = 12V
ATX SUPPLY ACTIVATED BY ATX "PS-ON PIN"

FIGURE 8. SHORT APPLIED TO SUPPLY AFTER POWER-UP

CORE Voltage Programming

The voltage identification pins (VID0, VID1, VID3, and VID4) set the CORE output voltage. Each VID pin is pulled to 2.5V by an internal 20µA current source and accepts open-collector/ open-drain/open-switch-to-ground or standard low-voltage TTL or CMOS signals.

Table 1 shows the nominal DAC voltage as a function of the VID codes. The power supply system is ±0.8% accurate over the operating temperature and voltage range.

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600

TABLE 1. VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

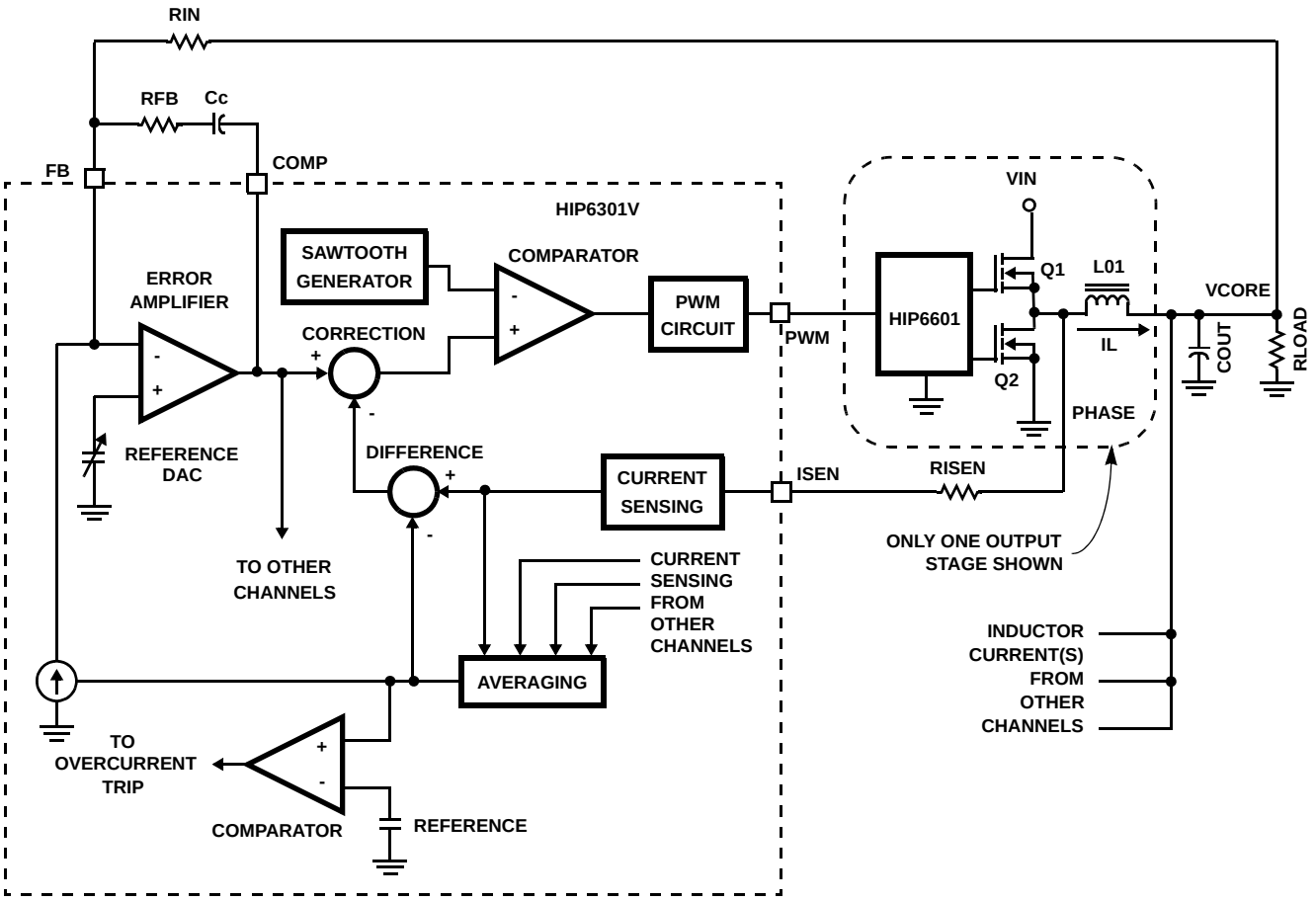


FIGURE 9. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM SHOWING CURRENT AND VOLTAGE SAMPLING

Current Sensing and Balancing

Overview

The HIP6301V and HIP6302V sample the on-state voltage drop across each synchronous MOSFET, Q_2, as an indication of the inductor current in that phase, see Figure 9. Neglecting AC effects (to be discussed later), the voltage drop across Q_2 is simply $r_{DS(ON)}(Q_2)$ x inductor current (I_L). Note that I_L, the inductor current, is either 1/2, 1/3, or 1/4 of the total current (I_{LT}), depending on how many phases are in use.

The voltage at Q_2's drain, the PHASE node, is applied to the R_{ISEN} resistor to develop the I_{ISEN} current through the ISEN pin. This pin is held at virtual ground, so the current through R_{ISEN} is shown in Equation 1:

$$I_L = \frac{r_{DS(ON)}(Q2)}{R_{ISEN}} \quad \text{(EQ. 1)}$$

The I_{ISEN} current provides information to perform the following functions:

1. Detection of an overcurrent condition
2. Reduce the regulator output voltage with increasing load current (droop)
3. Balance the I_L currents in multiple channels

Overcurrent, Selecting R_{ISEN}

The current detected through the R_{ISEN} resistor is averaged with the current(s) detected in the other 1, 2, or 3 channels. The averaged current is compared with a trimmed, internally generated current, and used to detect an overcurrent condition.

The nominal current through the R_{ISEN} resistor should be 50µA at full output load current, and the nominal trip point for overcurrent detection is 165% of that value, or 82.5µA (typical current levels) as shown in Equation 2. Therefore:

$$IR_{ISEN} = \frac{(I_L)r_{DS(ON)}(Q2)}{50\mu A} \quad \text{(EQ. 2)}$$

For a full load of 25A per phase, and an $r_{DS(ON)}$ (Q_2) of 4mΩ, R_{ISEN} = 2kΩ.

The overcurrent trip point would be 165% of 25A, or ~ 41A per phase. The R_{ISEN} value can be adjusted to change the overcurrent trip point, but it is suggested to stay within ±25% of nominal.

Droop, Selection of R_{IN}

The average of the currents detected through the R_{ISEN} resistors is also steered to the FB pin. There is no DC return path connected to the FB pin except for R_{IN}, so the average current creates a voltage drop across R_{IN}. This drop increases the apparent V_{CORE} voltage with increasing load current, causing the system to decrease V_{CORE} to maintain balance at the FB pin. This is the desired “droop” voltage used to maintain V_{CORE} within limits under transient conditions.

With a high dv/dt load transient, typical of high performance microprocessors, the largest deviations in output voltage occur at the leading and trailing edges of the load transient. In order to fully utilize the output-voltage tolerance range, the output voltage is positioned in the upper half of the range when the output is unloaded and in the lower half of the range when the controller is under full load. This droop compensation allows larger transient voltage deviations and thus reduces the size and cost of the output filter components.

R_{IN} should be selected to give the desired “droop” voltage at the normal full load current 50µA applied through the R_{ISEN} resistor (or at a different full load current if adjusted as in “Overcurrent, Selecting RISEN” on page 13).

$$R_{IN} = Vdroop/(50\mu A) \quad \text{(EQ. 3)}$$

For a Vdroop of 80mV, $R_{IN} = 1.6k\Omega$

The AC feedback components, R_{FB} and Cc, are scaled in relation to R_{IN}.

Current Balancing

The detected currents are also used to balance the phase currents.

Each phase’s current is compared to the average of all phase currents, and the difference is used to create an offset in that phase’s PWM comparator. The offset is in a direction to reduce the imbalance.

The balancing circuit can not make up for a difference in $r_{DS(ON)}$ between synchronous rectifiers. If a FET has a higher $r_{DS(ON)}$, the current through that phase will be reduced.

Figures 10 and 11 show the inductor current of a 2-phase system without and with current balancing.

Inductor Current

The inductor current in each phase of a multiphase buck converter has two components. There is a current equal to the load current divided by the number of phases (I_{LT}/n), and a sawtooth current, (I_{P-P}) resulting from switching. The sawtooth component is dependent on the size of the inductors, the switching frequency of each phase, and the values of the input and output voltage. Ignoring secondary effects, such as series resistance, the peak-to-peak value of the sawtooth current can be described by Equation 4.

$$I_{P-P} = \frac{V_{IN}(V_{CORE}) - V^2_{CORE}}{(L)(F_{SW})(V_{IN})} \quad \text{(EQ. 4)}$$

Where: V_{CORE} = DC value of the output or V_{ID} voltage
V_{IN} = DC value of the input or supply voltage
L = value of the inductor
F_{SW} = switching frequency

Example: For V_{CORE} = 1.6V,
V_{IN} = 12V,
L = 1.3µH,
F_{SW} = 250kHz,
Then I_{P-P} = 4.3A

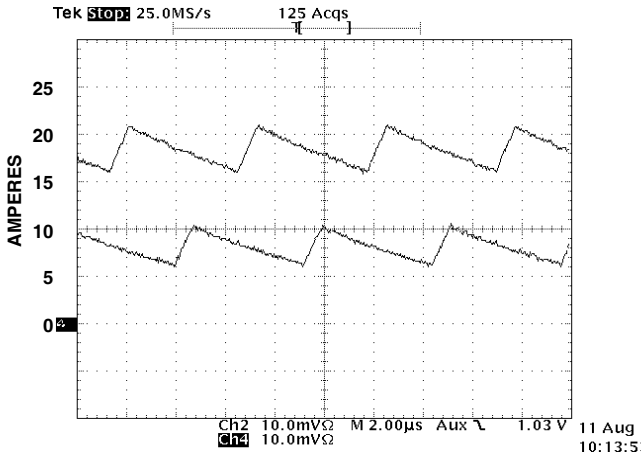


FIGURE 10. TWO CHANNEL MULTIPHASE SYSTEM WITH CURRENT BALANCING DISABLED

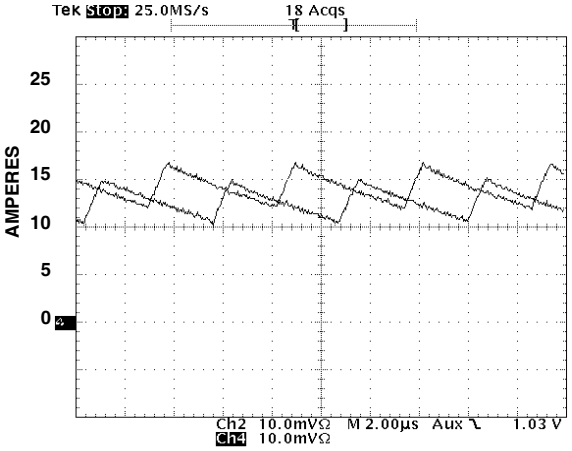


FIGURE 11. TWO CHANNEL MULTIPHASE SYSTEM WITH CURRENT BALANCING ENABLED

The inductor, or load current, flows alternately from V_{IN} through Q_1 and from ground through Q_2. The controller samples the on-state voltage drop across each Q_2 transistor to indicate the inductor current in that phase. The voltage drop is sampled 1/3 of a switching period, $1/F_{SW}$, after Q_1 is

turned OFF and Q_2 is turned on. Because of the sawtooth current component, the sampled current is different from the average current per phase. Neglecting secondary effects, the sampled current (I_{SAMPLE}) can be related to the load current (I_{LT}) by Equation 5.

$$I_{SAMPLE} = \frac{\frac{I_{LT}}{n} + (V_{IN})V_{CORE} - 3V_{CORE}^2}{(6L)(F_{SW})(V_{IN})} \quad \text{(EQ. 5)}$$

Where: I_{LT} = total load current
n = the number of channels

Example: Using the previously given conditions, and for I_{LT} = 100A,
n = 4

Then I_{SAMPLE} = 25.49A

As discussed previously, the voltage drop across each Q_2 transistor at the point in time when current is sampled is $r_{DS(ON)}$ (Q_2) x I_{SAMPLE}. The voltage at Q_2's drain, the PHASE node, is applied through the R_{ISEN} resistor to the HIP6301V ISEN pin. This pin is held at virtual ground, so the current into ISEN is calculated in Equations 6 and 7:

$$I_{SENSE} = \frac{(I_{SAMPLE})r_{DS(ON)}(Q2)}{R_{ISEN}} \quad \text{(EQ. 6)}$$

$$R_{ISEN} = \frac{(I_{SAMPLE})r_{DS(ON)}(Q2)}{50\mu A} \quad \text{(EQ. 7)}$$

Example: From the previous conditions,

where I_{LT} = 100A,
I_{SAMPLE} = 25.49A,
$r_{DS(ON)}$ (Q_2) = 4mΩ
Then: R_{ISEN} = 2.04k and
$I_{CURRENT\ TRIP}$ = 165%
Short circuit I_{LT} = 165A.

Channel Frequency Oscillator

The channel oscillator frequency is set by placing a resistor, R_T, to ground from the FS/DIS pin. Figure 12 is a curve showing the relationship between frequency, F_{SW}, and resistor R_T. To avoid pickup by the FS/DIS pin, it is important to place this resistor next to the pin.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes. Contact Intersil for evaluation board drawings of the component placement and printed circuit board.

There are two sets of critical components in a DC/DC converter using a HIP6301V or HIP6302V controller and a HIP6601 family gate driver. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

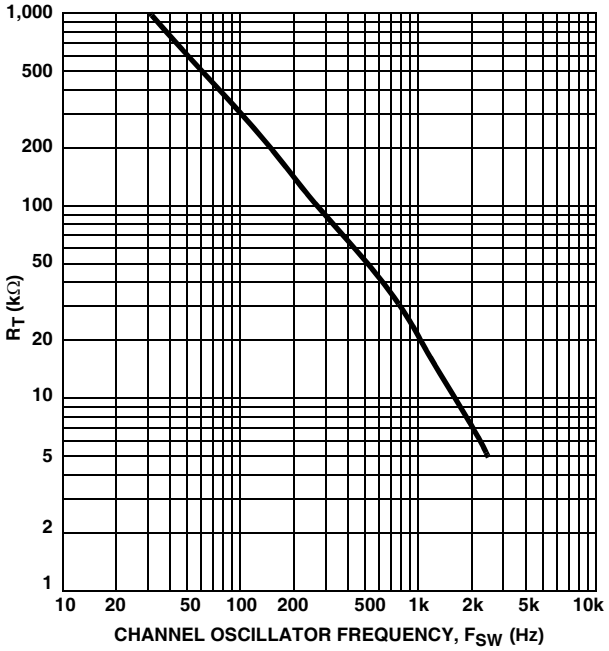


FIGURE 12. RESISTANCE R_T vs FREQUENCY

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches. Locate the output inductors and output capacitors between the MOSFETs and the load. Locate the gate driver close to the MOSFETs.

The critical small components include the bypass capacitors for VCC and PVCC on the gate driver ICs. Locate the bypass capacitor, C_{BP}, for the controller close to the device. It is especially important to locate the resistors associated with the input to the amplifiers close to their respective pins, since they represent the input to feedback amplifiers. Resistor R_T, that sets the oscillator frequency should also be located next to the associated pin. It is especially important to place the R_{SEN} resistor(s) at the respective ISEN terminals.

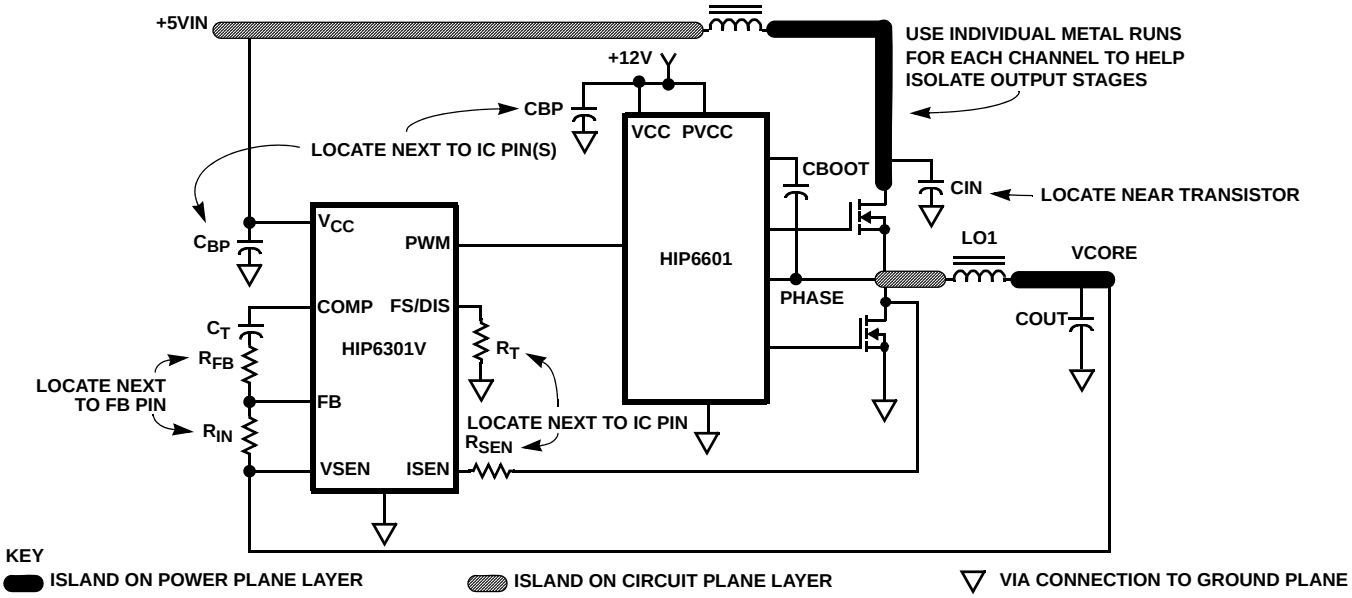


FIGURE 13. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

A multi-layer printed circuit board is recommended. Figure 13 shows the connections of the critical components for one output channel of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, (usually the middle layer of the PC board), for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to inductor L_{O1} short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the driver IC to the MOSFET gate and source should be sized to carry at least one ampere of current.

Component Selection Guidelines

Output Capacitor Selection

The output capacitor is selected to meet both the dynamic load requirements and the voltage ripple requirements. The load transient for the microprocessor CORE is characterized by high slew rate (di/dt) current demands. In general, multiple high quality capacitors of different size and dielectric are paralleled to meet the design constraints.

Modern microprocessors produce severe transient load rates. High frequency capacitors supply the initially transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. In most cases, multiple capacitors of small case size perform better than a single large case capacitor.

Bulk capacitor choices include aluminum electrolytic, OS-Con, Tantalum and even ceramic dielectrics. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Consult the capacitor manufacturer and measure the capacitor's impedance with frequency to select a suitable component.

Output Inductor Selection

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Small inductors in a multi-phase converter reduce the response time without significant increases in total ripple current.

The output inductor of each power channel controls the ripple current. The control IC is stable for channel ripple current (peak-to-peak) up to twice the average current. A

single channel's ripple current is approximtely calculated in Equation 8:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 8)}$$

The current from multiple channels tend to cancel each other and reduce the total ripple current. Figure 14 gives the total ripple current as a function of duty cycle, normalized to the parameter $(Vo)/(LxF_{SW})$ at zero duty cycle. To determine the total ripple current from the number of channels and the duty cycle, multiply the y-axis value by $(Vo)/(LxF_{SW})$.

Small values of output inductance can cause excessive power dissipation. The HIP6301V and HIP6302V are designed for stable operation for ripple currents up to twice the load current. However, for this condition, the RMS current is 115% above the value shown in "MOSFET Selection and Considerations" on page 17. With all else fixed, decreasing the inductance could increase the power dissipated in the MOSFETs by 30%.

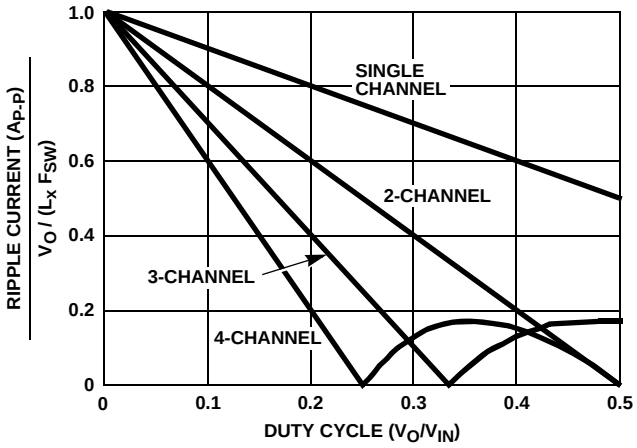


FIGURE 14. RIPPLE CURRENT vs DUTY CYCLE

Input Capacitor Selection

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and a voltage rating of 1.5x is a conservative guideline. The RMS current required for a multi-phase converter can be approximated with the aid of Figure 15.

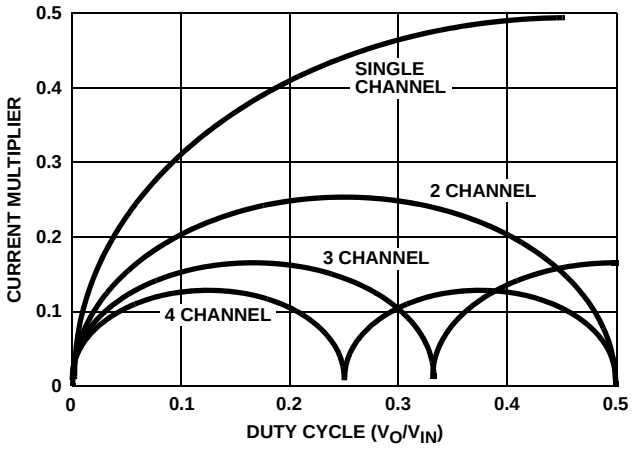


FIGURE 15. CURRENT MULTIPLIER vs DUTY CYCLE

First determine the operating duty ratio as the ratio of the output voltage divided by the input voltage. Find the current multiplier from the curve with the appropriate power channels. Multiply the current multiplier by the full load output current. The resulting value is the RMS current rating required by the input capacitor.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors should be placed very close to the drain of the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For bulk capacitance, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see Equation 9). The conduction losses are the main component of power dissipation for the lower MOSFETs, Q_2 and Q_4 of Figure 1. Only the upper MOSFETs, Q_1 and Q_3 have significant switching losses, since the lower device turns on and off into near zero voltage.

The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode. The gate-charge losses are dissipated by the Driver IC and don't heat the MOSFETs.

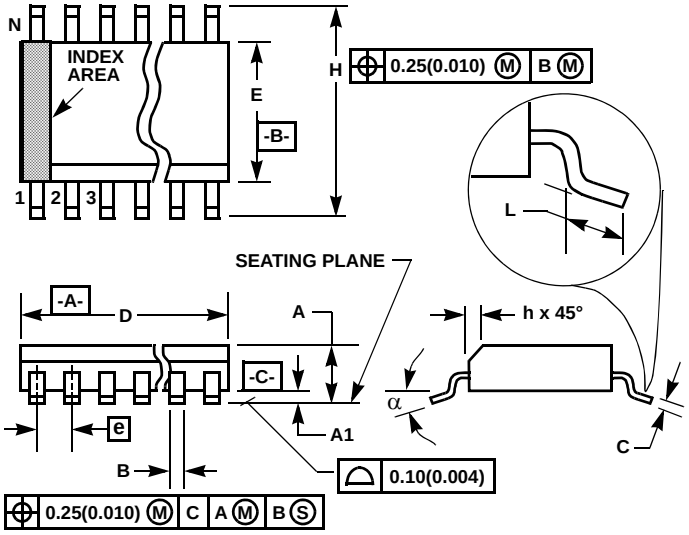
However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_{SW}}{2} \quad \text{(EQ. 9)}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

A diode, anode to ground, may be placed across Q_2 and Q_4 of Figure 1. These diodes function as a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFETs and the turn on of the upper MOSFETs. The diodes must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is usually acceptable to omit the diodes and let the body diodes of the lower MOSFETs clamp the negative inductor swing, but efficiency could drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Small Outline Plastic Packages (SOIC)



NOTES:

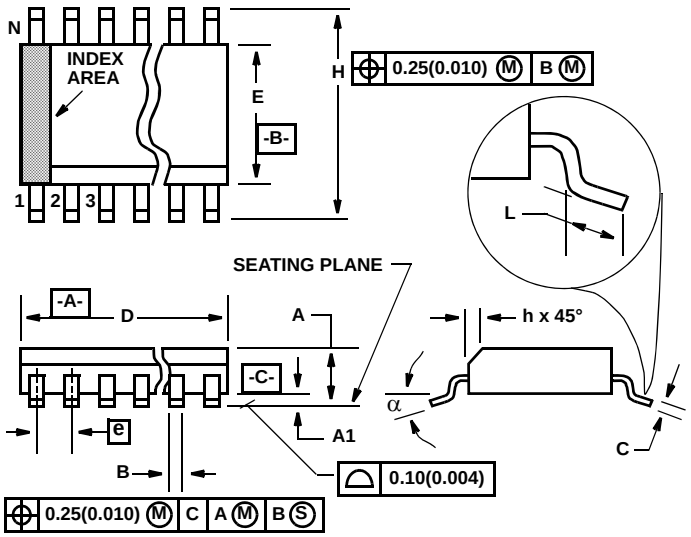
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 2 6/05

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.