19-3379; Rev 0; 8/04

Dual, 256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

General Description

The MAX5477/MAX5478/MAX5479 nonvolatile, dual, linear-taper, digital potentiometers perform the function of a mechanical potentiometer, but replace the mechanics with a simple 2-wire digital interface. Each device performs the same function as a discrete potentiometer or variable resistor and has 256 tap points.

The devices feature an internal, nonvolatile EEPROM used to store the wiper position for initialization during power-up. A write-protect feature prevents accidental overwrites of the EEPROM. The fast-mode I²C™-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnection complexity in many applications. Three address inputs allow a total of eight unique address combinations.

The MAX5477/MAX5478/MAX5479 provide three nominal resistance values: 10kΩ (MAX5477), 50kΩ (MAX5478), or 100kΩ (MAX5479). The nominal resistor temperature coefficient is 35ppm/°C end-to-end and 5ppm/°C ratiometric. The low temperature coefficient makes the devices ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain-amplifier circuit configurations.

The MAX5477/MAX5478/MAX5479 are available in 16-pin 3mm x 3mm x 0.8mm thin QFN and 14-pin 4.4mm x 5mm TSSOP packages. These devices operate over the extended -40°C to +85°C temperature range.

Applications

Mechanical Potentiometer Replacement

Low-Drift Programmable-Gain Amplifiers

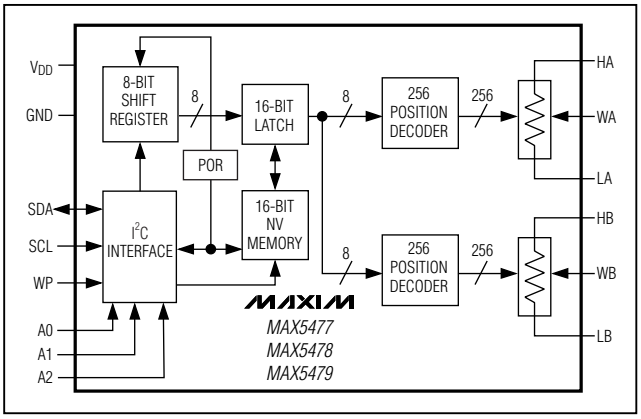
Volume Control

Liquid-Crystal Display (LCD) Contrast Control

Features

- **Power-On Recall of Wiper Position from Nonvolatile Memory**
- **EEPROM Write Protection**
- **Tiny 3mm x 3mm x 0.8mm Thin QFN Package**
- **35ppm/°C End-to-End Resistance Temperature Coefficient**
- **5ppm/°C Ratiometric Temperature Coefficient**
- **Fast 400kbps I²C-Compatible Serial Interface**
- **1µA (max) Static Supply Current**
- **Single-Supply Operation: +2.7V to +5.25V**
- **256 Tap Positions per Potentiometer**
- **±0.5 LSB DNL in Voltage-Divider Mode**
- **±1 LSB INL in Voltage-Divider Mode**

Functional Diagram



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Purchase of I²C components from Maxim Integrated Products, Inc. or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	END-TO-END RESISTANCE (kΩ)	TOP MARK	PACKAGE CODE
MAX5477ETE*	-40°C to +85°C	16 Thin QFN	10	ABO	T1633F-3
MAX5477EUD*	-40°C to +85°C	14 TSSOP	10	—	—
MAX5478ETE	-40°C to +85°C	16 Thin QFN	50	ABP	T1633F-3
MAX5478EUD	-40°C to +85°C	14 TSSOP	50	—	—
MAX5479ETE*	-40°C to +85°C	16 Thin QFN	100	ABQ	T1633F-3
MAX5479EUD*	-40°C to +85°C	14 TSSOP	100	—	—

**Future product—contact factory for availability.*

Pin Configurations appear at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
All Other Pins to GND.....-0.3V to (V_{DD} + 0.3V)
Maximum Continuous Current into H_, L_, and W_
MAX5477.....±5.0mA
MAX5478.....±1.3mA
MAX5479.....±0.6mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 17.5mW/°C above +70°C) 1399mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H_ = V_{DD}, L_ = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (VOLTAGE-DIVIDER MODE)						
Resolution				256		Taps
Integral Nonlinearity	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	(Note 2)			±0.5	LSB
Dual Code Matching		R0 and R1 set to same code (all codes)			±1	LSB
End-to-End Resistance Temperature Coefficient	TC_R			35		ppm/°C
Ratiometric Resistance Temperature Coefficient				5		ppm/°C
Full-Scale Error		MAX5477		-3		LSB
		MAX5478		-0.6		
		MAX5479		-0.3		
Zero-Scale Error		MAX5477		3		LSB
		MAX5478		0.6		
		MAX5479		0.3		
DC PERFORMANCE (VARIABLE-RESISTOR MODE)						
Integral Nonlinearity (Note 3)	INL	V_{DD} = 3V			±3	LSB
		V_{DD} = 5V			±1.5	
Differential Nonlinearity (Note 3)	DNL	V_{DD} = 3V, MAX5477, guaranteed monotonic			±1	LSB
		V_{DD} = 3V, MAX5478			±1	
		V_{DD} = 3V, MAX5479			±1	
		V_{DD} = 5V			±1	
Dual Code Matching		R0 and R1 set to same code (all codes), V_{DD} = 3V or 5V			±3	LSB
DC PERFORMANCE (RESISTOR CHARACTERISTICS)						
Wiper Resistance	R_W	(Note 4)		325	675	Ω
Wiper Capacitance	C_W			10		pF
End-to-End Resistance	R_{HL}	MAX5477	7.5	10	12.5	kΩ
		MAX5478	37.5	50	62.5	
		MAX5479	75	100	125	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H_ = V_{DD}, L_ = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage (Note 5)	V_{IH}	V_{DD} = 3.4V to 5.25V		2.4			V
		V_{DD} < 3.4V		0.7 x V_{DD}			
Input Low Voltage	V_{IL}	(Note 5)				0.8	V
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
WP Pullup Resistance	I_{WP}			255			kΩ
Input Leakage Current	I_{LEAK}					±1	µA
Input Capacitance					5		pF
DYNAMIC CHARACTERISTICS							
Crosstalk		HA = 1kHz (0 to V_{DD}), LA = GND, LB = GND, measure WB			80		dB
3dB Bandwidth		MAX5478 (Note 6)			100		kHz
Total Harmonic Distortion Plus Noise	THD+N	H_ = $1V_{RMS}$, f = 1kHz, L_ = GND, measure W_			0.003		%
NONVOLATILE MEMORY RELIABILITY							
Data Retention		T_A = +85°C			50		Years
Endurance		T_A = +25°C			200,000		Stores
		T_A = +85°C			50,000		
POWER SUPPLY							
Power-Supply Voltage	V_{DD}			2.70		5.25	V
Supply Current	I_{DD}	Writing to EEPROM, digital inputs at GND or V_{DD} (Note 7)			250	400	µA
		Normal operation, digital inputs at GND or V_{DD}	WP = GND		15	20.6	
			WP = V_{DD}		0.5	1	

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H_ = V_{DD}, L_ = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C. See Figure 1.) (Notes 8 and 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SECTION						
Wiper Settling Time	t_{WS}	MAX5478 (Note 10)		500		ns
DIGITAL SECTION						
SCL Clock Frequency	f_{SCL}				400	kHz
Setup Time for START Condition	t_{SU-STA}		0.6			µs
Hold Time for START Condition	t_{HD-STA}		0.6			µs
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs

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TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H_ = V_{DD}, L_ = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C. See Figure 1.) (Notes 8 and 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	t_{SU-DAT}		100			ns
Data Hold Time	t_{HD-DAT}		0		0.9	µs
SDA, SCL Rise Time	t_R				300	ns
SDA, SCL Fall Time	t_F				300	ns
Setup Time for STOP Condition	t_{SU-STO}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}	Minimum power-up rate = 0.2V/µs	1.3			µs
Pulse Width of Spike Suppressed	t_{SP}				50	ns
Capacitive Load for Each Bus Line	C_B	(Note 11)			400	pF
Write NV Register Busy Time		(Note 12)			12	ms

Note 1: All devices are production tested at T_A = +25°C and are guaranteed by design and characterization for -40°C < T_A < +85°C.

Note 2: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H_ = V_{DD} and L_ = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

Note 3: The DNL and INL are measured with the potentiometer configured as a variable resistor. H_ is unconnected and L_ = GND. For V_{DD} = +5V, the wiper is driven with 400µA (MAX5477), 80µA (MAX5478), or 40µA (MAX5479). For V_{DD} = +3V, the wiper is driven with 200µA (MAX5477), 40µA (MAX5478), or 20µA (MAX5479).

Note 4: The wiper resistance is measured using the source currents given in Note 3.

Note 5: The devices draw current in excess of the specified supply current when the digital inputs are driven with voltages between (V_{DD} - 0.5V) and (GND + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

Note 6: Wiper at midscale with a 10pF load (DC measurement). L_ = GND, an AC source is applied to H_, and the W_ output is measured. A 3dB bandwidth occurs when the AC W_/H_ value is 3dB lower than the DC W_/H_ value.

Note 7: The programming current exists only during power-up and EEPROM writes.

Note 8: The SCL clock period includes rise and fall times (t_R = t_F). All digital input signals are specified with t_R = t_F = 2ns and timed from a voltage level of (V_{IL} + V_{IH}) / 2.

Note 9: Digital timing is guaranteed by design and characterization, and is not production tested.

Note 10: This is measured from the STOP pulse to the time it takes the output to reach 50% of the output step size (divider mode). It is measured with a maximum external capacitive load of 10pF.

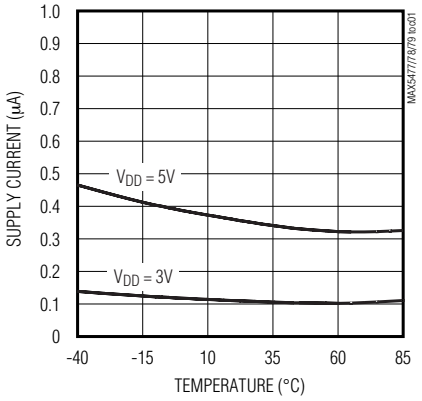
Note 11: An appropriate bus pullup resistance must be selected depending on board capacitance. Refer to the I²C-bus specification document linked to this web address: www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf

Note 12: The idle time begins from the initiation of the STOP pulse.

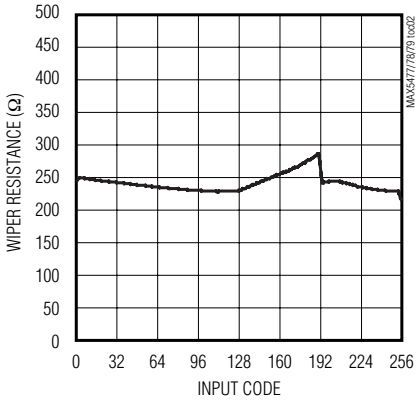
Typical Operating Characteristics

(V_{DD} = +5V, H_ = V_{DD}, L_ = GND, T_A = +25°C, unless otherwise noted.)

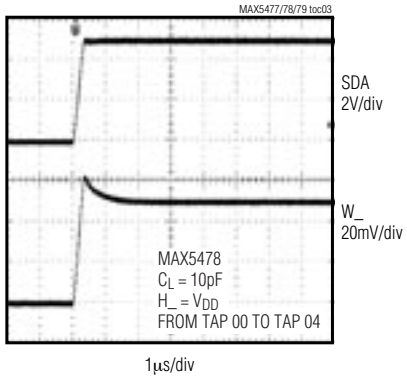
SUPPLY CURRENT vs. TEMPERATURE



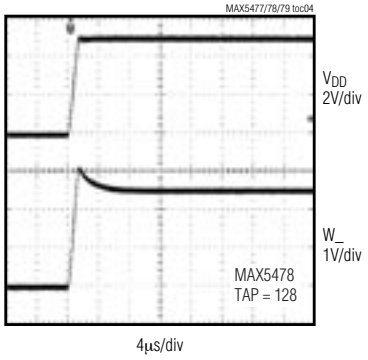
WIPER RESISTANCE vs. INPUT CODE



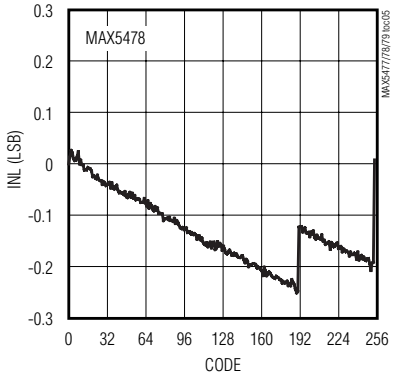
TAP-TO-TAP SWITCHING TRANSIENT



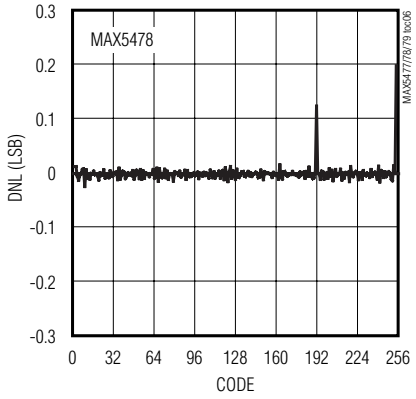
WIPER TRANSIENT AT POWER-ON



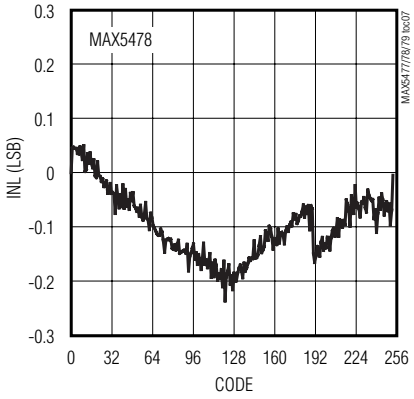
INTEGRAL NONLINEARITY vs. CODE (VDM MODE)



DIFFERENTIAL NONLINEARITY vs. CODE (VDM MODE)



INTEGRAL NONLINEARITY vs. CODE (VRM MODE)

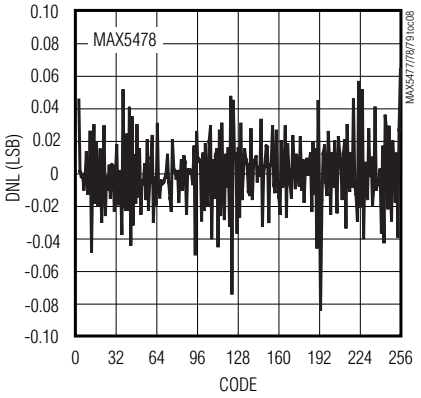


Dual, 256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

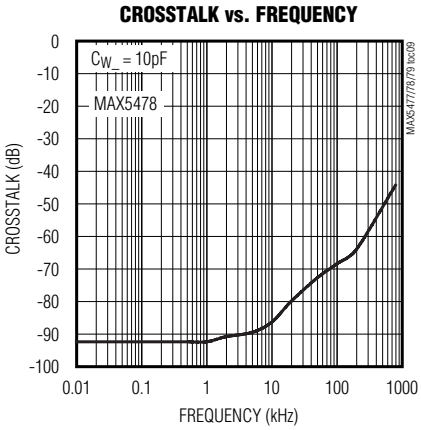
Typical Operating Characteristics (continued)

(V_{DD} = +5V, H_ = V_{DD}, L_ = GND, T_A = +25°C, unless otherwise noted.)

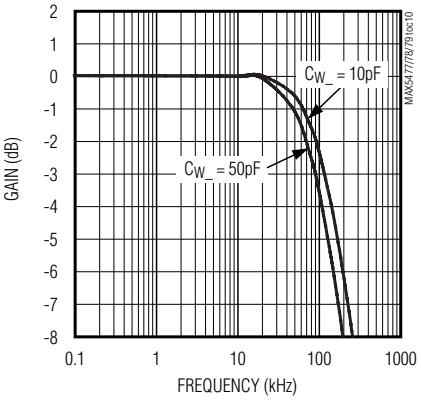
DIFFERENTIAL NONLINEARITY vs. CODE (VRM MODE)



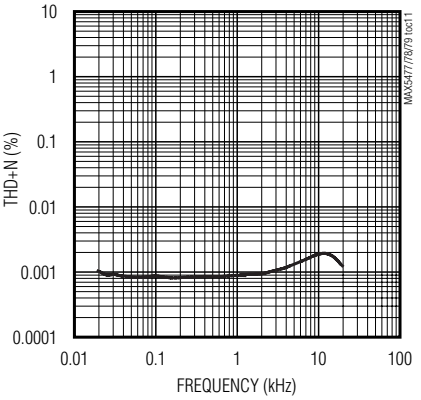
CROSSTALK vs. FREQUENCY



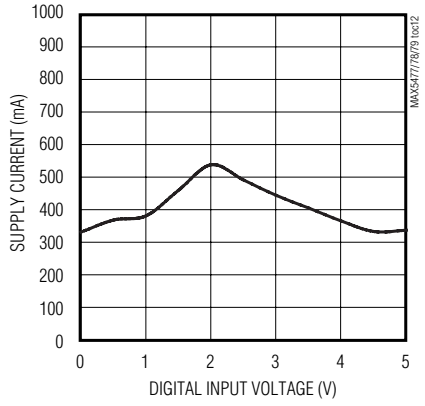
MIDSCALE WIPER RESPONSE vs. FREQUENCY (MAX5478)



THD+N vs. FREQUENCY



SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



Pin Description

PIN		NAME	FUNCTION
TSSOP	THIN QFN		
1	15	HA	Potentiometer A High Terminal
2	14	WA	Potentiometer A Wiper Terminal
3	13	LA	Potentiometer A Low Terminal
4	12	HB	Potentiometer B High Terminal
5	11	WB	Potentiometer B Wiper Terminal
6	10	LB	Potentiometer B Low Terminal
7	9	WP	Write-Protect Input. Connect to GND to allow changes to the wiper position and the data stored in the EEPROM. Connect to V_{DD} or leave open to enable the write protection of the EEPROM.
8	7	GND	Ground
9	6	A2	Address Input 2. Connect to V_{DD} or GND (see Table 1).
10	5	A1	Address Input 1. Connect to V_{DD} or GND (see Table 1).
11	4	A0	Address Input 0. Connect to V_{DD} or GND (see Table 1).
12	3	SDA	I²C Serial Data
13	2	SCL	I²C Clock Input
14	1	V_{DD}	Power-Supply Input. Connect a +2.7V to +5.25V power supply to V_{DD} and bypass V_{DD} to GND with a 0.1µF capacitor installed as close to the device as possible.
—	8, 16	N.C.	No Connection. Not internally connected.
—	EP	EP	Exposed Paddle. Connect to GND or leave floating.

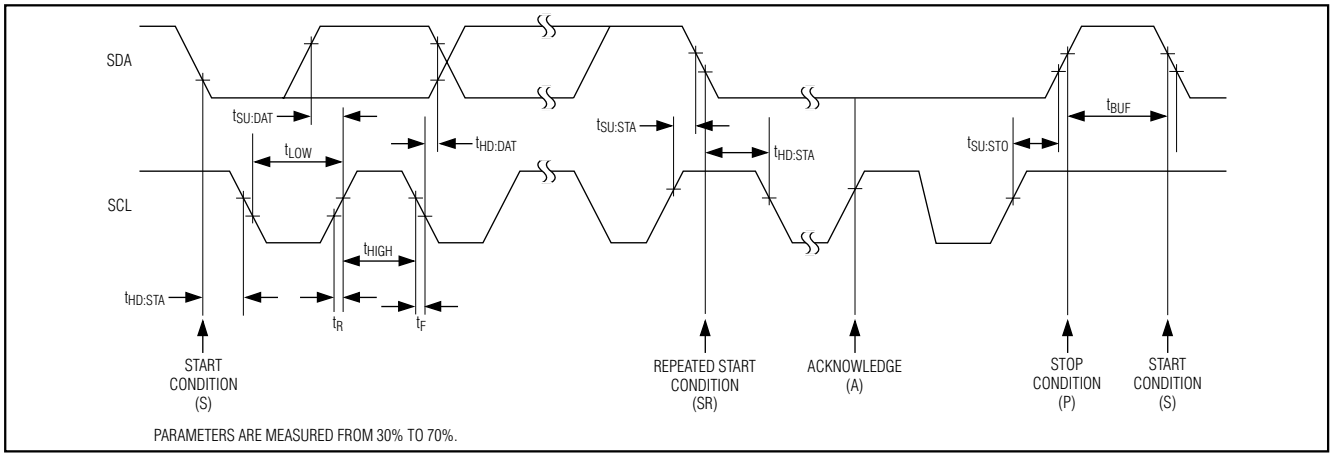


Figure 1. I²C Serial-Interface Timing Diagram

Detailed Description

The MAX5477/MAX5478/MAX5479 contain two resistor arrays with 255 elements in each array. The MAX5477 has a total end-to-end resistance of 10kΩ, the MAX5478 has an end-to-end resistance of 50kΩ, and the MAX5479 has an end-to-end resistance of 100kΩ.

The MAX5477/MAX5478/MAX5479 provide access to the high, low, and wiper terminals for a standard voltage-divider configuration. Connect H_, L_, and W_ in any desired configuration as long as their voltages remain between GND and V_{DD}.

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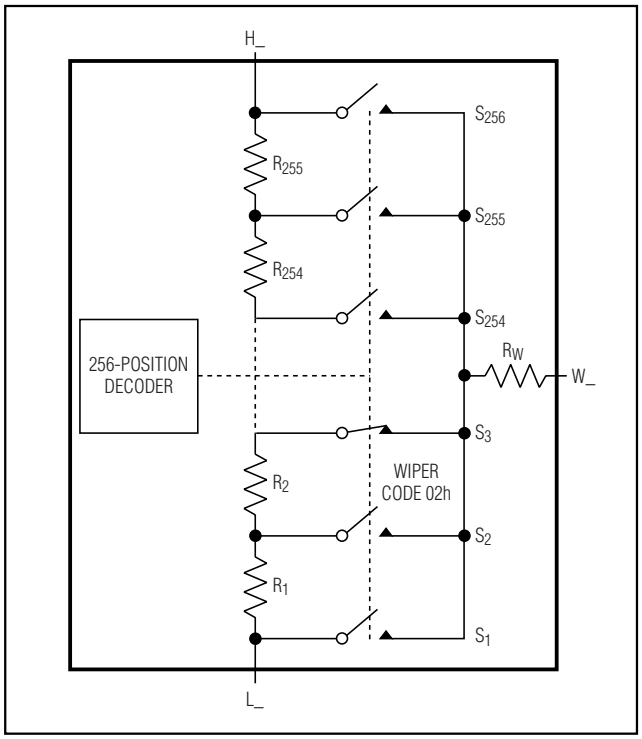


Figure 2. Potentiometer Configuration

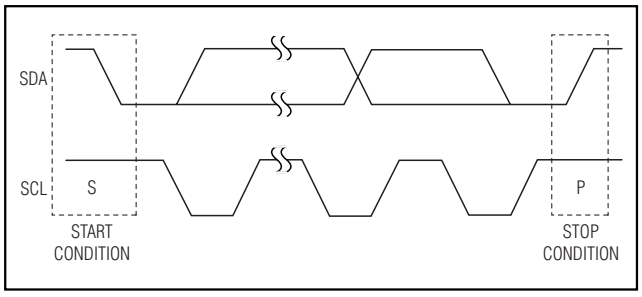


Figure 3. Start and Stop Conditions

A simple 2-wire I²C-compatible serial interface moves the wiper among the 256 tap points (Figure 2). A nonvolatile memory stores the wiper position and recalls the stored wiper position upon power-up. The nonvolatile memory is guaranteed for 50 years for wiper data retention and up to 200,000 wiper store cycles.

Analog Circuitry

The MAX5477/MAX5478/MAX5479 consist of two resistor arrays with 255 resistive elements; 256 tap points are accessible to the wipers, along the resistor string between H_ and L_. The wiper tap point is selected by programming the potentiometer through the I²C interface. An address byte, a command byte, and 8 data bits program the wiper position for each potentiometer. The H_ and L_ terminals of the MAX5477/MAX5478/MAX5479 are similar to the two end terminals of a mechanical potentiometer. The MAX5477/MAX5478/MAX5479 feature power-on reset circuitry that loads the wiper position from the nonvolatile memory at power-up.

Digital Interface

The MAX5477/MAX5478/MAX5479 feature an internal, nonvolatile EEPROM that stores the wiper state for initialization during power-up. The shift register decodes the command and address bytes, routing the data to the proper memory registers. Data written to a volatile memory register immediately updates the wiper position, or writes data to a nonvolatile register for storage (see Table 2).

The volatile register retains data as long as the device is powered. Removing power clears the volatile register. The nonvolatile register retains data even after power is removed. Upon power-up, the power-on reset circuitry controls the transfer of data from the nonvolatile register to the volatile register.

A write-protect feature prevents accidental overwriting of the EEPROM. Connect WP to V_{DD} or leave open to prevent any EEPROM write cycles. The wiper register only updates with the value in the EEPROM when WP =

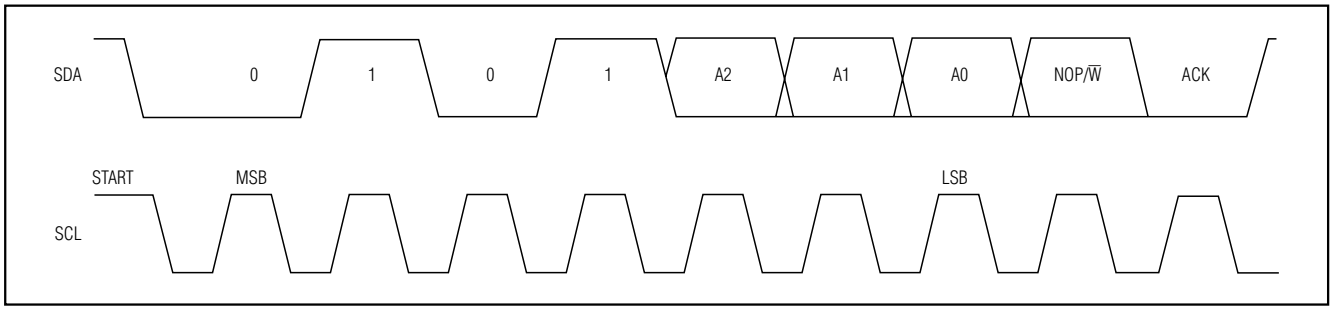


Figure 4. Slave Address

Table 1. Slave Addresses

ADDRESS INPUTS			SLAVE ADDRESS
A2	A1	A0	
GND	GND	GND	0101000
GND	GND	V_{DD}	0101001
GND	V_{DD}	GND	0101010
GND	V_{DD}	V_{DD}	0101011
V_{DD}	GND	GND	0101100
V_{DD}	GND	V_{DD}	0101101
V_{DD}	V_{DD}	GND	0101110
V_{DD}	V_{DD}	V_{DD}	0101111

V_{DD}. Connect WP to GND to allow write commands to the EEPROM and to update the wiper position from either the value in the EEPROM or directly from the I²C interface. Connecting WP to GND increases the supply current by 19.6µA (max).

Serial Addressing

The MAX5477/MAX5478/MAX5479 operate as slave devices that send and receive data through an I²C-/SMBus™-compatible 2-wire serial interface. The interface uses a serial data access (SDA) line and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to the MAX5477/MAX5478/MAX5479, and generates the SCL clock that synchronizes the data transfer (Figure 1).

The MAX5477/MAX5478/MAX5479 SDA line operates as both an input and an open-drain output. The SDA line requires a pullup resistor, typically 4.7kΩ. The MAX5477/MAX5478/MAX5479 SCL line operates only as an input. The SCL line requires a pullup resistor (typically 4.7kΩ) if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. SCL and SDA should not exceed V_{DD} in a mixed-voltage system, despite the open-drain drivers.

Each transmission consists of a START (S) condition (Figure 3) sent by a master, followed by the MAX5477/MAX5478/MAX5479 7-bit slave address plus the NOP/$\overline{W}$ bit (Figure 4), 1 command byte and 1 data byte, and finally a STOP (P) condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master controller signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master controller issues a STOP condition by transitioning the SDA from low to high while SCL is high, when it finishes communicating with the slave. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 5).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 6). Thus, each byte transferred effectively requires 9 bits. The master controller generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line remains stable low during the high period of the clock pulse.

Slave Address

The MAX5477/MAX5478/MAX5479 have a 7-bit-long slave address (Figure 4). The 8th bit following the 7-bit

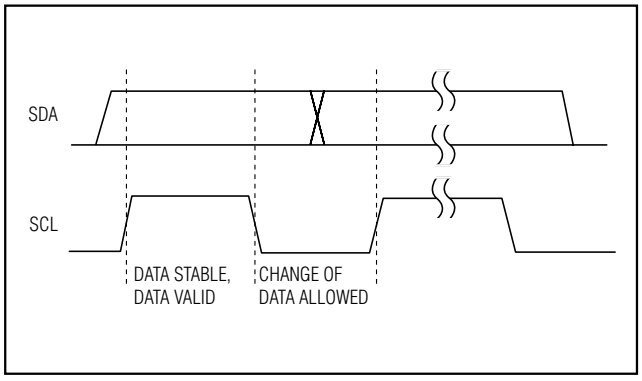


Figure 5. Bit Transfer

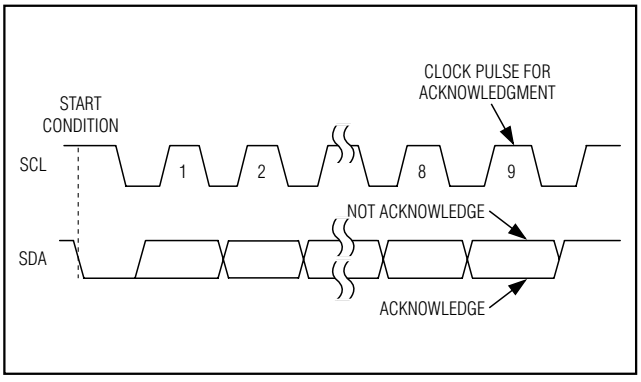


Figure 6. Acknowledge

SMBus is a trademark of Intel Corporation.

Dual, 256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

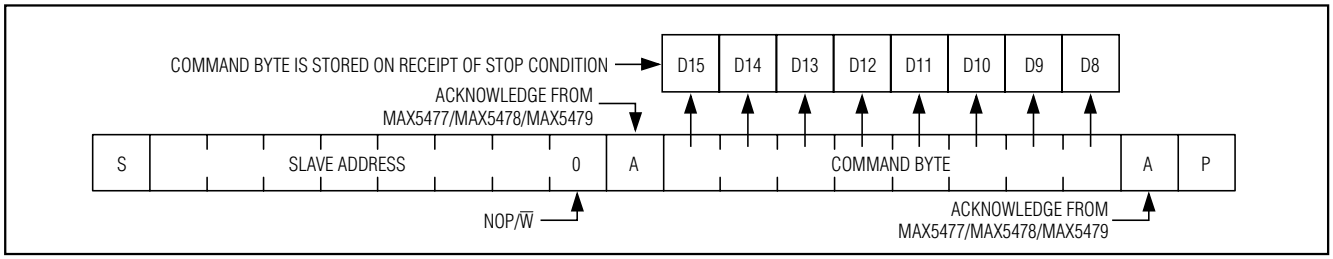


Figure 7. Command Byte Received

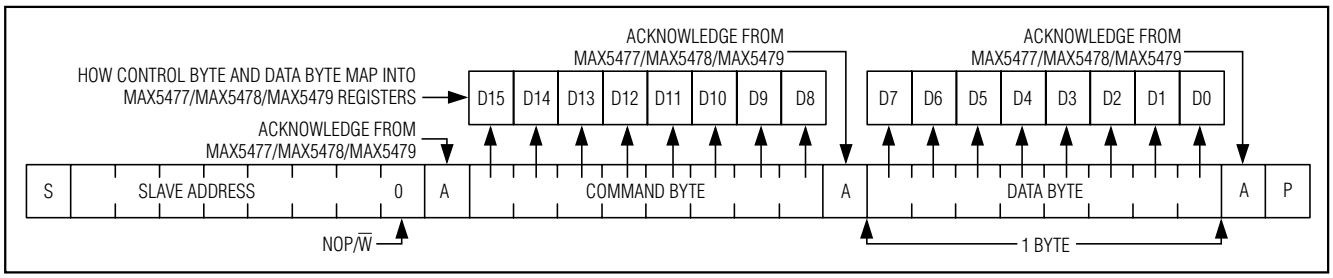


Figure 8. Command and Single Data Byte Received

slave address is the NOP/$\overline{W}$ bit. Set the NOP/$\overline{W}$ bit low for a write command and high for a no-operation command.

The MAX5477/MAX5478/MAX5479 provide three address inputs (A0, A1, and A2), allowing up to eight devices to share a common bus (Table 1). The first 4 bits (MSBs) of the MAX5477/MAX5478/MAX5479 slave addresses are always 0101. A2, A1, and A0 set the next 3 bits in the slave address. Connect each address input to V_{DD} or GND to set these 3 bits. Each device must have a unique address to share a common bus.

Message Format for Writing

Write to the MAX5477/MAX5478/MAX5479 by transmitting the device's slave address with NOP/$\overline{W}$ (8th bit) set to zero, followed by at least 1 byte of information (Figure 7). The 1st byte of information is the command byte. The bytes received after the command byte are the data bytes. The 1st data byte goes into the internal register of the MAX5477/MAX5478/MAX5479 as selected by the command byte (Figure 8).

Command Byte

Use the command byte to select the source and destination of the wiper data (nonvolatile or volatile memory registers) and swap data between nonvolatile and volatile memory registers (see Table 2).

Command Descriptions

VREG: The data byte writes to the volatile memory register and the wiper position updates with the data in the volatile memory register.

NVREG: The data byte writes to the nonvolatile memory register. The wiper position is unchanged.

NVREGxVREG: Data transfers from the nonvolatile memory register to the volatile memory register (wiper position updates).

VREGxNVREG: Data transfers from the volatile memory register into the nonvolatile memory register.

Nonvolatile Memory

The internal EEPROM consists of a 16-bit nonvolatile register that retains the value written to it prior to power down. The nonvolatile register is programmed with the midscale value at the factory. The nonvolatile memory is guaranteed for 50 years for wiper position retention and up to 200,000 wiper write cycles. A write-protect feature prevents accidental overwriting of the EEPROM. Connect WP to V_{DD} or leave open to enable the write-protect feature. The wiper position only updates with the value in the EEPROM when WP = V_{DD}. Connect WP to GND to allow EEPROM write cycles and to update the wiper position from nonvolatile memory or directly from the I²C serial interface.

Power-Up

Upon power-up, the MAX5477/MAX5478/MAX5479 load the data stored in the nonvolatile memory register into the volatile memory register, updating the wiper position with the data stored in the nonvolatile memory register. This initialization period takes 10µs.

Table 2. Command Byte Summary

		ADDRESS BYTE									COMMAND BYTE									DATA BYTE										
SCL CYCLE NUMBER	START (S)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	STOP (P)	NOTES
		A6	A5	A4	A3	A2	A1	A0		ACK (A)		TX	NV	V	R3	R2	R1	R0	ACK (A)	D7	D6	D5	D4	D3	D2	D1	D0	ACK (A)		
VREG		0	1	0	1	A2	A1	A0	0		0	0	0	1	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0			
NVREG		0	1	0	1	A2	A1	A0	0		0	0	1	0	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0			WIPER A ONLY
NVREGxVREG		0	1	0	1	A2	A1	A0	0		0	1	1	0	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0			
VREGxNVREG		0	1	0	1	A2	A1	A0	0		0	1	0	1	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0			
VREG		0	1	0	1	A2	A1	A0	0		0	0	0	1	0	0	1	0		D7	D6	D5	D4	D3	D2	D1	D0			
NVREG		0	1	0	1	A2	A1	A0	0		0	0	1	0	0	0	1	0		D7	D6	D5	D4	D3	D2	D1	D0			WIPER B ONLY
NVREGxVREG		0	1	0	1	A2	A1	A0	0		0	1	1	0	0	0	1	0		D7	D6	D5	D4	D3	D2	D1	D0			
VREGxNVREG		0	1	0	1	A2	A1	A0	0		0	1	0	1	0	0	1	0		D7	D6	D5	D4	D3	D2	D1	D0			
VREG		0	1	0	1	A2	A1	A0	0		0	0	0	1	0	0	1	1		D7	D6	D5	D4	D3	D2	D1	D0			
NVREG		0	1	0	1	A2	A1	A0	0		0	0	1	0	0	0	1	1		D7	D6	D5	D4	D3	D2	D1	D0			WIPERS A AND B
NVREGxVREG		0	1	0	1	A2	A1	A0	0		0	1	1	0	0	0	1	1		D7	D6	D5	D4	D3	D2	D1	D0			
VREGxNVREG		0	1	0	1	A2	A1	A0	0		0	1	0	1	0	0	1	1		D7	D6	D5	D4	D3	D2	D1	D0			

Standby

The MAX5477/MAX5478/MAX5479 feature a low-power standby mode. When the device is not being programmed, it enters into standby mode and supply current drops to 500nA (typ).

Applications Information

The MAX5477/MAX5478/MAX5479 are ideal for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or for programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 9 and 10 show an application where the MAX5477/MAX5478/MAX5479 provide an adjustable, positive LCD bias voltage. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 9) or by a fixed resistor and a variable resistor (see Figure 10).

Programmable Filter

Figure 11 shows the MAX5477/MAX5478/MAX5479 in a 1st-order programmable application filter. Adjust the gain of the filter with R_2, and set the cutoff frequency with R_3. Use the following equations to calculate the gain (A) and the -3dB cutoff frequency (f_C):

$$A = 1 + \frac{R_1}{R_2}$$

$$f_C = \frac{1}{2\pi \times R_3 \times C}$$

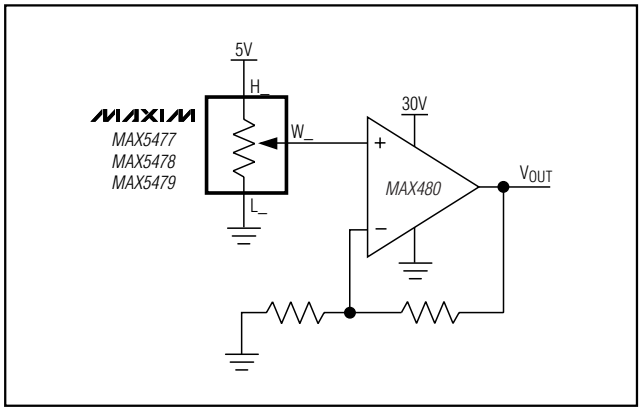


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

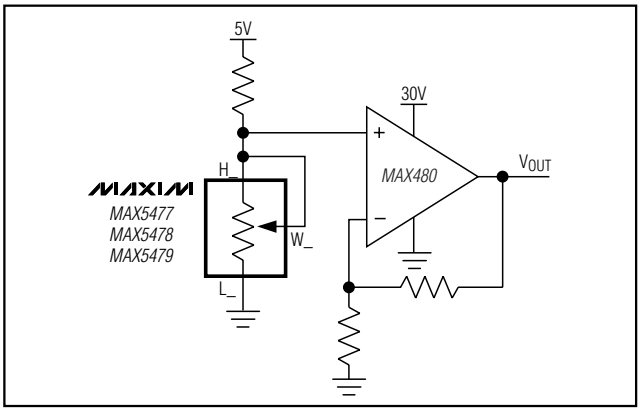


Figure 10. Positive LCD Bias Control Using a Variable Resistor

256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

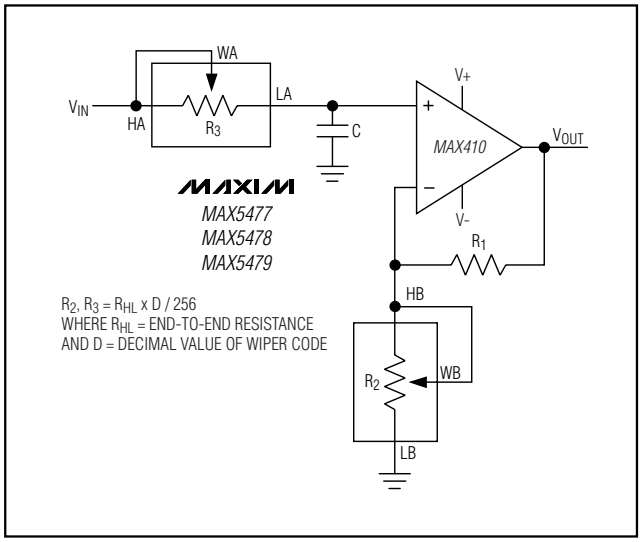


Figure 11. Programmable Filter

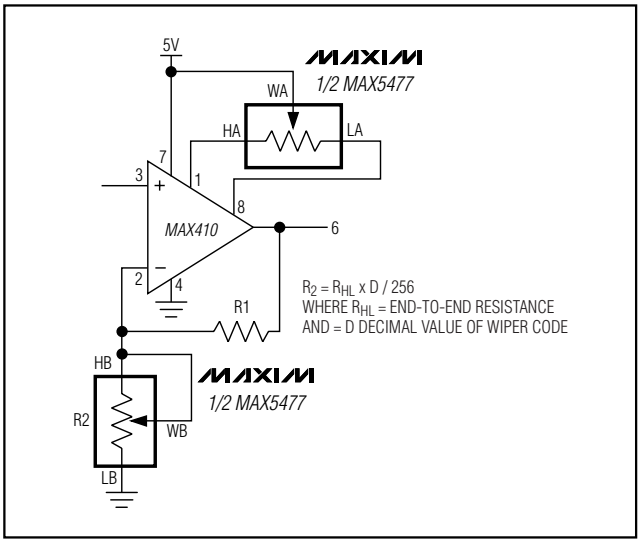


Figure 12. Offset Voltage Adjustment Circuit

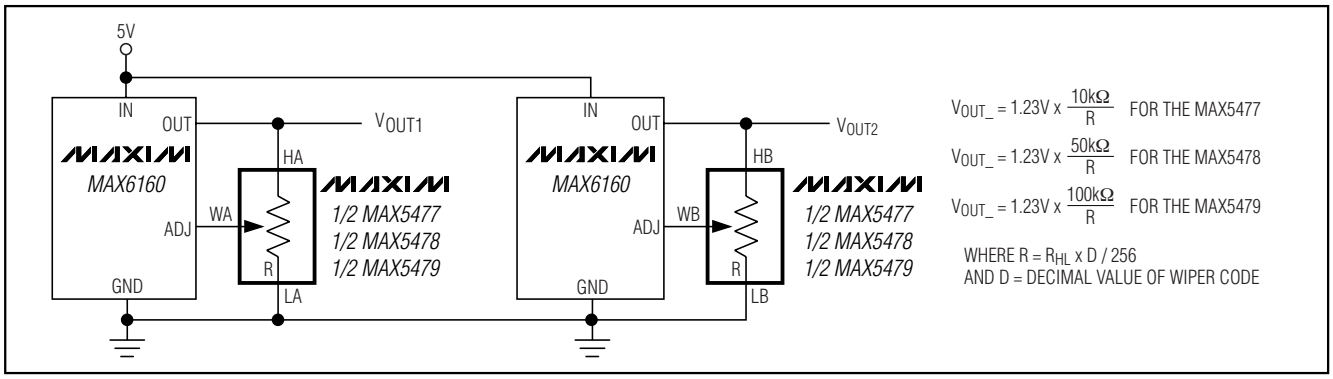
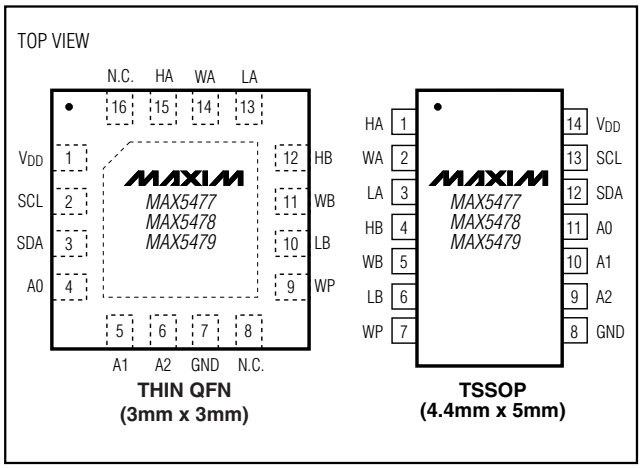


Figure 13. Adjustable Voltage Reference

Pin Configurations



Offset Voltage and Gain Adjustment

Connect the high and low terminals of one potentiometer of a MAX5477 between the NULL inputs of a MAX410 and the wiper to the op amp's positive supply to nullify the offset voltage over the operating temperature range. Install the other potentiometer in the feedback path to adjust the gain of the MAX410 (Figure 12).

Adjustable Voltage Reference

Figure 13 shows the MAX5477/MAX5478/MAX5479 used as the feedback resistors in multiple adjustable voltage reference applications. Independently adjust the output voltages of the MAX6160 parts from 1.23V to V_{IN} - 0.2V by changing the wiper positions of the MAX5477/MAX5478/MAX5479.

Chip Information

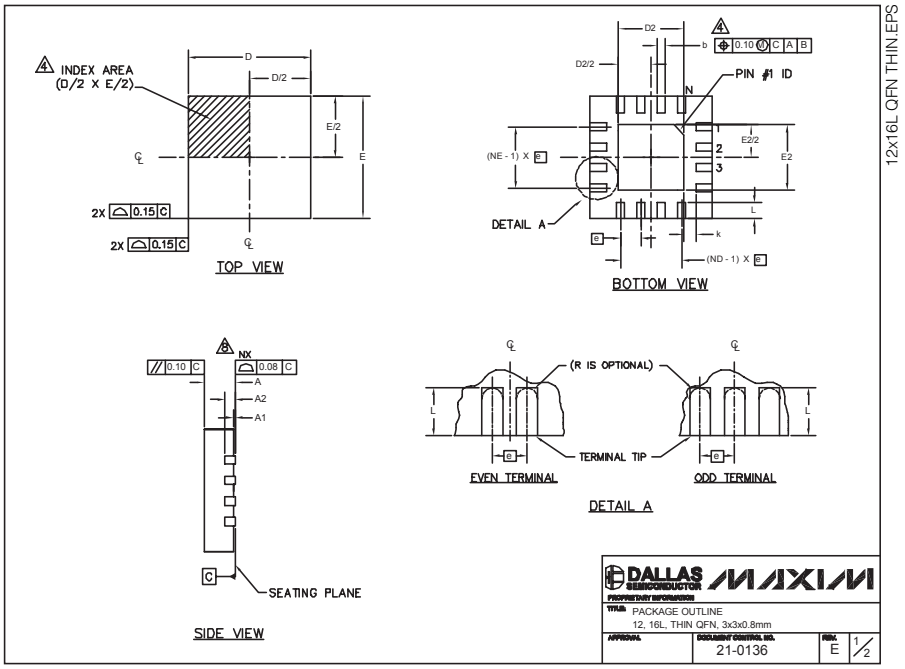
TRANSISTOR COUNT: 12,651

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.85	0.90	0.95	0.85	0.90	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

⚠4 THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

⚠5 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.

⚠6 ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

⚠8 COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

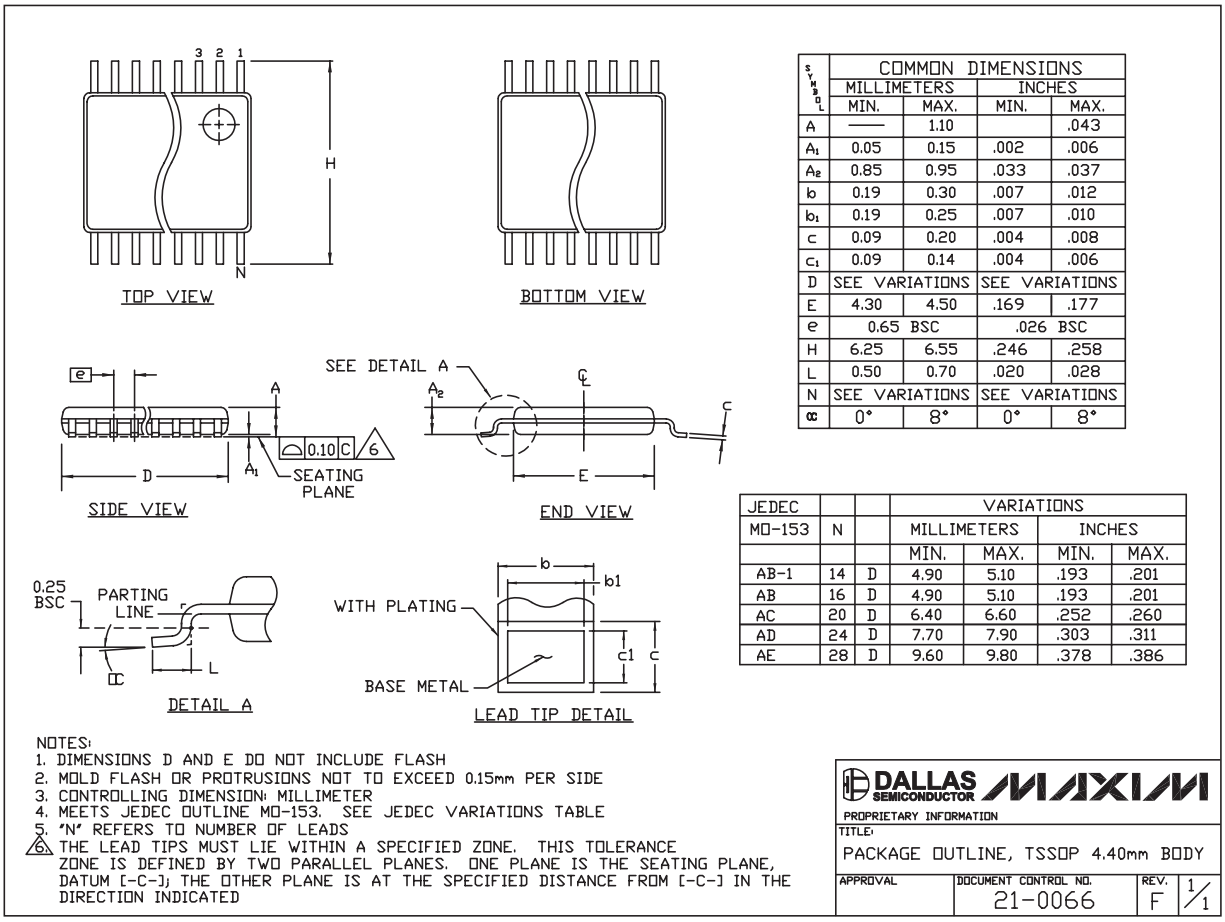
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0136
REV. E
2/2

Dual, 256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1