

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

## description

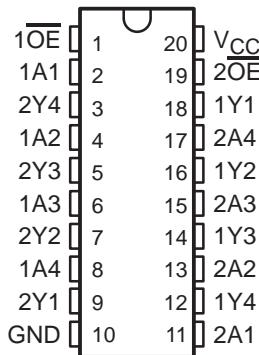
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F241 and 'F244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $OE$  and  $\overline{OE}$  inputs.

The 'F240 is organized as two 4-bit buffers/line drivers with separate output enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

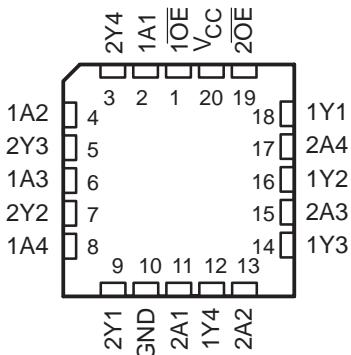
The SN74F240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F240 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F240 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54F240 . . . J PACKAGE  
SN74F240 . . . DB, DW, OR N PACKAGE  
(TOP VIEW)



SN54F240 . . . FK PACKAGE  
(TOP VIEW)



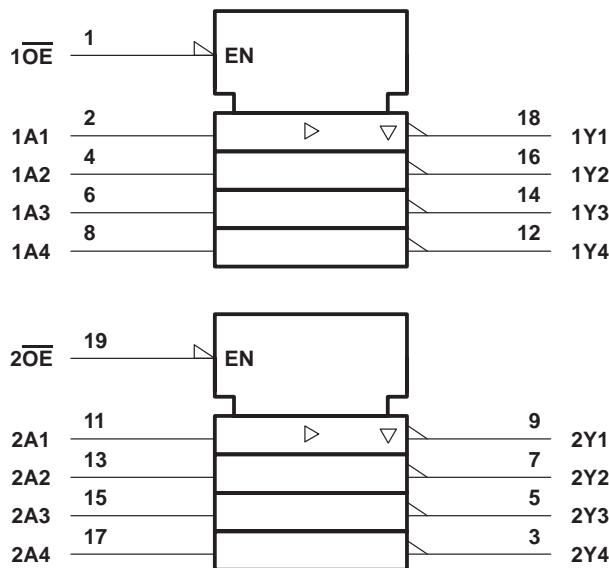
FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

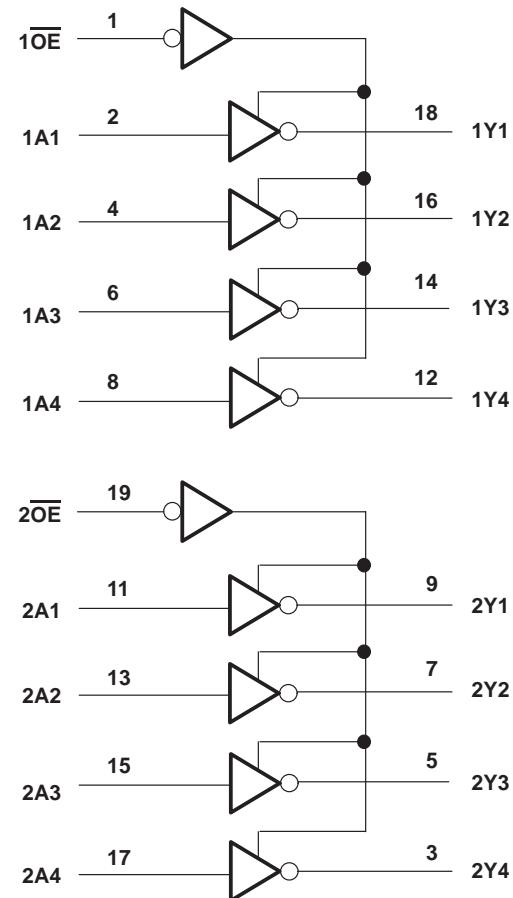
# SN54F240, SN74F240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDFS061A - D2932, MARCH 1987 - REVISED OCTOBER 1993

## logic symbol†



## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

**recommended operating conditions**

		SN54F240			SN74F240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55	125		0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54F240			SN74F240			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.3	2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2				
		I <sub>OH</sub> = -15 mA			2	3.1		
	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -3 mA					2.7		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.38	0.55				V
		I <sub>OL</sub> = 64 mA				0.42	0.55	
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50			50	µA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50			-50	µA
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20			20	µA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V			-1			-1	mA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0	-100	-225	-100	-225			mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	Outputs high	19	29	19	29		mA
		Outputs low	50	75	50	75		
		Outputs disabled	42	63	42	63		

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**SN54F240, SN74F240  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SDFS061A – D2932, MARCH 1987 – REVISED OCTOBER 1993

**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†			UNIT	
			'F240			SN54F240		SN74F240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Any A	Y	2.2	4.7	7	2.2	9	2.2	8	ns
t <sub>PHL</sub>			1.2	3.1	4.7	1.2	6	1.2	5.7	
t <sub>PZH</sub>	OE	Y	1.2	3.1	5.3	1.2	6.7	1.2	6.1	ns
t <sub>PZL</sub>			3.2	6.5	9	3.2	10.5	3.2	10	
t <sub>PHZ</sub>	OE	Y	1.2	3.6	5.3	1.2	6.5	1.2	6.3	ns
t <sub>PLZ</sub>			1.2	5.6	8	1.2	12.5	1.2	9.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9758501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9758501Q2A SNJ54F 240FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9758501QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758501QR A SNJ54F240J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9758501QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758501QS A SNJ54F240W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/33201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 33201B2A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/33201BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33201BRA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/33201BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33201BSA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/33201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 33201B2A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/33201BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33201BRA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/33201BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33201BSA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54F240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54F240J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F240DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SN74F240DBR	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F240	
SN74F240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F240DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F240N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F240NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74F240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54F240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9758501Q2A SNJ54F240FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54F240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758501QR A SNJ54F240J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54F240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758501QS A SNJ54F240W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54F240, SN74F240 :**

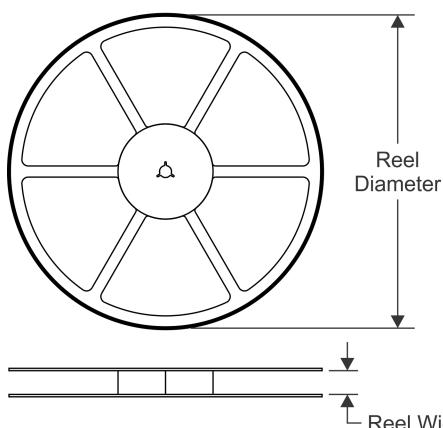
- Catalog: [SN74F240](#)
- Military: [SN54F240](#)

NOTE: Qualified Version Definitions:

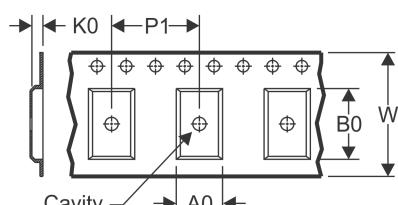
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

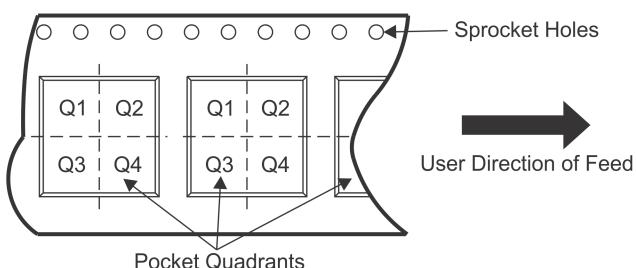


## TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74F240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1	
SN74F240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1	
SN74F240NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1	

**TAPE AND REEL BOX DIMENSIONS**

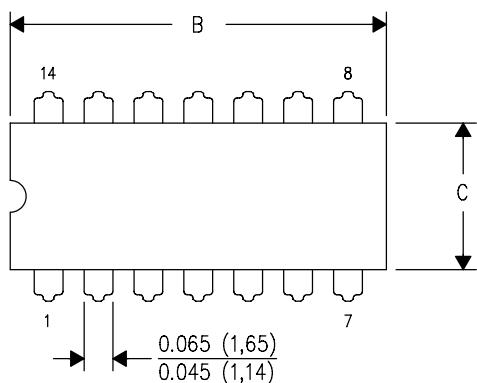

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F240DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74F240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74F240NSR	SO	NS	20	2000	367.0	367.0	45.0

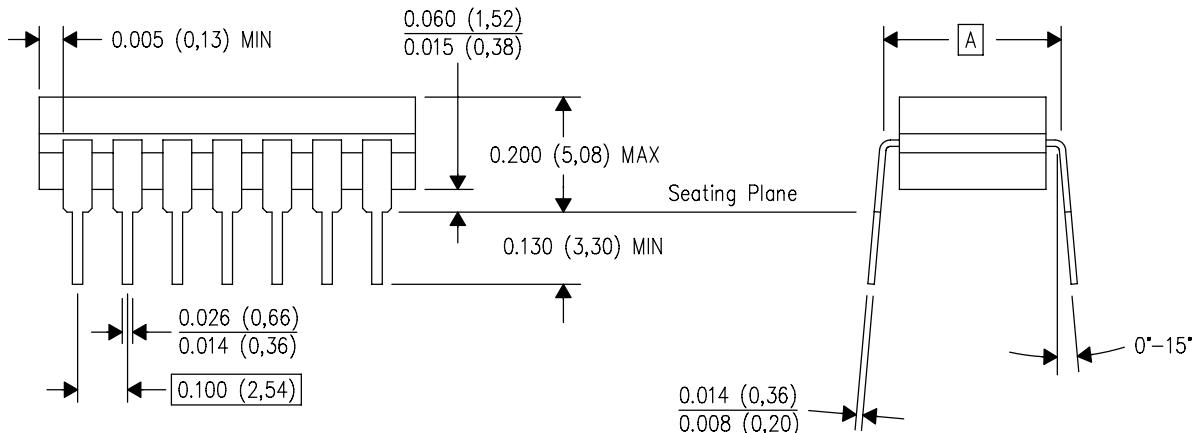
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

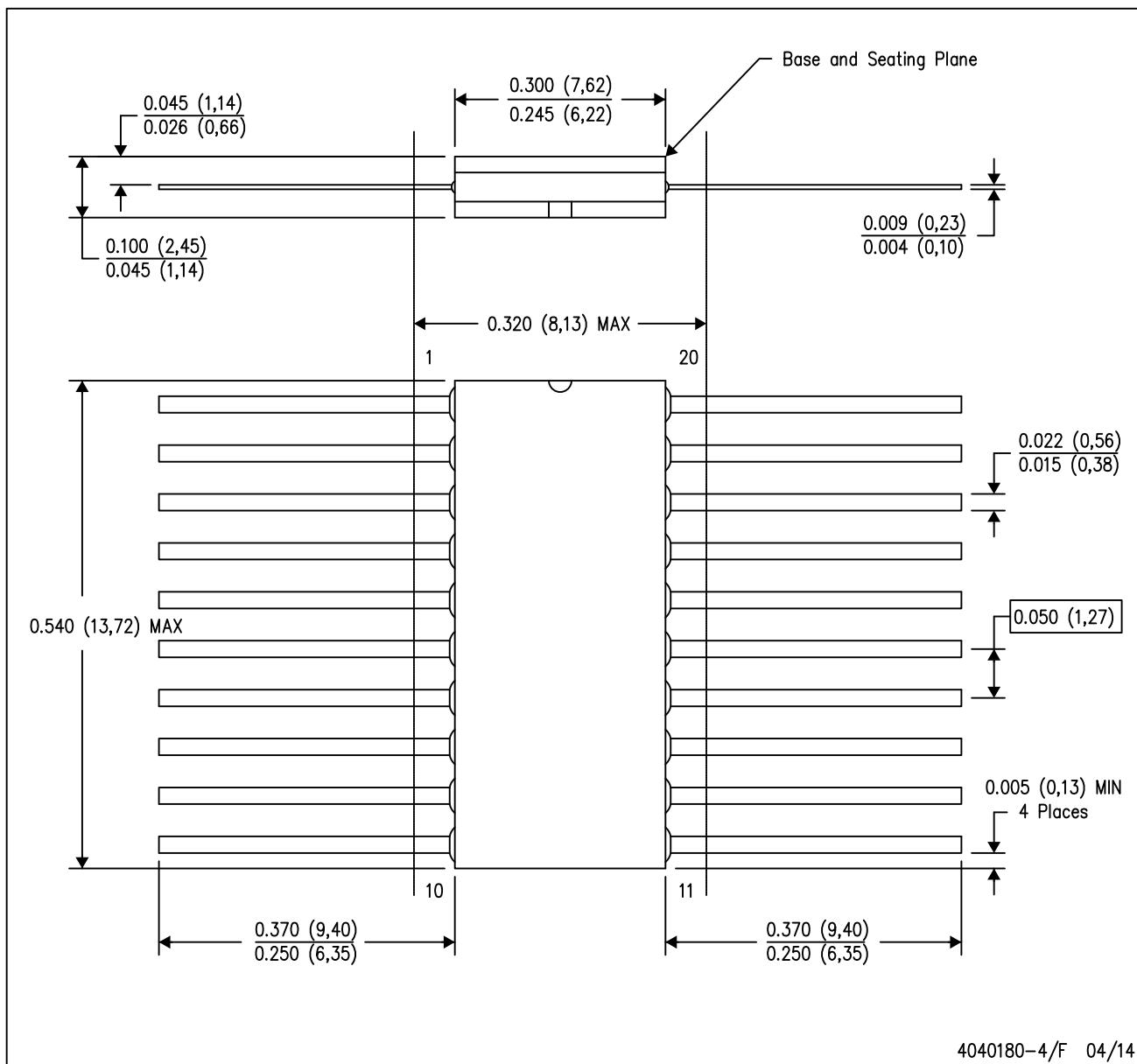


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



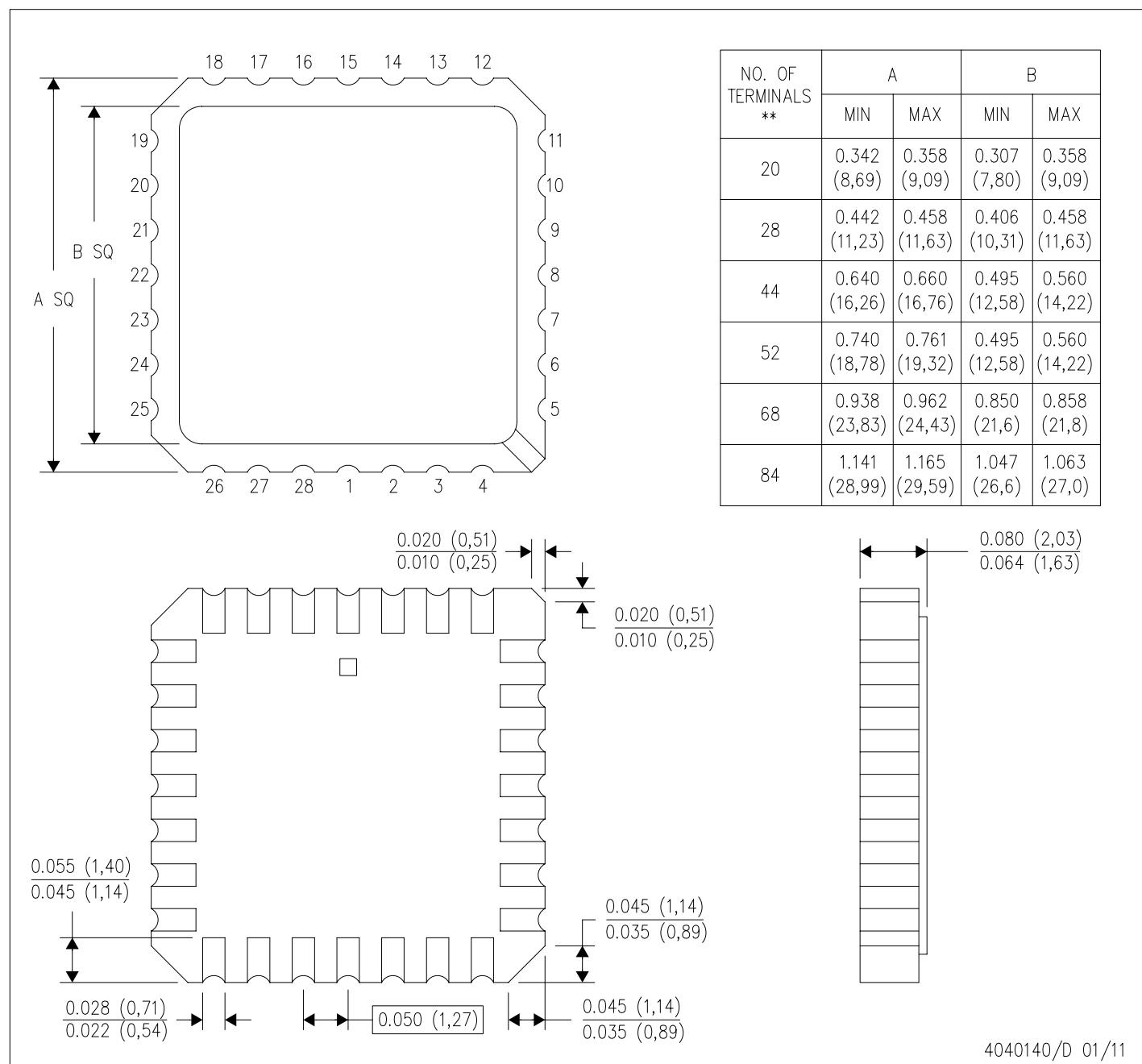
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

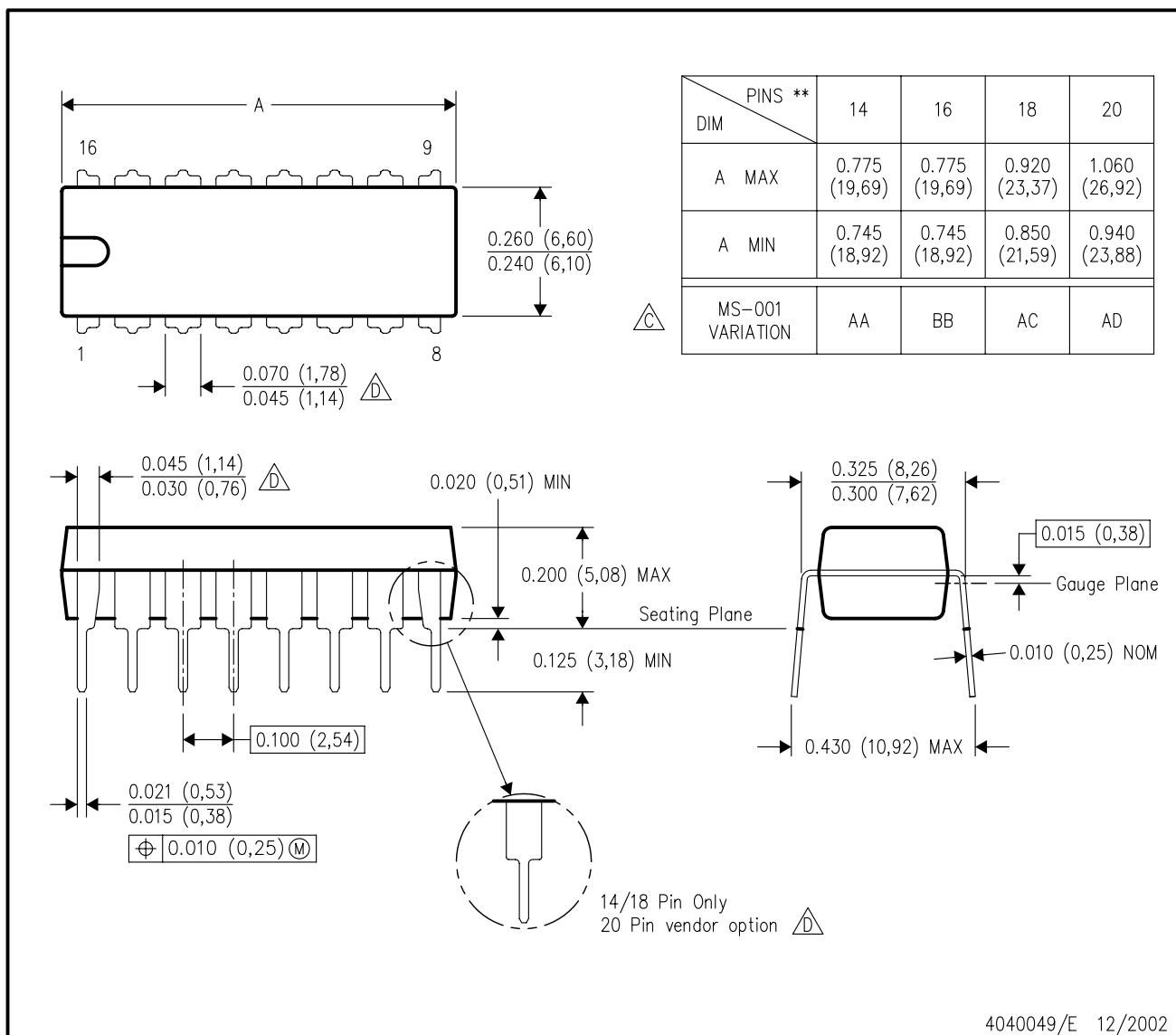
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



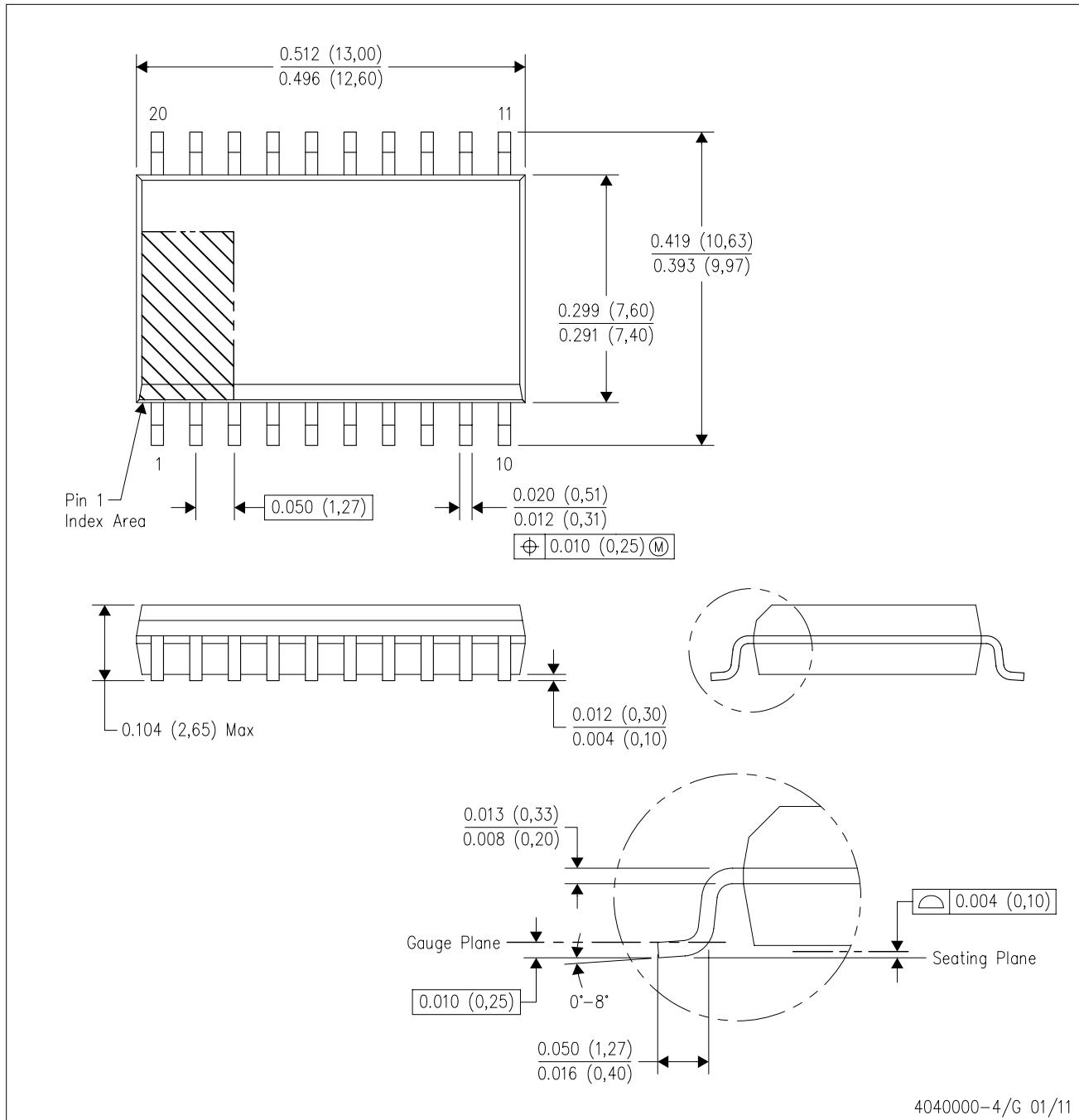
NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

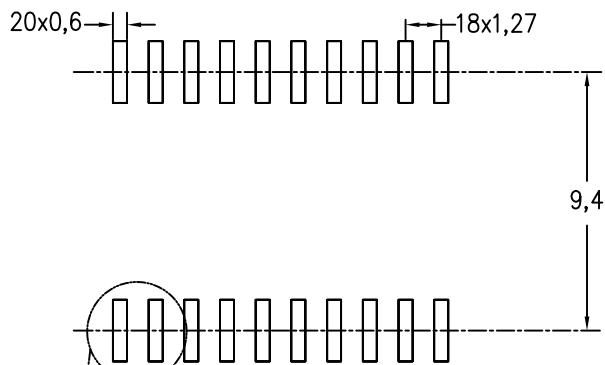
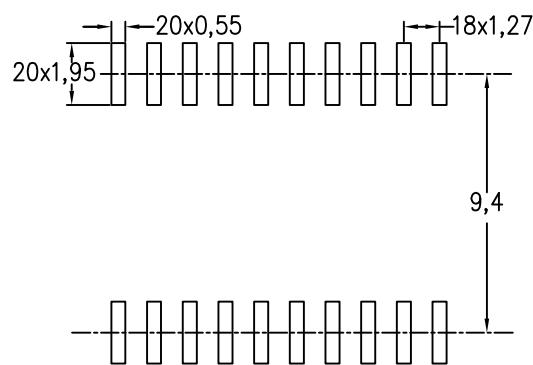


NOTES:

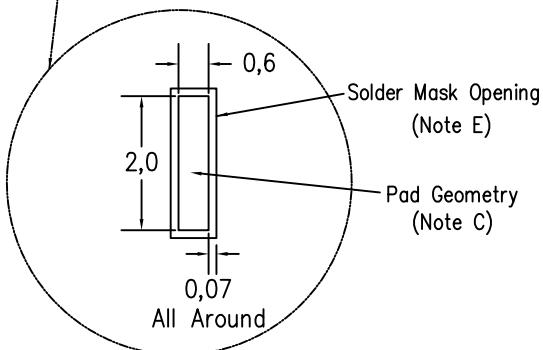
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/F 08/13

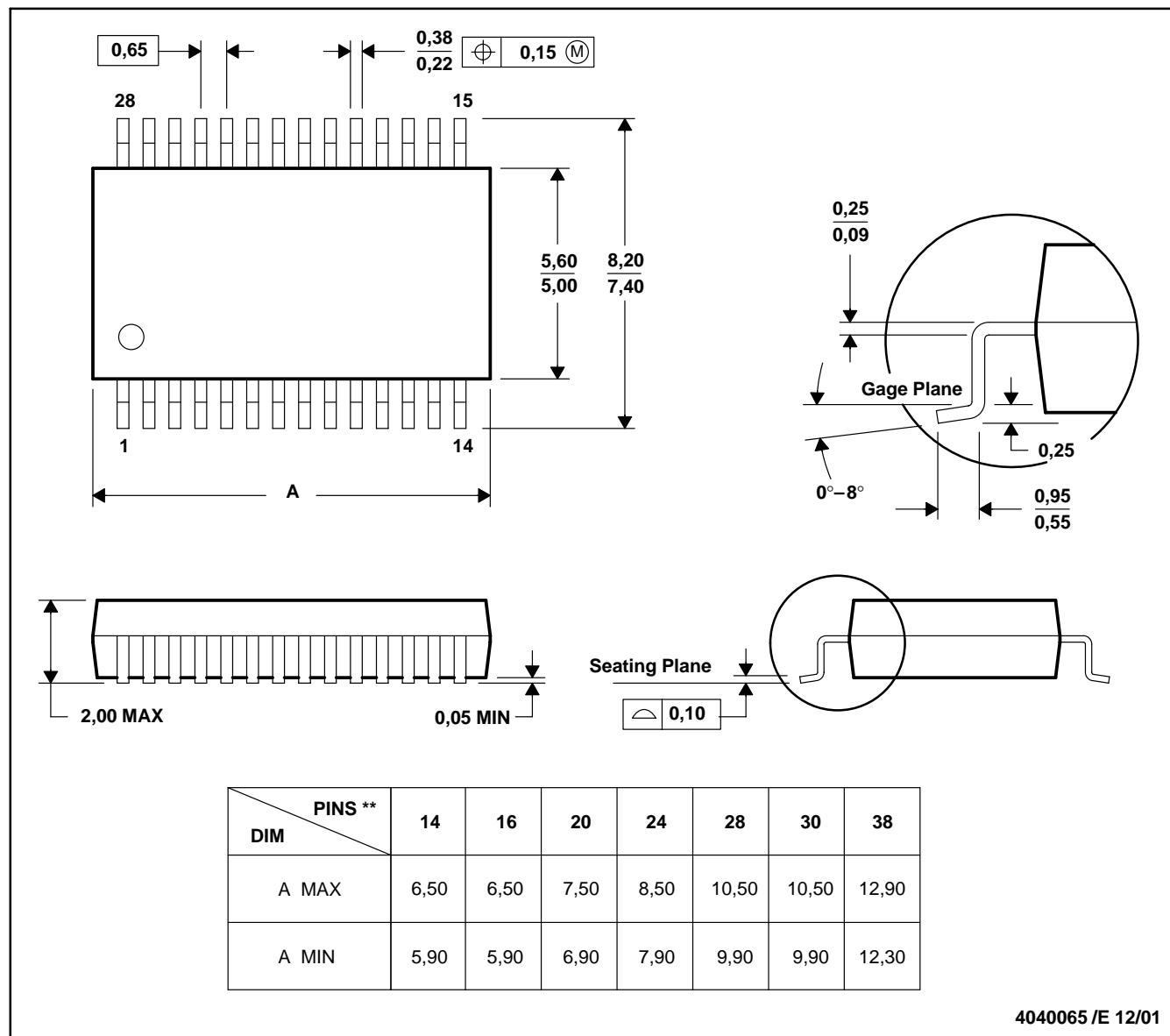
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



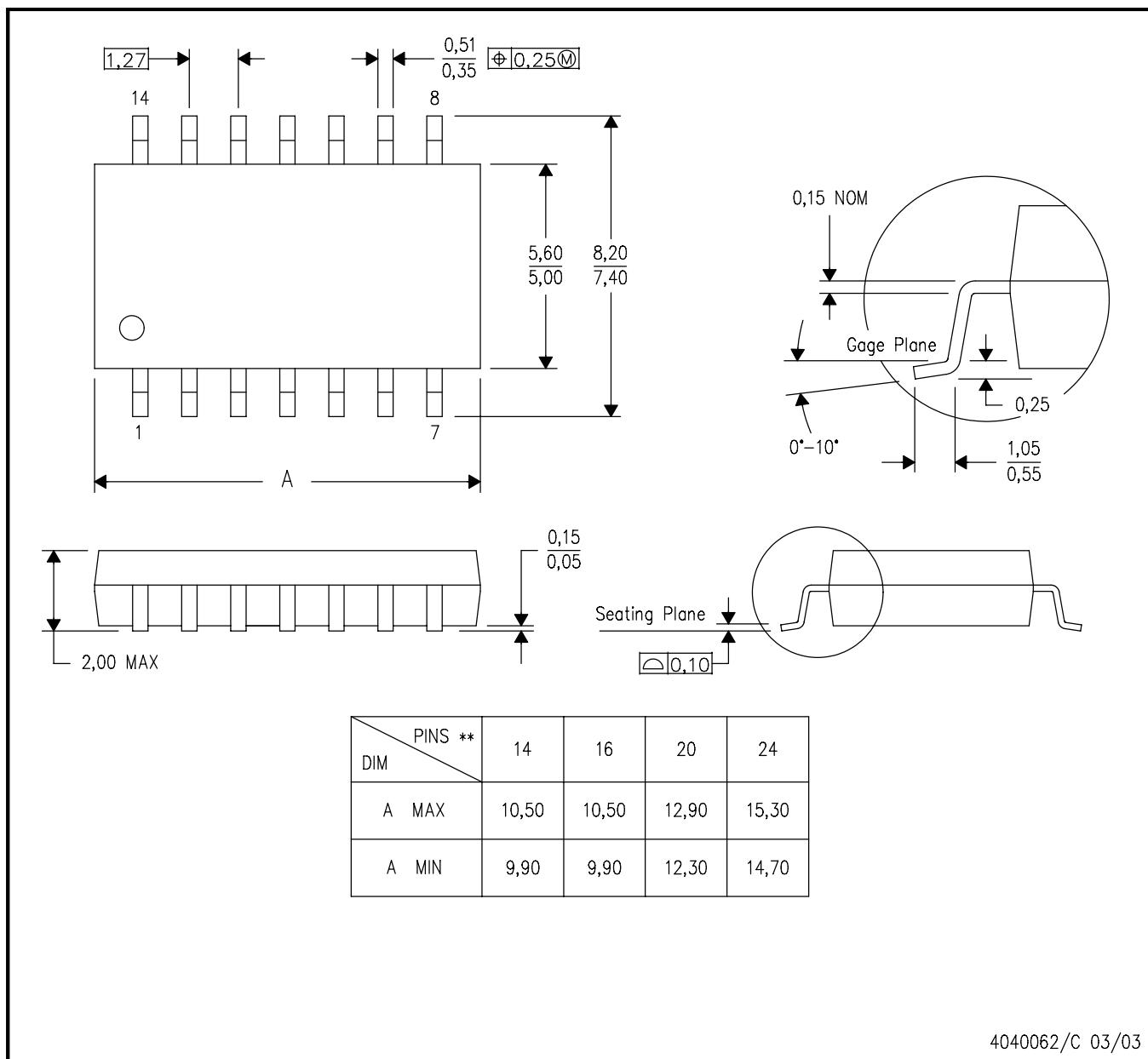
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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