PD- 93774A

International
IOR Rectifier

SMPS MOSFET

IRF820AS
IRF820AL

HEXFET® Power MOSFET

Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V_{DSS}	R_{DS}(on) max	I_D
500V	**3.0Ω**	**2.5A**

Benefits
- Low Gate Charge Qg Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{OSS} specified (See AN 1001)

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TO-262
IRF820AL

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑥	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑥	1.6	
I_{DM}	Pulsed Drain Current ①⑥	10	
P_D @T_C = 25°C	Power Dissipation	50	W
	Linear Derating Factor	0.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③⑥	3.4	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies:

- Two Transistor Forward
- Half Bridge and Full Bridge

Notes ① through ⑤ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V_{GS} = 10V, I_D = 1.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	1.4	—	—	S	V_{DS} = 50V, I_D = 1.5A⑥
Q_g	Total Gate Charge	—	—	17	nC	I_D = 2.5A
Q_{gs}	Gate-to-Source Charge	—	—	4.3		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.5		V_{GS} = 10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	8.1	—	ns	V_{DD} = 250V
t_r	Rise Time	—	12	—		I_D = 2.5A
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		R_G = 21Ω
t_f	Fall Time	—	13	—		R_D = 97Ω,See Fig. 10 ④⑥
C_{iss}	Input Capacitance	—	340	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	53	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	2.7	—		f = 1.0MHz, See Fig. 5⑥
C_{oss}	Output Capacitance	—	490	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	15	—		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	28	—		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤⑥

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②⑥	—	140	mJ
I_{AR}	Avalanche Current①	—	2.5	A
E_{AR}	Repetitive Avalanche Energy①	—	5.0	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	10		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J = 25°C, I_S = 2.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	330	500	ns	T_J = 25°C, I_F = 2.5A
Q_{rr}	Reverse RecoveryCharge	—	760	1140	nC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

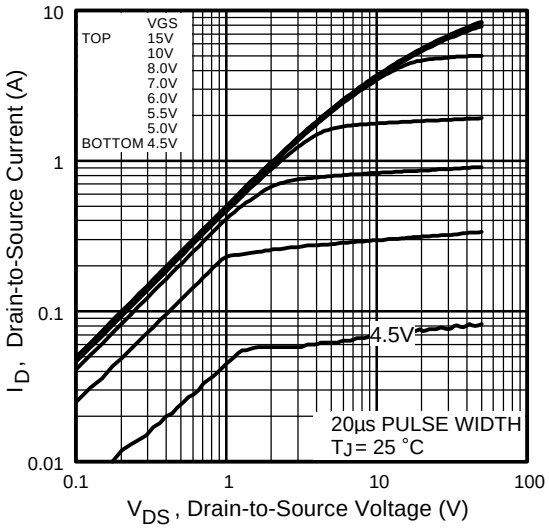


Fig 1. Typical Output Characteristics

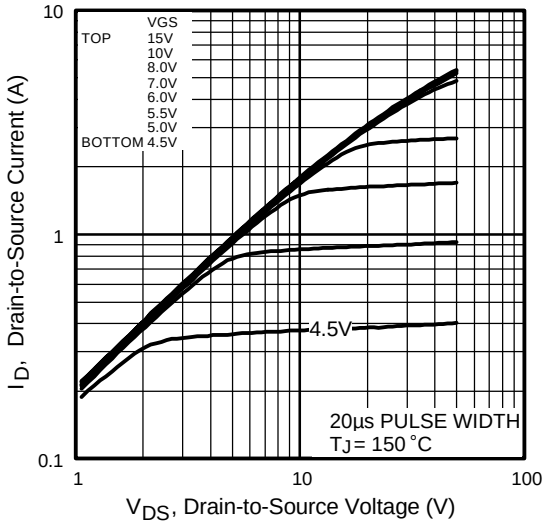


Fig 2. Typical Output Characteristics

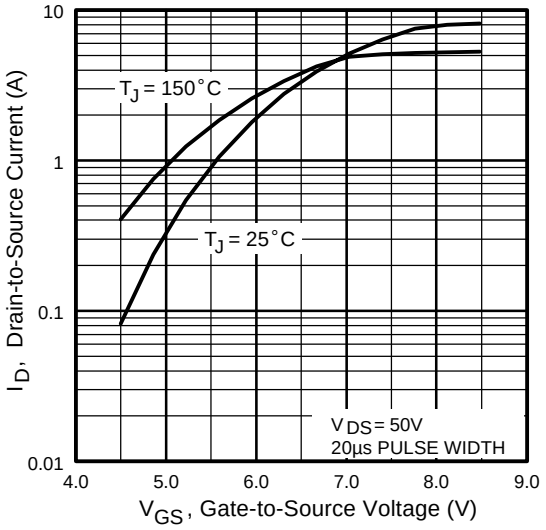


Fig 3. Typical Transfer Characteristics

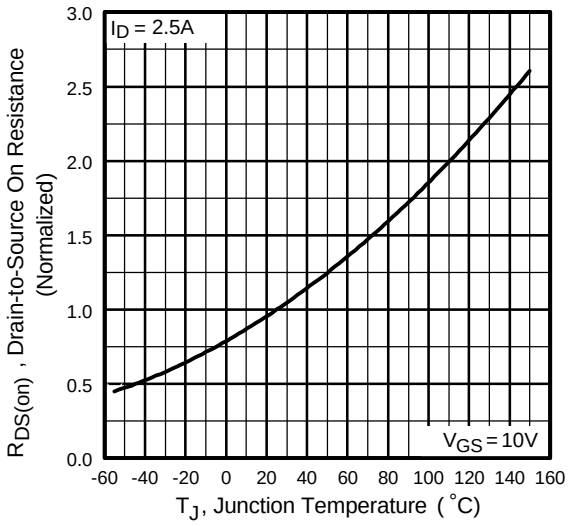


Fig 4. Normalized On-Resistance Vs. Temperature

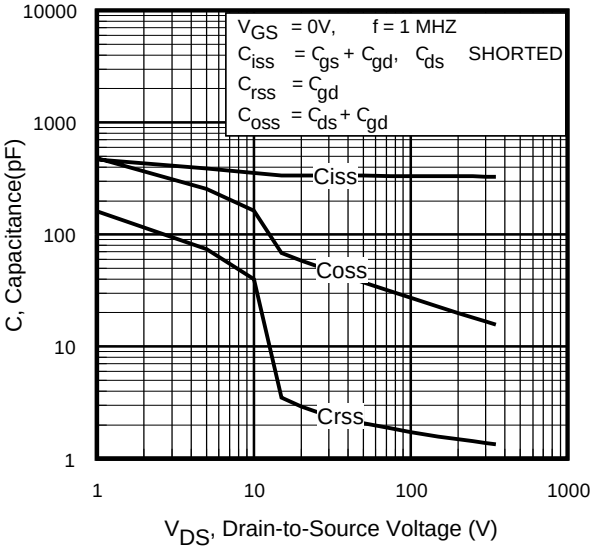


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

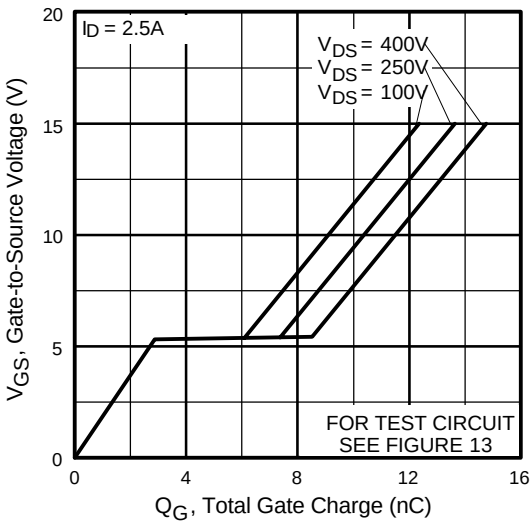


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

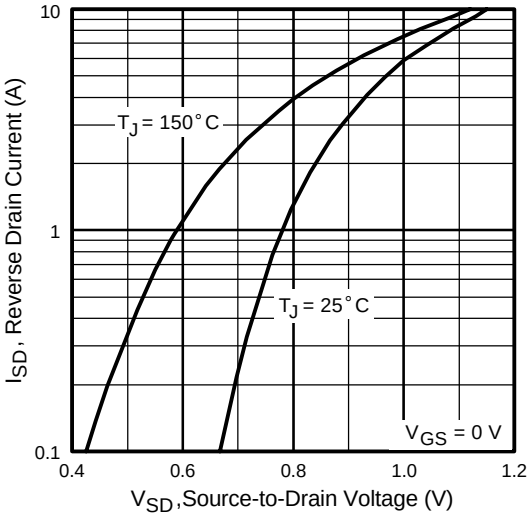


Fig 7. Typical Source-Drain Diode Forward Voltage

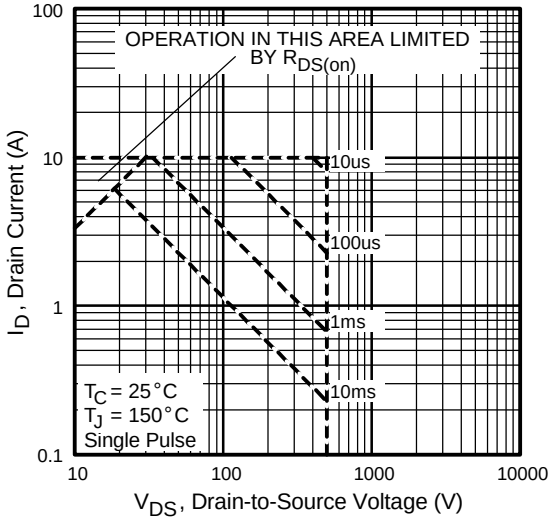


Fig 8. Maximum Safe Operating Area

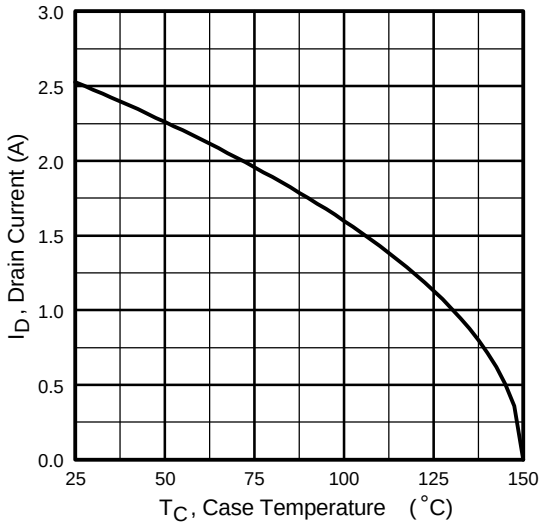


Fig 9. Maximum Drain Current Vs. Case Temperature

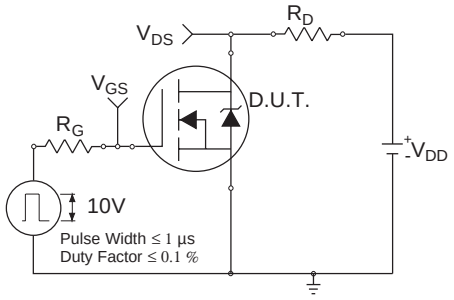


Fig 10a. Switching Time Test Circuit

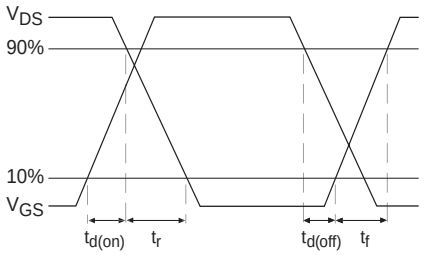


Fig 10b. Switching Time Waveforms

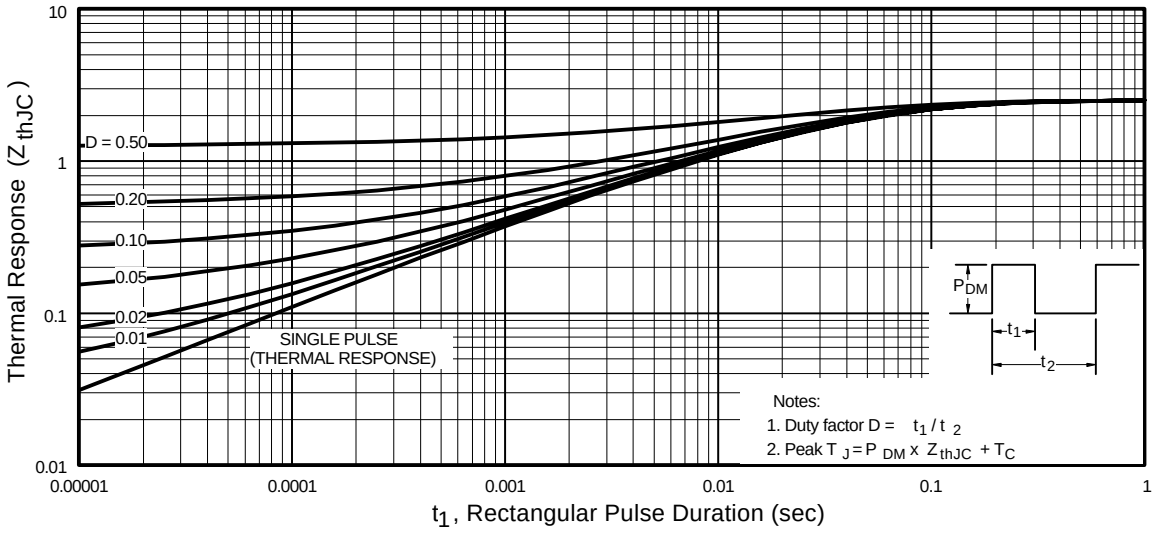


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

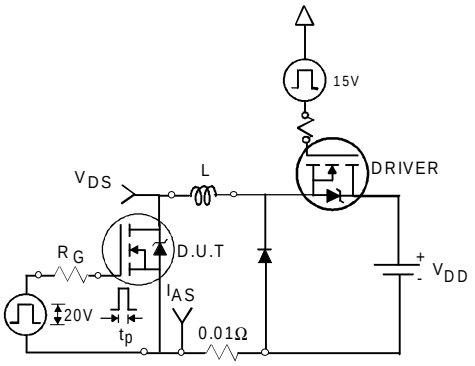


Fig 12a. Unclamped Inductive Test Circuit

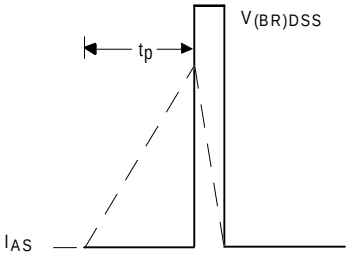


Fig 12b. Unclamped Inductive Waveforms

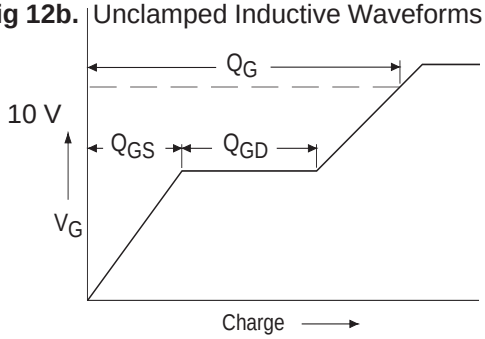


Fig 13a. Basic Gate Charge Waveform

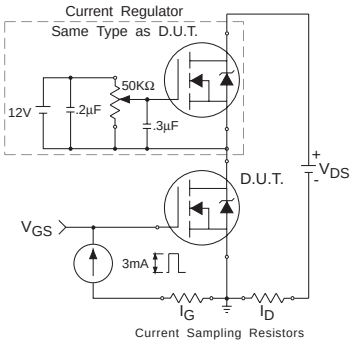


Fig 13b. Gate Charge Test Circuit

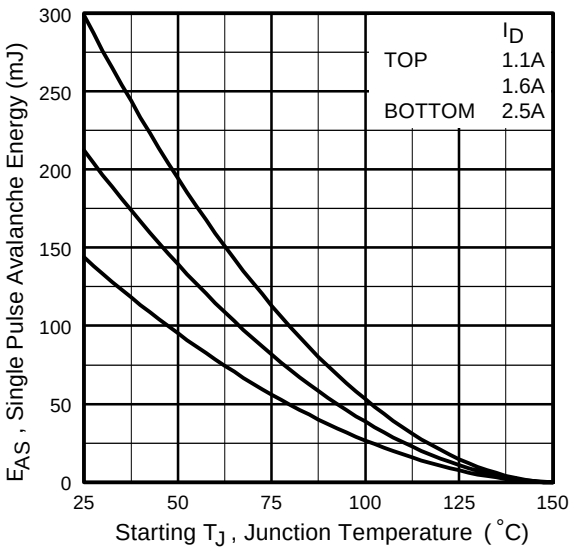


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

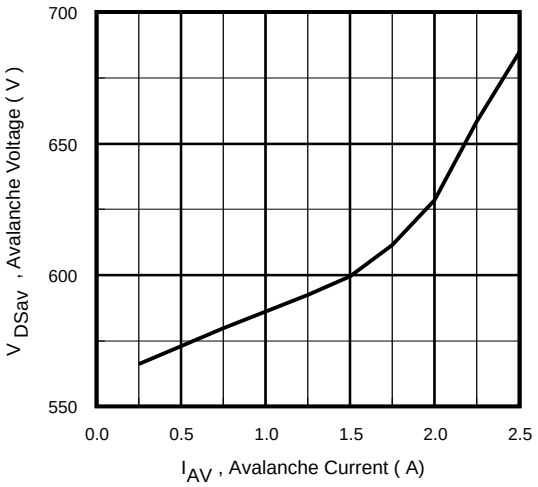
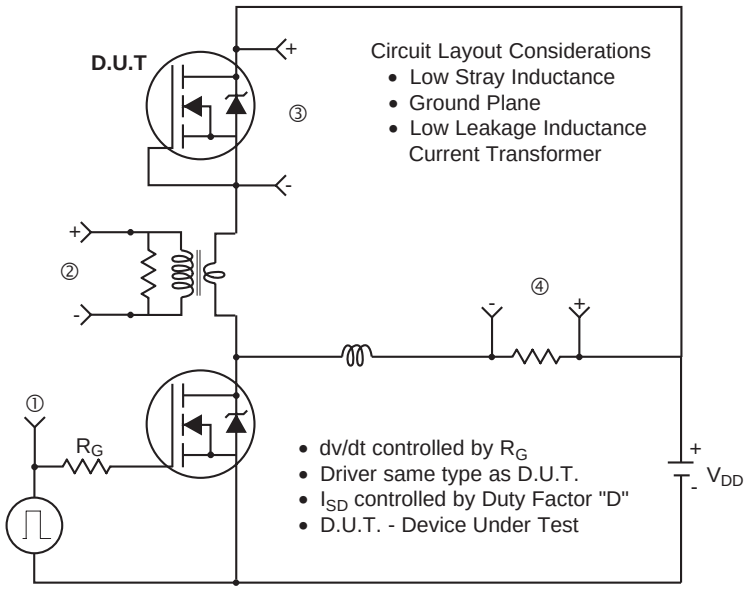
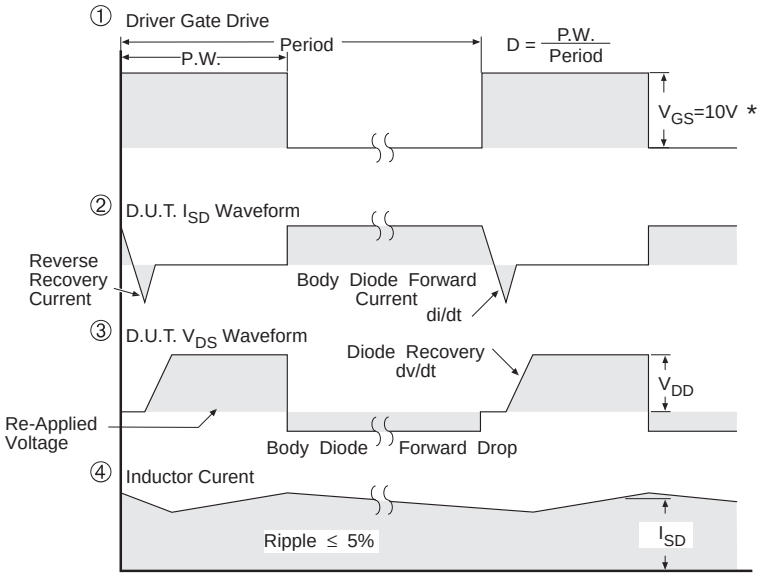


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit

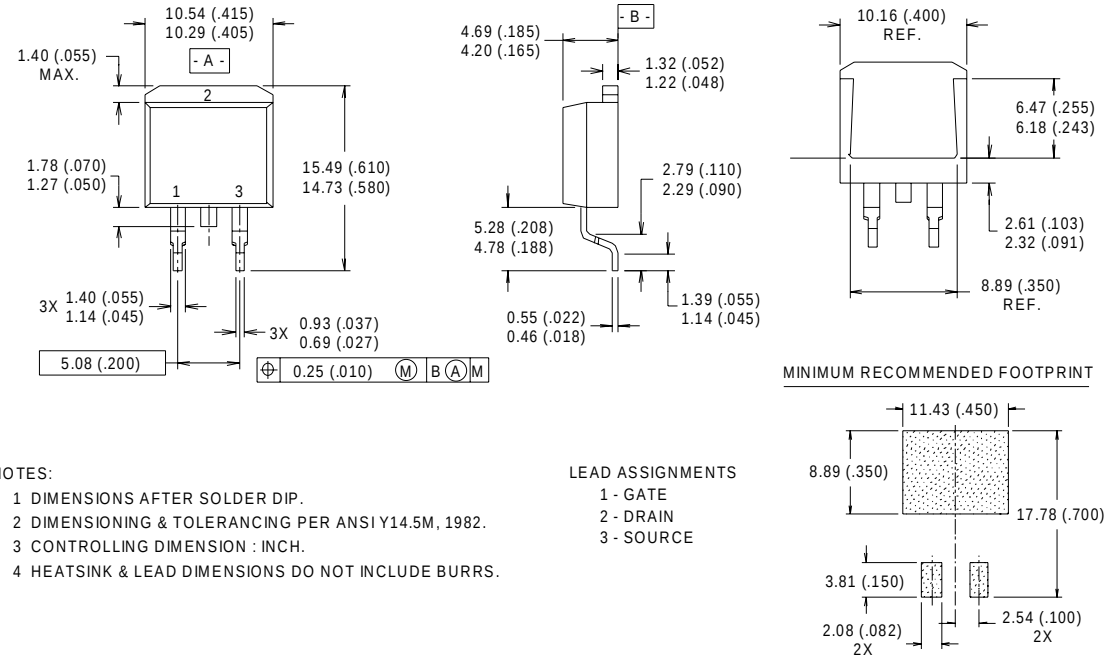




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® power MOSFETs

D²Pak Package Outline

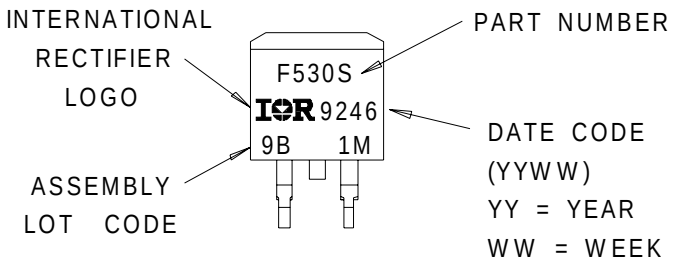


NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

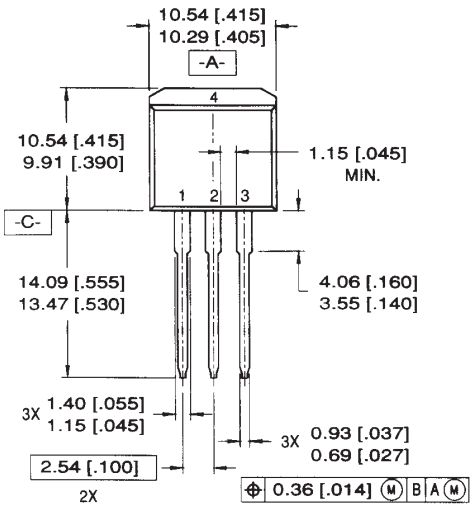
Part Marking Information

D²Pak



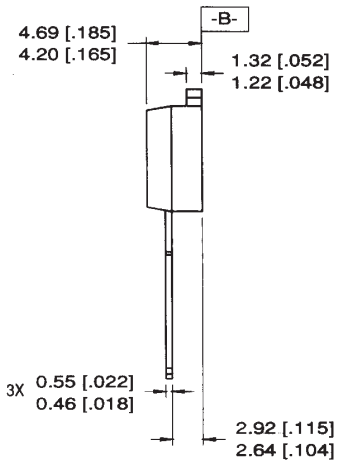
Package Outline

TO-262



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN



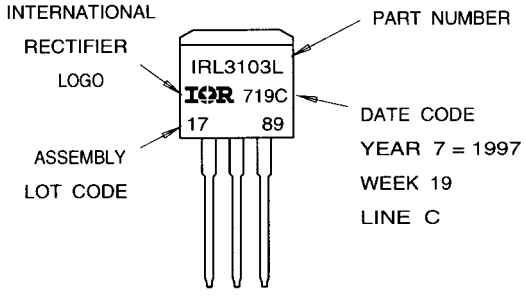
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

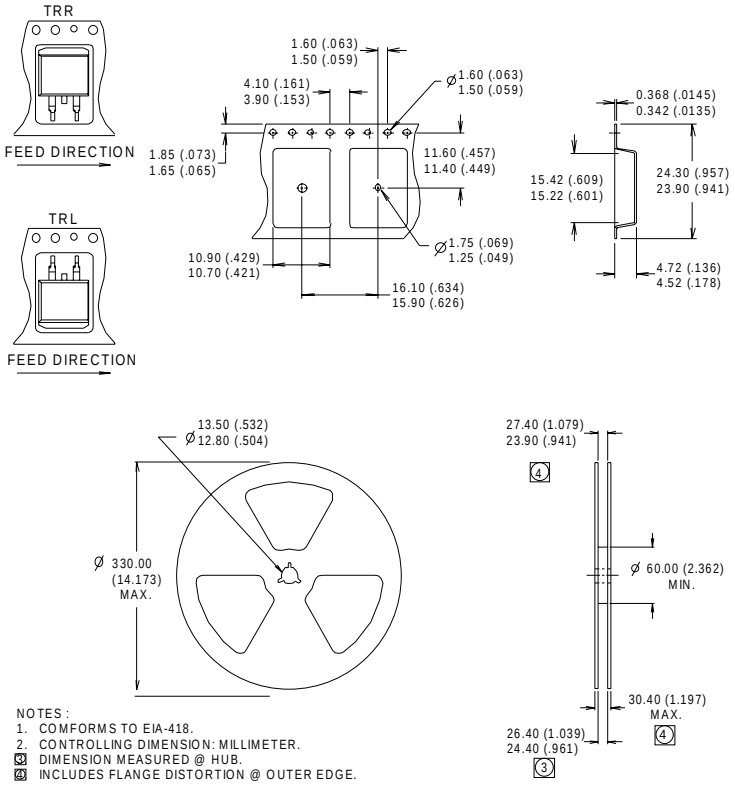
TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Tape & Reel Information

D²Pak



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 45mH R_G = 25Ω, I_{AS} = 2.5A. (See Figure 12)

③ $I_{SD} \leq$ 2.5A, di/dt ≤ 270A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Uses IRF820A data and test conditions

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

International
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Data and specifications subject to change without notice. 5/00