

256K (32K x 8) CMOS EPROM

FEATURES

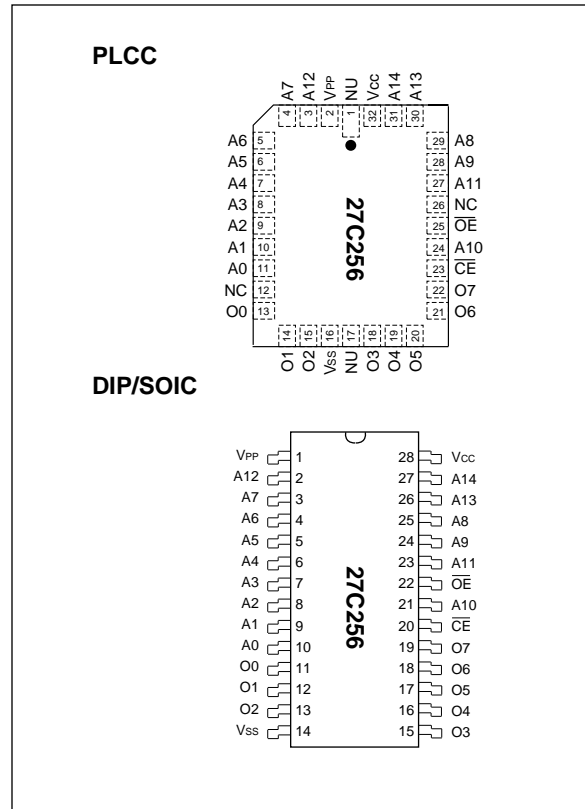
- High speed performance
 - 90 ns access time available
- CMOS Technology for low power consumption
 - 20 mA Active current
 - 100 μ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin PLCC Package
 - 28-pin SOIC package
 - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C
 - Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming -0.6V to +14.0V

Voltage on A9 w.r.t. VSS -0.6V to +13.5V

Output voltage w.r.t. VSS -0.6V to VCC +1.0V

Storage temperature -65°C to +150°C

Ambient temp. with power applied -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%) Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C							
Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	I _{LI}	-10	10	μA	V _{IN} = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400 μA I _{OL} = 2.1 mA
Output Leakage	all	—	I _{LO}	-10	10	μA	V _{OUT} = 0V to VCC
Input Capacitance	all	—	C _{IN}	—	6	pF	V _{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C _{OUT}	—	12	pF	V _{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	I _{CC1} I _{CC2}	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE} = \overline{CE} = V_{IL}$; I _{OUT} = 0 mA; V _{IL} = -0.1 to 0.8V; V _{IH} = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	I _{CC(S)}	—	2 3 100	mA mA μA	$\overline{CE} = VCC \pm 0.2V$
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	VCC-0.7	100 VCC	μA V	VPP = 5.5V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

		AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$ $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial: $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ Automotive: $T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$											
Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t _{ACC}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
\overline{CE} to Output Delay	t _{CE}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE} = V_{IL}$
\overline{OE} to Output Delay	t _{OE}	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE} = V_{IL}$
\overline{CE} or \overline{OE} to O/P High Impedance	t _{OFF}	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address \overline{CE} or \overline{OE} , whichever goes first	t _{OH}	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = .45V$; $V_{OH} = 1.5V$ and $V_{OL} = 1.5V$
 Output Load: 1 TTL Load + 30pF

FIGURE 1-1: READ WAVEFORMS

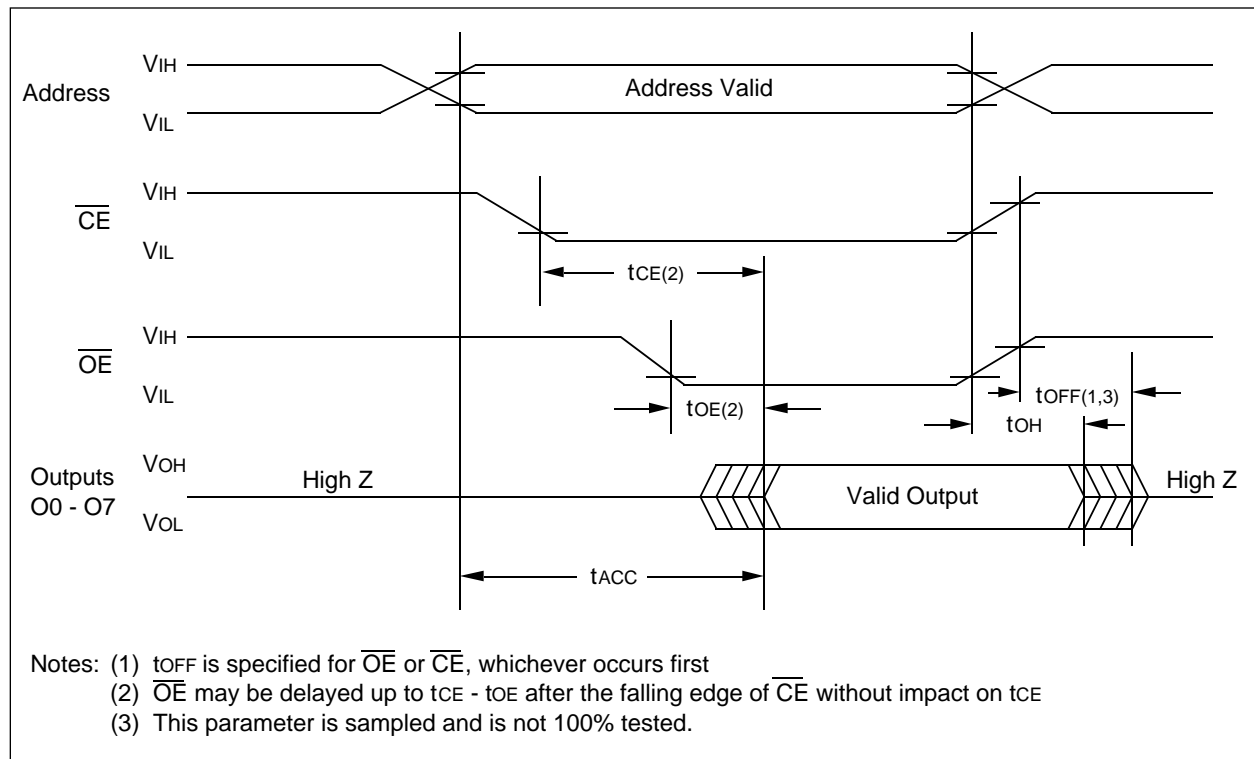


TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V						
Parameter	Status	Symbol	Min	Max.	Units	Conditions
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	μA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	0.45	V V	IOH = -400 μA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	I PP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: $V_{IH}=2.4V$ and $V_{IL}=0.45V$; $V_{OH}=2.0V$; $V_{OL}=0.8V$ Output Load: 1 TTL Load + 100pF Ambient Temperature: $T_{amb}=25^{\circ}C \pm 5^{\circ}C$ $V_{CC}= 6.5V \pm 0.25V$, $V_{PP} = V_H = 13.0V \pm 0.25V$				
Parameter	Symbol	Min.	Max.	Units	Remarks
Address Set-Up Time	tAS	2	—	μs	
Data Set-Up Time	tDS	2	—	μs	
Data Hold Time	tDH	2	—	μs	
Address Hold Time	tAH	0	—	μs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	μs	
Program Pulse Width (1)	tPW	95	105	μs	100 μs typical
\overline{CE} Set-Up Time	tCES	2	—	μs	
\overline{OE} Set-Up Time	tOES	2	—	μs	
VPP Set-Up Time	tVPS	2	—	μs	
Data Valid from \overline{OE}	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 μs ±5%.

2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS

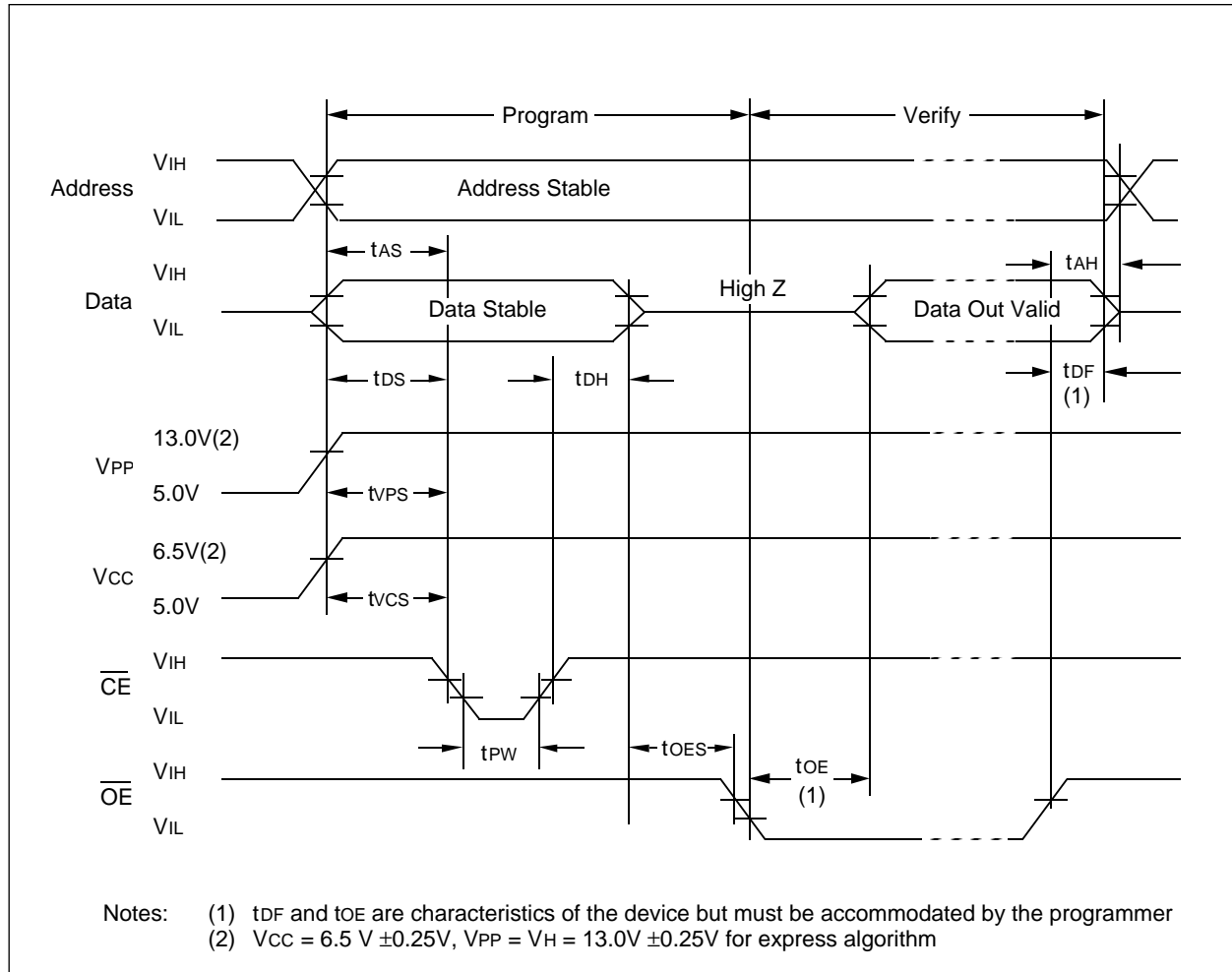


TABLE 1-6: MODES

Operation Mode	\overline{CE}	OE	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

- the \overline{CE} pin is low to power up (enable) the chip
- the \overline{OE} pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of \overline{OE} (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the \overline{CE} pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 μ A.

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The \overline{OE} pin is high and the program mode is not defined.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 μ W/cm² for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

- VCC is brought to the proper voltage,
- VPP is brought to the proper VH level,
- the \overline{OE} pin is high, and
- the \overline{CE} pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low going pulse on the \overline{CE} line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- VCC is at the proper level,
- VPP is at the proper VH level,
- the \overline{CE} line is high, and
- the \overline{OE} line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only \overline{CE} need be under separate control to each device. By pulsing the \overline{CE} line low on a particular device, that device will be programmed; all other devices with \overline{CE} held high will not be programmed with the data, although address and data will be available on their input pins.

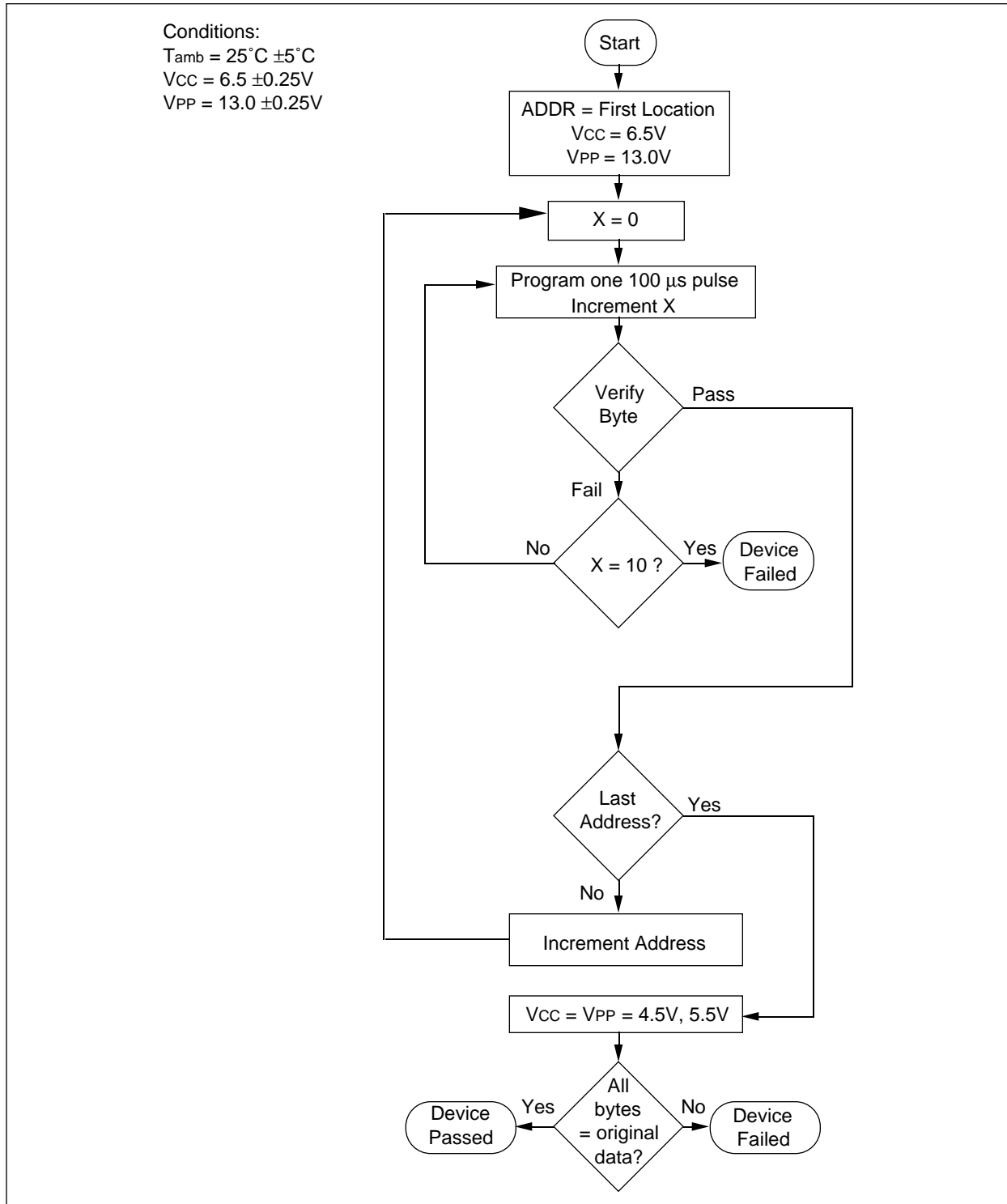
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The \overline{CE} and \overline{OE} lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin \rightarrow	Input	Output								
Identity \downarrow	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	H e x
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	8C

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C256

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27C256 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use listed part numbers, and refer to factory or listed sales offices.

27C256	-	90	I	/TS	
					Package:
					L = Plastic Leaded Chip Carrier
					P = Plastic DIP (Mil 600)
					SO = Plastic SOIC (Mil 300)
					Temperature Range:
					Blank = 0°C to +70°C
					I = -40°C to +85°C
					E = -40°C to +125°C
					Access Time:
					90 = 90 ns
					10 = 100 ns
					12 = 120 ns
					15 = 150 ns
					20 = 200 ns
					Device
					27C256 256K (32K x 8) CMOS EPROM

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

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Detroit

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Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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